Simple Digital Control Improving Dynamic Performance of Power Factor Preregulators

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***Abstract*— This paper presents the practical implementation of a fully digital control for boost power factor preregulators (PFP's). The control algorithm, which is simple and fast, provides a significant improvement in the system's dynamic performance compared to usual analog control techniques. The paper discusses the design criteria and the actions taken for the implementation of the digital control, which is performed by means of a standard microcontroller (Siemens 80C166). The effectiveness of the approach is assessed by experimental tests.**

***Index Terms*—Digital control, power factor preregulator.**

I. Introduction

AS COMPARED to conventional analog controllers, digital regulators offer several advantages such as the possibility of implementing nonlinear and sophisticated control algorithms, reduction of the number of control components, high reliability, low sensitivity to components' aging, negligible offsets, and thermal drifts. On the other hand, digital regulators may imply a higher development cost and a limitation in the attainable control bandwidth due to the sampling process. These drawbacks, which in the past limited their application to dc power supplies, can now be partially overcome by modern microcontrollers, featuring a very high performance level at a relatively low cost. Therefore, microcontroller applications are now feasible not only in the area of ac drives and three-phase converters, where they are indeed extremely popular, but also in the field of dc/dc converters.

For instance, digital control has been applied to dc/dc converters in [1] and [2], mainly to implement sophisticated and nonlinear control laws. This paper instead discusses the implementation of a simple and effective digital control of a boost power factor preregulator, using a standard microcontroller (Siemens 80C166). The control strategy is defined according to what is normally done in conventional analog controllers and widely discussed in literature [3], [4]. Nevertheless, by exploiting the potentialities of the digital implementation, it is possible not only to get the aforementioned general advantages, but also, more specifically, to significantly improve the system dynamics. On the other hand, the well-known drawback of the digital approach, represented by the limited bandwidth of the current control loop, is shown to produce a phase-leading current absorption from the grid which, anyway, can be fully compensated.

The first part of the paper gives a detailed explanation of the adopted control technique. In the following part, a theoretical explanation of the input-current phase displacement is provided. Finally, in the last part of the paper, all the details concerning the practical implementation with the 80C166 μC (control timing, hardware requirements, and prototype ratings) are discussed, and the results coming from laboratory tests are presented.

Manuscript received July 16, 1997; revised March 10, 1998. Recommended by Associate Editor, T. Sloane.

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Publisher Item Identifier S 0885-8993(98)06470-9.

II. Power Factor Preregulators

Fig. 1 shows the basic scheme of a boost PFP. As is known, this topology is particularly suited for average current control [3]. The PFP's current controller operates the switch so as to draw from the grid an average current whose waveform is proportional to the line voltage V_g, as implied by (1), where $g_{V_o}(t)$ is the instantaneous conductance of the converter

$$i_L(t) = g_{V_o}(t) \cdot V_g'(t). \tag{1}$$

A key point in PFP's control is that, due to the low-frequency power unbalance, the output capacitor always presents a voltage ripple at twice the line frequency. The voltage ripple, assuming unity power factor and neglecting the input inductor energy, is given by (2), where ω_f is the line angular frequency and P_o is the output power

$$|\Delta V_o(t)| = \frac{P_o}{2\omega_f C V_o} \cdot \sin(2\omega_f t). \tag{2}$$

This cannot be compensated by the voltage control loop without causing the input-current distortion, which, therefore, usually limits the achievable bandwidth to a fraction of the line frequency (10–20 Hz). Among the different possible solutions to this problem [5]–[8], this paper takes into account the output-voltage ripple notch filtering, which, thanks to the digital approach, can be easily and efficiently implemented [5].

III. Digital Control Strategy

The scheme of a boost PFP with digital control is shown in Fig. 2. The inner loop controls the average current by means of a proportional–integral (PI) regulator (K_I). The reference

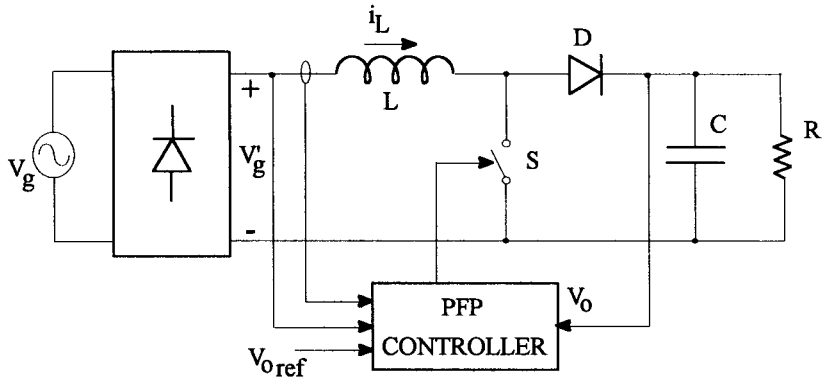


Fig. 1. Basic scheme of a boost PFP.

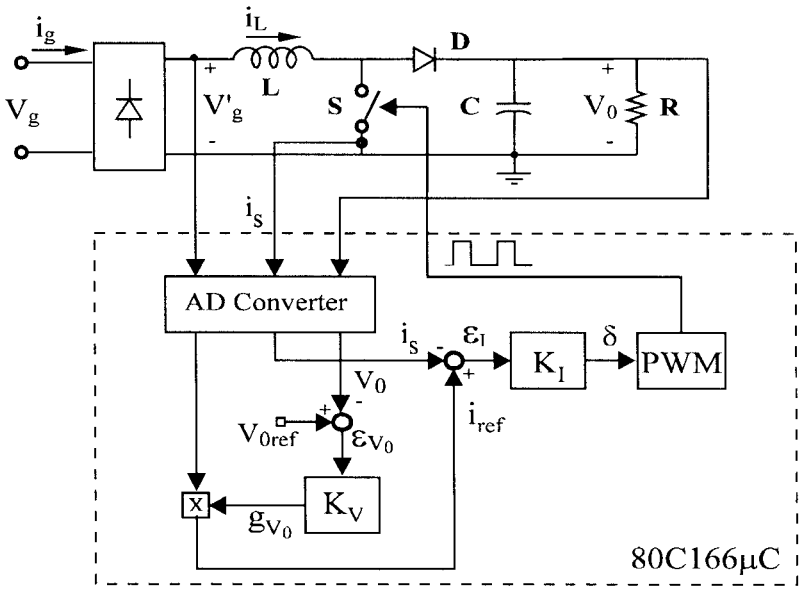


Fig. 2. Scheme of converter and digital controller.

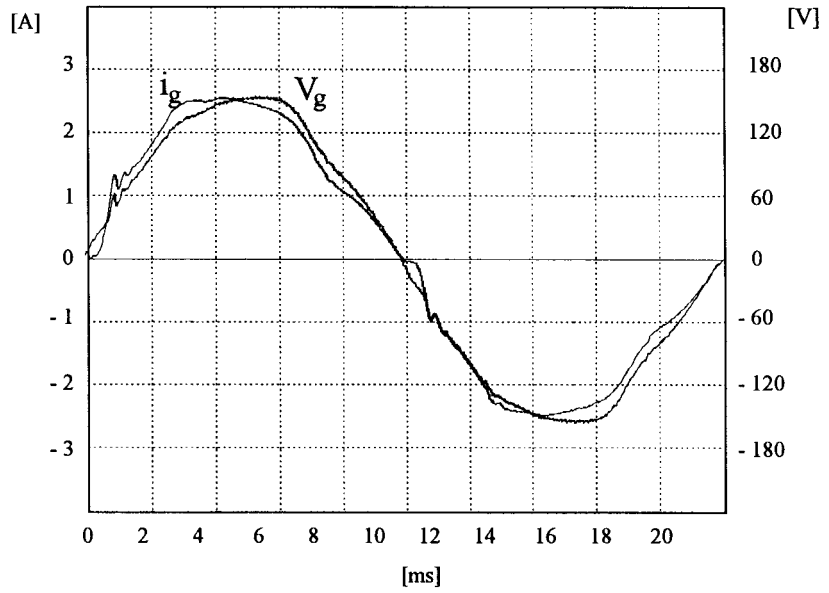


Fig. 3. Measured input current and voltage waveforms.

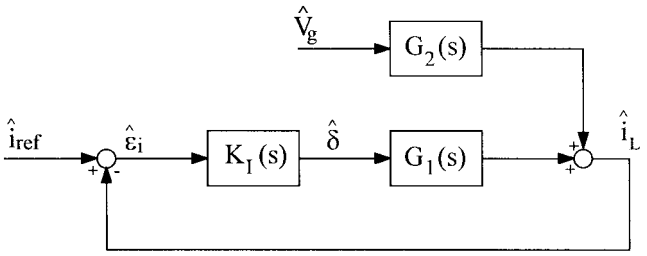


Fig. 4. Block diagram of current control loop.

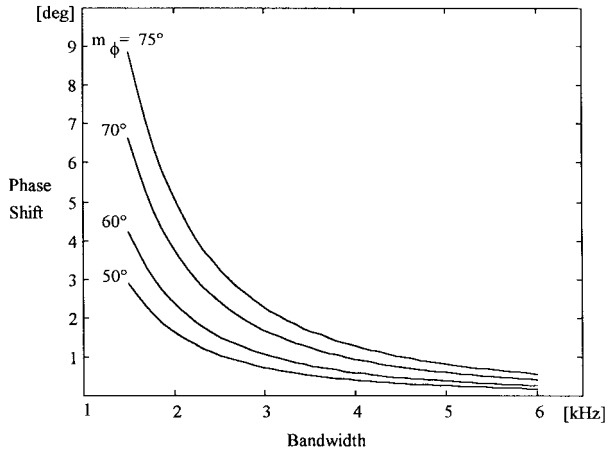


Fig. 5. Phase displacement as a function of current control-loop bandwidth and phase margin (m_ϕ).

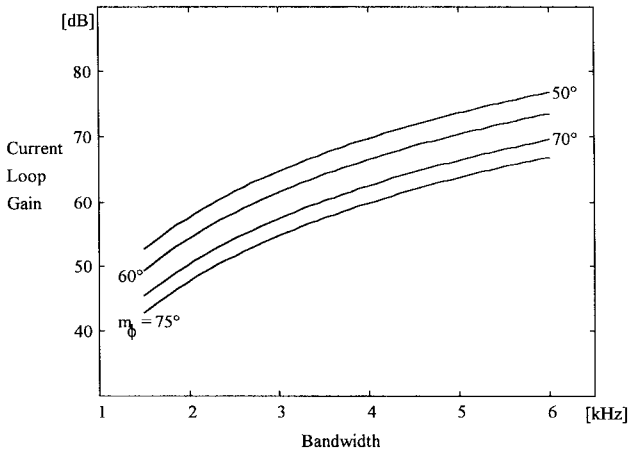


Fig. 6. Current-loop gain at $\omega = \omega_f$ as a function of current control-loop bandwidth and phase margin (m_ϕ).

for this loop is provided by multiplying the sampled input-voltage signal by the output of the voltage-loop PI regulator (K_V). The control requires the sampling of three variables: input rectified voltage (V_g'), output voltage (V_o), and average input current (i_S), which is performed by means of insulated transducers with a sampling frequency equal to the modulation frequency (20 kHz).

As far as the current loop is concerned, the required calculations, implementing a digital PI regulator with antiwindup, are performed immediately after the current sampling to minimize the delay. The regulator is designed to get a 2-kHz bandwidth, which was selected to ensure a satisfactory tracking of the current reference and, at the same time, allow the direct design in the continuous time domain. A phase margin greater

TABLE I
PARAMETERS USED IN THE COMPUTATION OF FIGS. 5 AND 6

Input Voltage	$V_g = 110V_{RMS}$
Output Voltage	$V_o = 200V$
Rated Output Power	$P_o = 200W$
Input Inductor	$L = 4.6mH$
Output Capacitor	$C = 470\mu F$

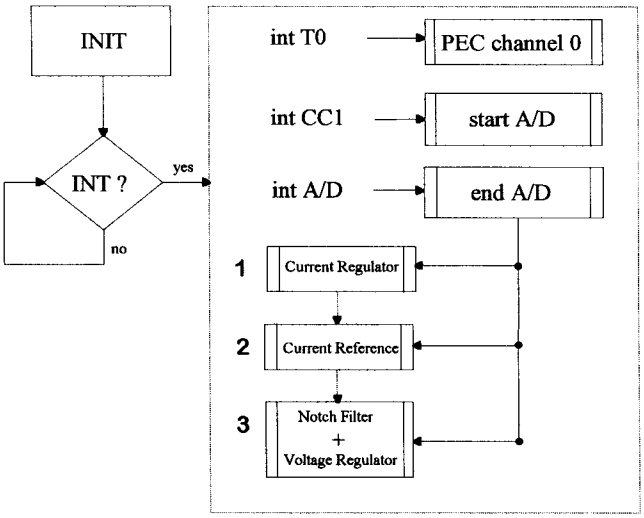


Fig. 7. Flowchart of control algorithm.

than 70°, necessary to cope with the delay introduced by the analog–digital (A/D) converter's holder, was also set. It is worth noting that a fairly high phase margin in the continuous time design of the PI regulator has to be adopted to cope with the discretization errors which are introduced mapping the regulator in the discrete time domain. The Euler's integration method, which has been used to derive the discrete time approximations of all the regulators used in this application, is negatively affected by the reduced ratio between the sampling frequency and the required bandwidth, which is equal to ten in this case, and some oversizing of the phase margin may prevent stability problems.

An important advantage of the digital approach is that the average value of the sensed current is obtained, without low-pass filters in the loop, by synchronizing sampling and modulation so that the current is always sampled in the middle of the switch on period. This allows precise regulation of the average current without introducing any delay in the loop as long as the converter operates in the continuous conduction mode (CCM). It is worth noting that when the converter enters the discontinuous conduction mode (DCM), even if the average current is no longer equal to the sensed current and the converter's dynamics change, no stability problems arise, mainly because of the very low gain of the current loop in such conditions. An effective and detailed analysis of the converter's behavior in DCM, which validates the previous

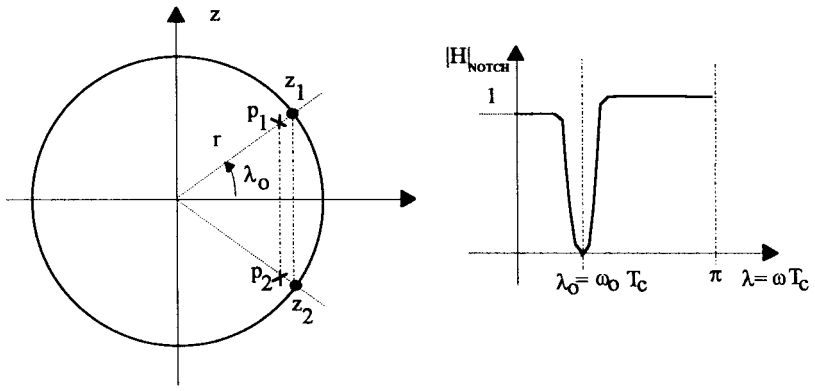


Fig. 8. Notch filter design.

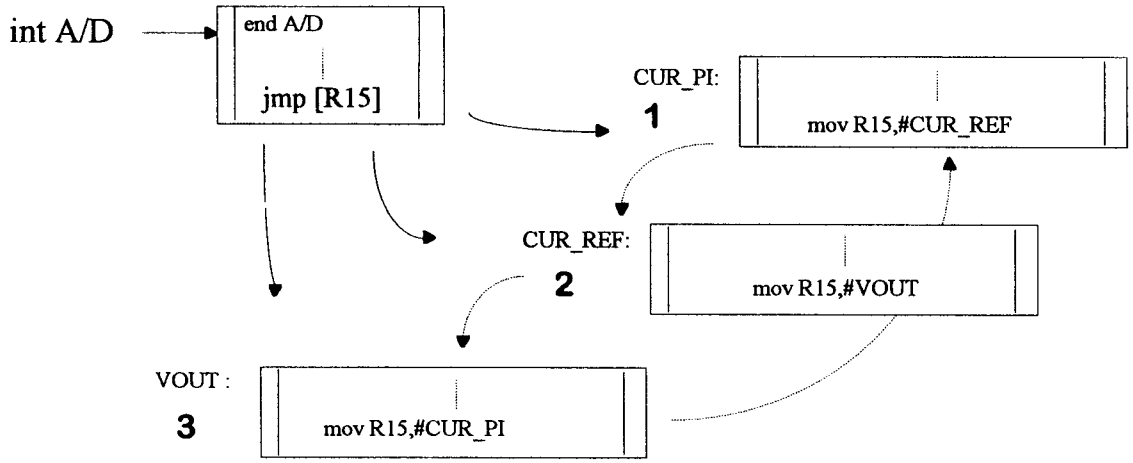


Fig. 9. Sequence of interrupt service routines.

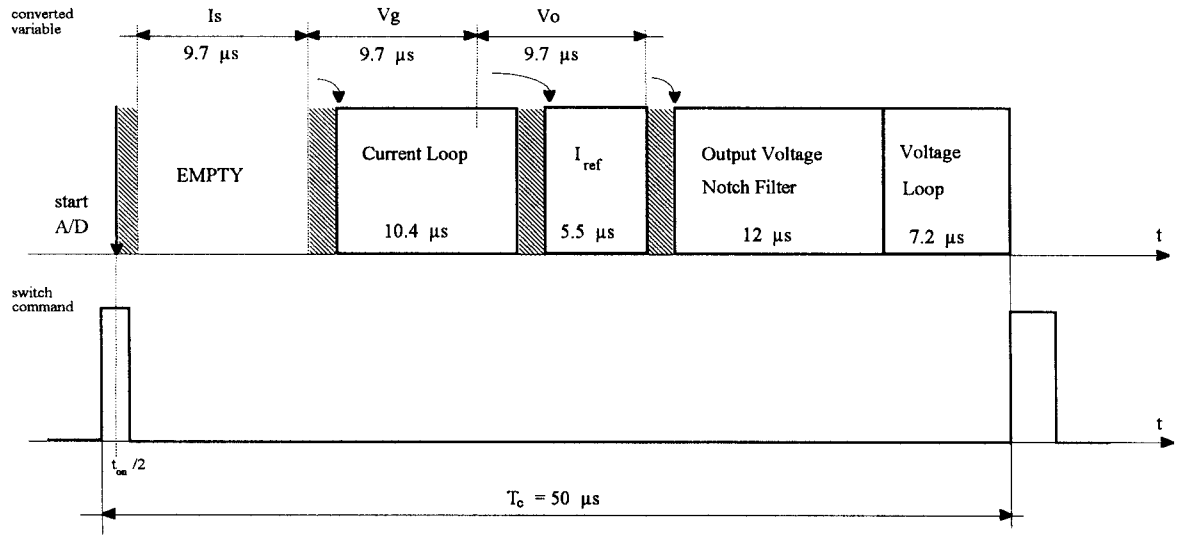


Fig. 10. Timing of the control algorithm. Shaded areas represent the dead time of interrupt service routines ($\approx$1 μs).

statement can be found in [9]. However, the input current is distorted until the converter enters the CCM again.

As shown in Fig. 2, the reference for the current loop is provided by multiplying the sampled rectified input voltage (V_g') and a scaling factor given by the output-voltage regulator (g_{Vo}). This task is accomplished by a proper routine which starts after the input-voltage conversion.

The transfer function to be compensated by the output-voltage regulator is given in [3], [4] and does not call for special design provisions since the required bandwidth (typically, around 20 Hz) is much lower than the sampling frequency. In order to increase the voltage-loop bandwidth, while limiting the input-current distortion, the application of analog notch filters to the sensed voltage has been investigated

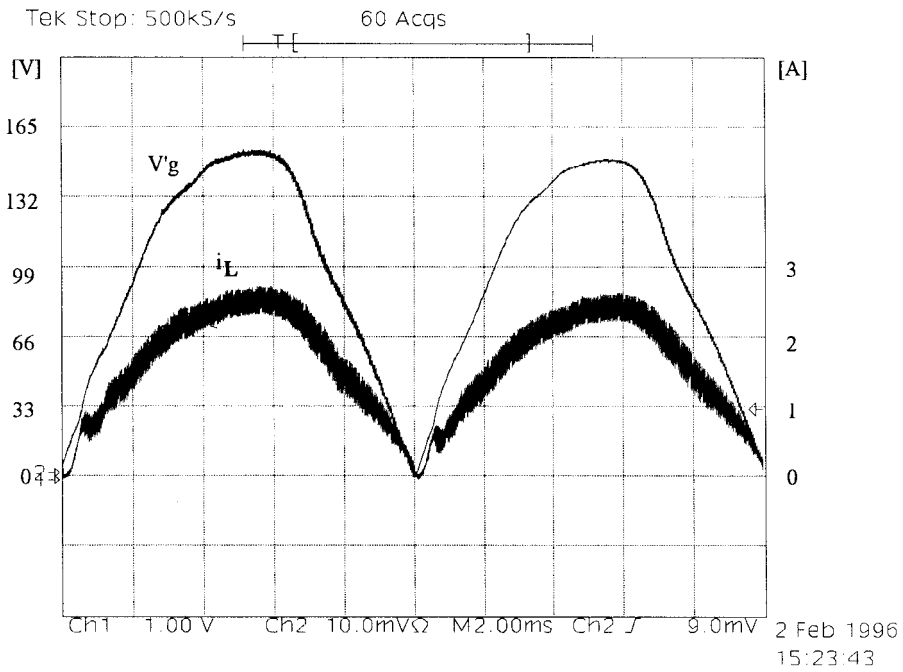


Fig. 11. Input current and voltage waveform.

TABLE II
PROTOTYPE RATINGS

Input Voltage	V_g =	110V_{RMS}
Output Voltage	V_o =	200V
Rated Output Power	P_o =	200W
Switching Frequency	f_{sw} =	20kHz
Input Inductor	L =	4.6mH
Output Capacitor	C =	470μF

TABLE III
80C166-μC BOARD FEATURES

Clock frequency	40 MHz
A/D resolution	10 bit
Bus Extension	16 bit
On board RAM	256 Kb

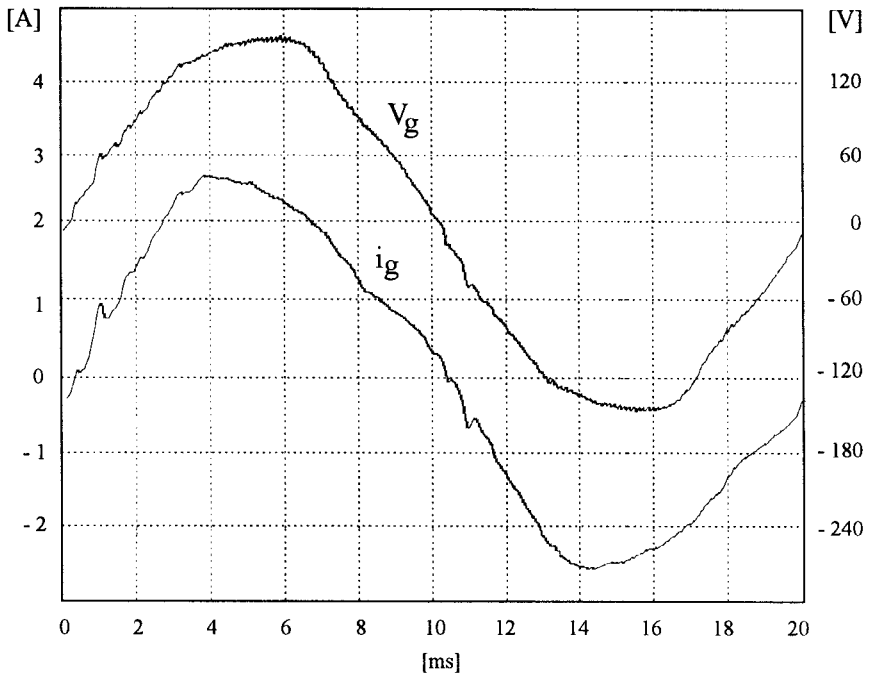
TABLE IV
CONTROL PARAMETERS (CONTINUOUS TIME DOMAIN)

Current PI gains	$K_{PI}= 2.7$
	$K_{II}= 9087$
Voltage PI gains @ 10 Hz BW	$K_{PV}= 6.15$
	$K_{IV}= 381$
Voltage PI gains @ 20 Hz BW	$K_{PV}= 12.3$
	$K_{IV}= 1289$
Voltage PI gains @ 40 Hz BW	$K_{PV}= 24.6$
	$K_{IV}= 4731$

TABLE V
TRANSDUCERS' SCALE FACTORS

Current transducer	1.1 [VA^{-1}]
Ouput voltage transducer	34
Input voltage transducer	67

[5], [6]. This solution, however, introduces undesired effects on the phase of the open-loop gain, especially when the selectivity of the filter is low (low Q factor). A high rejection of the 100-Hz frequency and a high selectivity, which would reduce the phase effects, are not easy to achieve in an analog design of the filter, mainly because of the tolerances and the variations (with time and temperature) of the required passive components' values. Digital filters instead, being insensitive to aging and tolerances, allow a strong reduction of the 100-Hz component in the feedback signal (high-Q factor) and therefore produce very small effects on the phase. Indeed, the selectivity of the digital filter is only limited by the quantization errors in its coefficients due to the fixed point architecture of the microcontroller, as it will be explained in Section V. Thus, even if a properly designed passive notch filter could theoretically achieve the same performance guaranteed by a digital solution, it would be quite difficult to practically implement it, guaranteeing the necessary reliability and effectiveness. The practical implementation of the digital solution is, instead, straightforward. In the control program, another interrupt routine, which starts after the output-voltage conversion, implements the digital notch filter and a PI regu-



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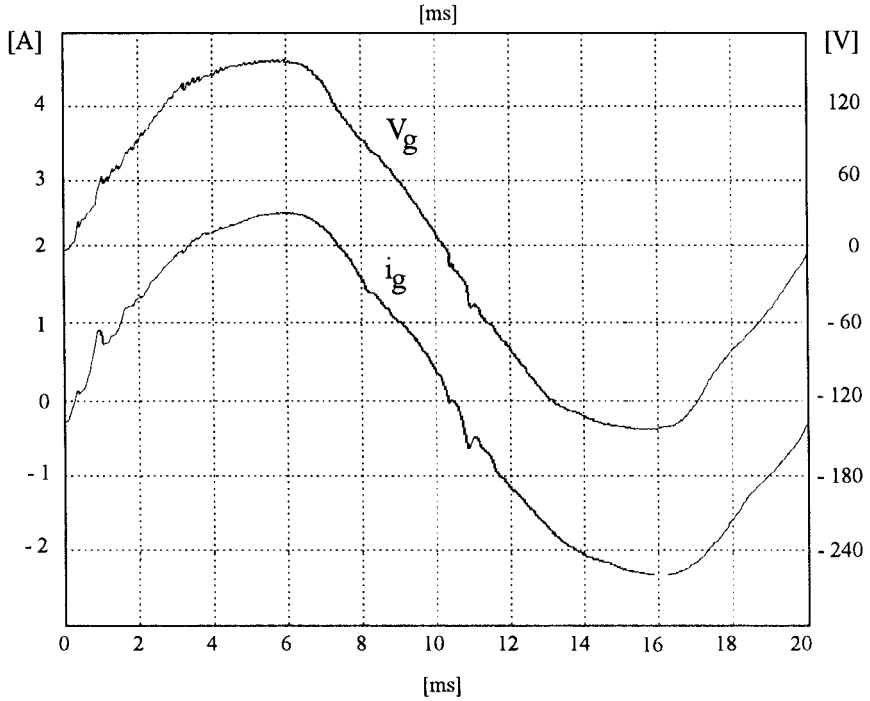


(b)

Fig. 12. Line voltage and current: (a) without and (b) with notch filter.

lator to get to a high-bandwidth voltage control with reduced input-current distortion.

IV. Input-Current Phase Displacement

Fig. 3 shows the phase displacement between the measured current and voltage on the grid. As it can be seen, the current waveform appears to be about 7° leading the voltage waveform. Such an effect can be explained considering the control block diagram shown in Fig. 4, which refers to a small-signal analysis of the current loop. The transfer functions G_1 and G_2 can be derived by state-space averaging the converter equations in CCM. They are given in (3), where, for instance, $\overline{\delta}$ represents the steady-state value of the duty cycle δ, while $\hat{\delta}$ represents its perturbed value. K_I represents the current

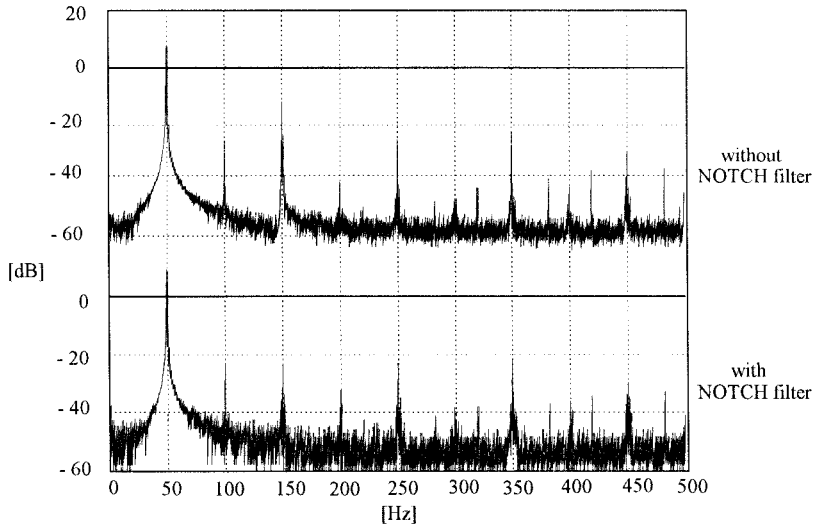


Fig. 13. Line-current spectra without (top) and with (bottom) notch filter.

controller (PI regulator)

$$G_1(s) = \frac{\hat{i}_L}{\hat{\delta}} = \frac{s\bar{V}_o C + \frac{\bar{V}_o}{R} + (1-\bar{\delta})\cdot \bar{i}_L}{s^2 LC + s\frac{L}{R} + (1-\bar{\delta})^2}$$

$$G_2(s) = \frac{\hat{i}_L}{\hat{V}_g} = \frac{sC + \frac{1}{R}}{s^2 LC + s\frac{L}{R} + (1-\bar{\delta})^2}$$

$$K_I(s) = K_{PI} + \frac{K_{II}}{s}. \tag{3}$$

By closing the loop, the transfer functions from $\hat{i}_{\text{ref}}$ to $\hat{i}_L$ (W_1), which is the current closed loop, and from $\hat{V}_g$ to $\hat{i}_L$ (W_2) can be calculated

$$W_1(s) = \frac{\hat{i}_L}{\hat{i}_{\text{ref}}} = \frac{G_1(s)\cdot K_I(s)}{1 + G_1(s)\cdot K_I(s)}$$

$$W_2(s) = \frac{\hat{i}_L}{\hat{V}_g} = \frac{G_2(s)}{1 + G_1(s)\cdot K_I(s)}. \tag{4}$$

Assuming a steady-state condition with constant average output voltage, $\hat{i}_{\text{ref}}$ can then be expressed as

$$\hat{i}_{\text{ref}} = g_{V_o}\cdot \hat{V}_g \tag{5}$$

where g_{V_o} is a constant factor depending on input-voltage steady-state level. Therefore, using (4) and (5), the complete transfer function from $\hat{v}_g$ to $\hat{i}_L$ can be found to be

$$W(s) = \frac{\hat{i}_L}{\hat{V}_g} = g_{V_o}\cdot W_1(s) + W_2(s). \tag{6}$$

Calculating the phase of $W(s)$ at $s = j\omega_f$, the expected phase displacement between input voltage and current can be found. The results of this calculation for different current-loop bandwidths and phase margins are shown in Fig. 5.

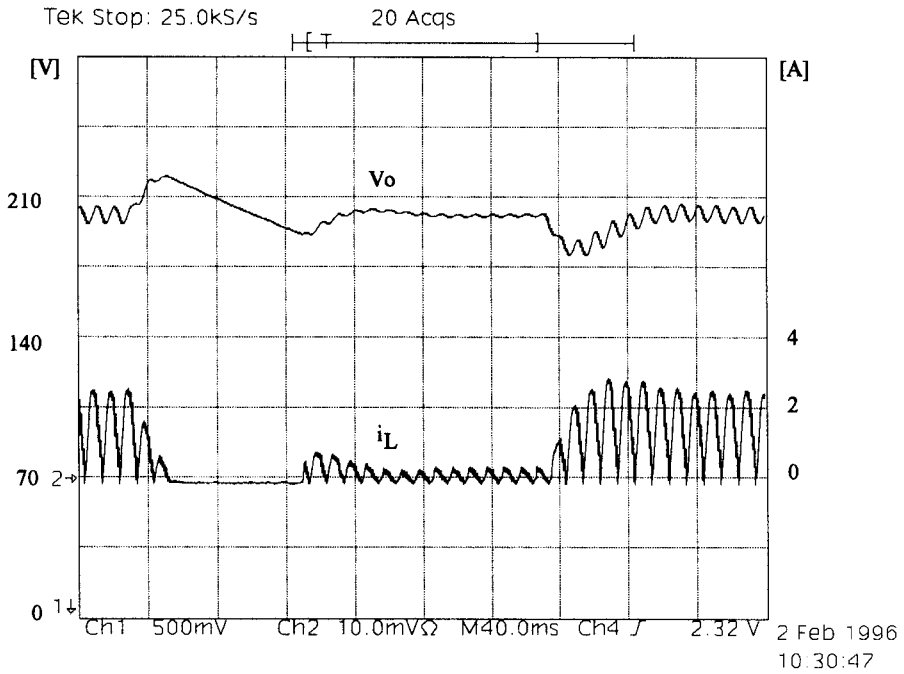
Fig. 6 instead displays the current open-loop gain $G_1(s)K_I(s)$ at the line frequency ω_f for different bandwidths and phase margins. The numerical values used for the computation of Figs. 5 and 6 are reported in Table I. The value of the steady-state duty cycle $\bar{\delta}$ has been varied from 0.1 to 0.9 noticing only minimum changes in the obtained graphics. As an example, the predicted phase shift with a 2-kHz bandwidth and a 75° phase margin for the current loop varies from 5.28° to 5.26°. The proportional (K_{PI}) and integral (K_{II}) regulator gains which define the K_I transfer function are not reported, being uniquely determined by the numerical values of the loop's phase margin and bandwidth.

As is shown by (6), the outcoming leading phase displacement between input current and voltage is totally due to the term W_2, since W_1 is practically unity at the line frequency.

The effect of W_2 is heavier when the current-loop gain is small because as it is possible to see in (3) and (4), W_2 and G_1K_I are inversely proportional to each other. As Fig. 6 shows, the bigger the phase margin or the smaller the loop bandwidth, the smaller the loop gain. Therefore, with low-current-loop bandwidths, the phase displacement tends to be higher. In standard analog implementations, this effect is normally negligible, thanks to the high-current-loop achievable bandwidth. This is no longer true for the digital implementation of the current controller because of the bandwidth limitation imposed by the sampling process. Anyway, since the phase shift is constant, once the converter power rating and controller bandwidth are defined, the practical solution to the problem is straightforward; inserting a suitable delay line between the input-voltage sampling and the elaboration of the converted data, the leading phase shift can be completely compensated, thus restoring an almost unity input power factor.

V. Digital Control Implementation

The control strategy described in Section III was practically implemented by means of the 80C166 μC. Fig. 7 represents a flowchart of the control algorithm. The program starts executing the standard initialization routines and then enters an idle mode, waiting for interrupts. There are three interrupt sources: the first (T0) is related to the pulsewidth modulation (PWM) process and calls for the duty-cycle update at the beginning of each modulation period. This has the highest priority. The second comes from the timer CC1, which is programmed to count down from a half of the duration of the switch on period. When the countdown ends an interrupt is generated and, as a result, the A/D conversion of the first control variable (switch current) is started. The third interrupt is produced when the current A/D conversion is over. The sequence of the



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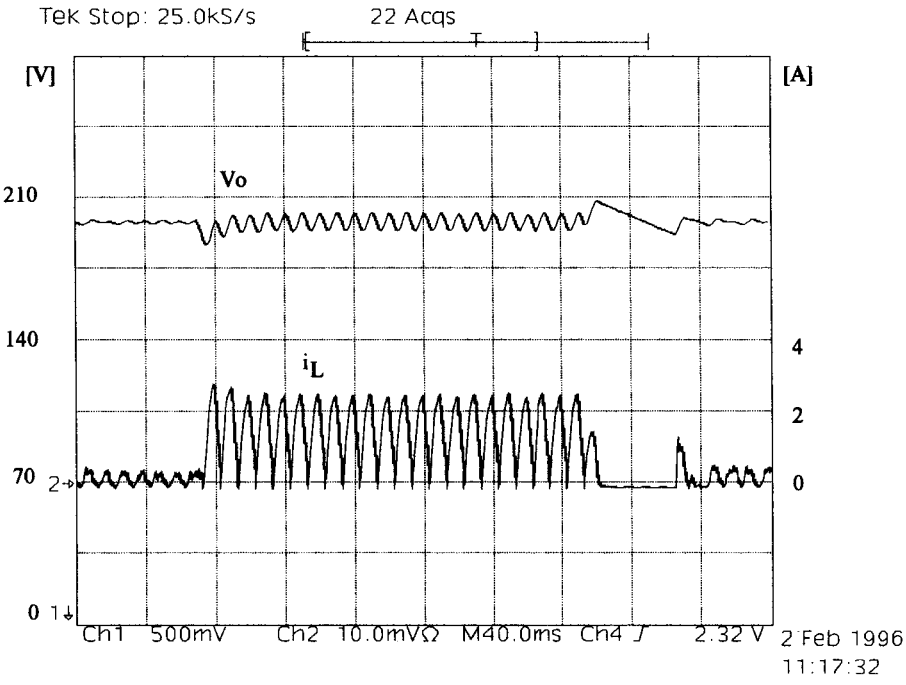

(b)

Fig. 14. Dynamic behavior of the tested PFP in the case of load step changes: (a) without and (b) with notch filter.

A/D conversions proceeds automatically: the second sampled variable is the input voltage and the last is the output voltage. At the end of each conversion, when the interrupt labeled INT A/D in Fig. 7 is generated, a proper service routine elaborates the result and programs the next conversion.

The sampling of the switch current is operated at the half of the switch on period, thus allowing to acquire the average inductor current value with no need for low-pass filters to eliminate the ripple. The routine handling the current conversion implements the PI current regulator. At its very end, this routine programs the next service routine, so that when the second conversion is over, the elaboration of the input-voltage sample can be performed. This consists of phase-shift compensation, which is done by means of a delay line and current reference calculation. Once again, at its end this routine programs the next interrupt handling so that, when the third conversion is over, all calculations regarding output voltage can be performed. These consist of a digital notch filter to eliminate the voltage ripple from the feedback signal and of a conventional PI voltage regulator.

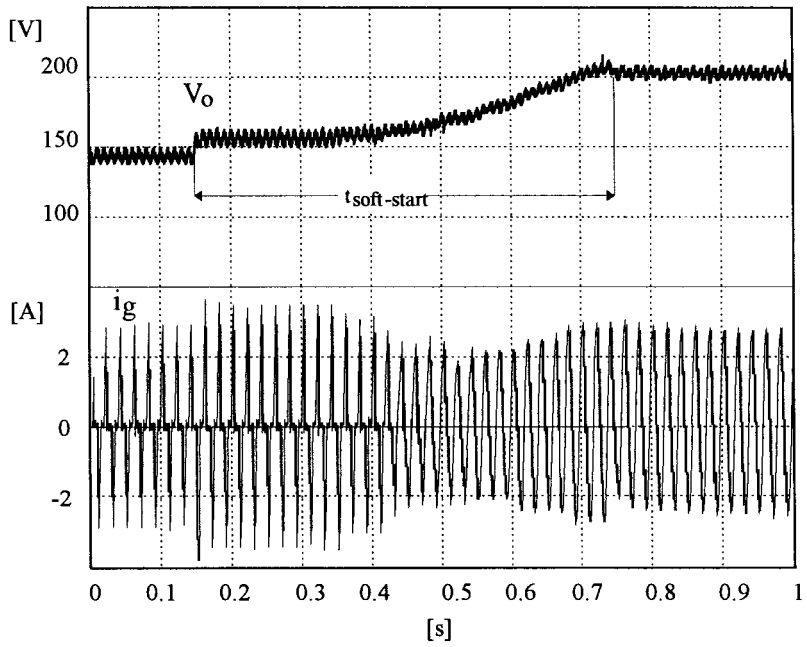

Fig. 15. Soft-start process.

The digital notch filter can be directly designed in the discrete time domain by allocating two transmission zeros and a couple of poles at the ripple frequency (λ_o), as shown in Fig. 8.

As is known, the closer the poles and the zeros, the more selective the filter and negligible the phase perturbation. Anyway, as a consequence of the fixed point architecture of the adopted μC, it was not possible to select the poles radius to be more than 0.95. The discretization in the filter coefficients would otherwise have caused filter instability. An additional low-pass filter was then needed to compensate for the unwanted high-frequency amplification introduced by the notch filter. Its consequence is a 10° phase lag at 20 Hz, which must be considered in designing the voltage regulator.

At the end, this routine programs again the interrupt service routine for the inductor current, so that a new modulation period can begin. Fig. 9 shows the explained sequence of the interrupt service routines.

A key point of this implementation is control timing. It is important to notice that the only actual constraint for the control algorithm is to be able to determine the duty cycle for the next modulation period before the end of the current one. As shown in Fig. 10, this is always possible, since it requires about 22 μs (comprising A/D conversion, dead times, and current loop). Therefore, since in the worst case, when the duty cycle is close to 100%, there is more than 25 μs available, this critical calculation always ends within the current modulation period. Of course, the other control tasks may instead end in the following modulation period; this is not a problem anyway since they operate on slowly variable signals, which are not affected by the resulting one-cycle delay in the calculations.

VI. Experimental Results

The experimental results, obtained from the digitally controlled boost PFP which has been discussed so far, are reported in this section. The ratings of the boost PFP used for the experimental tests are given by Table II. Table III describes the main features of the μC evaluation board, while the gains of the current PI regulator are listed in Table IV. The voltage PI regulator has been designed to guarantee three different loop bandwidths (10, 20, and 40 Hz). The corresponding gains are listed in Table IV too. Finally, Table V lists the current and voltage transducers' scale factors used prior to the conversion of the analog signals.

The experimental verification of the prototype operation was focused at first on testing the power factor correction's quality. As shown in Fig. 11, the input current replicates the input-voltage waveform pretty well; accordingly the measured power factor is 0.994, while the total harmonic distortion of the corresponding input voltage V_g and filtered current i_g are 3.8% and 6.2%, respectively.

Fig. 12 shows the effect of the digital notch filter applied to the output-voltage feedback signal. It is possible to note that the current distortion is strongly reduced by the filter. The designed bandwidth for the output-voltage control loop is 20 Hz both in the case of Figs. 11 and 12. Moreover, as for any of the performed tests, the compensation of input-current phase lead is active. As it can be seen, the digital notch filter effectively reduces the current distortion for a given bandwidth. To further illustrate this effect, Fig. 13 shows the measured line-current spectra.

It is possible to notice the evident reduction of the third harmonic component of the spectrum, which accounts for the measured total harmonic distortion (THD) reduction from above 10% to about 6%.

Inversely, it is also possible, given a certain THD acceptable level, to push the voltage-loop bandwidth far beyond the achievable limit with no filter. As a consequence of the voltage-loop bandwidth's increase, it is possible improve the dynamic performance of the PFP. As a comparison, Fig. 14

shows the behavior of the converter in case of a load step change from full to minimum load (200 $\Omega \rightarrow 1500\ \Omega$) and back. The designed voltage-loop bandwidths are 10 and 40 Hz, respectively, so as to ensure a similar current harmonic distortion without and with notch filter. The difference in the dynamic responses is pretty evident. The settling time at load reconnection, for instance, passes from about 80 to about 20 ms. It is worth noting that this comparison implicitly testifies a significant superiority of the proposed solution also to the conventional analog ones, which do not employ notch filters and which, therefore, exhibit a reduced voltage-loop bandwidth, typically well below 20 Hz. As a consequence, the dynamic response of such systems is fairly similar to the one exhibited by the proposed solution when the notch filter is not employed and the voltage-loop bandwidth, in order to maintain the input-current distortion at acceptable levels, is limited to 10 Hz.

Finally, Fig. 15 shows the behavior of the tested prototype at startup. A soft-start procedure was implemented to gradually raise the output capacitor voltage from its precharged level ($\approx$150 V) to its final level of 200 V. This was done by slowly increasing the saturation level of the output-voltage PI regulator, thus limiting the current surge. The duration of the whole process $(t_{\text{soft start}})$ is about 0.6 s.

VII. Conclusion

This paper presents the implementation and test of a fully digital control for a boost PFP. The implementation is done by using the 80C166 microcontroller. The paper shows how the higher development cost of the digital implementation is compensated by a significant improvement of the dynamic performance achievable by the converter. The digital approach, in fact, can be effectively exploited in implementing simple compensations for each of the unwanted effects deriving from the limited current and voltage-loop bandwidths, which, instead, may be rather complicated in analog implementations.

In particular, this paper discusses the phase-leading current absorption from the grid which is due to the current-loop limited bandwidth, providing a simple theoretical explanation of it.

Finally, the results of the experimental tests assessing control performance are presented and discussed.

Acknowledgment

The authors are very grateful to Dr. R. Veronese for his decisive help in the experimental activity.

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