Design and Fully Digital Control of Parallel Active Filters for Thyristor Rectifiers to Comply with IEC-1000-3-2 Standards

Simone Buso, *Member, IEEE*, Luigi Malesani, *Fellow, IEEE*, Paolo Mattavelli, *Associate Member, IEEE*, and Roberto Veronese

***Abstract*—This paper presents the implementation of a digitally controlled parallel active filter for a thyristor rectifier with inductive load. Using a state-of-the-art digital signal processor (DSP) platform (ADSP21020 and ADMC200), a fully digital control of the system, based on the dead-beat control of inverter currents and space vector modulation, is implemented. The intrinsic calculation delay of the dead-beat algorithm is shown to represent a serious hurdle for the achievement of a satisfactory compensation quality. In particular, meeting the IEC 1000-3-2 standards for class A equipment appears to be quite difficult, especially in the high-frequency range. This paper investigates the effects of the input passive filters and power converter design on the system's performance and describes the implementation of the digital control by means of the specified hardware. Experimental results are finally given to evaluate the achieved performance.**

***Index Terms*—Active filters, harmonic standards, VSI current control.**

I. Introduction

HARMONIC and reactive power compensation of thyristor rectifiers represents a challenging problem, especially when IEC standards for class A equipment (IEC 1000-3-2) have to be met. The use of parallel active filters allows the compensation of low-order harmonics [1]–[3], while the fulfillment of the specified standards, especially in the high-frequency range, is very difficult to achieve, even if a very fast current loop is implemented [4]–[6].

This paper presents the implementation of a compensation system, featuring a digitally controlled active filter, intended for the application to existing and particularly critical power supplies (retrofit). The proposed digital implementation is based on the ADSP21020 digital signal processor (DSP) and the ADMC200 motion control board. To get the required speed of response, a dead-beat control algorithm is implemented, which, as is known, guarantees the best possible dynamic performances among the fully digital solutions [7]–[9]. Indeed, provided that the power converter, used as the active filter, is correctly designed, the dead-beat control can replicate the reference current with only a two-cycle delay error. Thanks to the speed of the adopted DSP board, it is possible to implement the control of inverter currents and the space vector modulation routine necessary for inverter operation in a small fraction of the modulation period. Therefore, our power converter can be driven at the maximum switching frequency allowed by insulated gate bipolar transistor (IGBT) components. Nevertheless, due to the inherent delay of the dead-beat control algorithm, this is not enough to meet the aforementioned standards. To fulfill the harmonic limits, a significant oversizing of the input passive filter is needed. Besides, it is advisable to adopt all possible control refinements, such as those proposed in [9]. Different current control techniques [5], [6] for the active filter, of course, may allow one to meet the considered standards more easily. This paper discusses some design issues, mainly regarding the system's passive filters, and considers their effect on the control's stability and performance. Then, attention is focused on the hardware platform employed here, and all the provisions, which have been taken to fit its standard structure to the control of the power converter, are described.

Finally, experimental results from a laboratory prototype are presented to describe the performance of the implemented system.

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S. Buso and R. Veronese are with the Department of Electronics and Informatics, University of Padova, 35131 Padova, Italy (e-mail: simone@tania.dei.unipd.it).

L. Malesani and P. Mattavelli are with the Department of Electrical Engineering, University of Padova, 35131 Padova, Italy (e-mail: pmatta@tania.dei.unipd.it).

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II. Basic Scheme of the System

The basic scheme of the active filter application discussed in this paper is shown in Fig. 1. A three-phase thyristor rectifier supplying an inductive load is considered. The harmonic content and reactive power absorption of this system are reduced by a parallel active filter, implemented by using a three-phase voltage-source IGBT inverter. The passive elements (L_1, C_1) required for filtering the harmonic components at the modulation frequency and the residual compensation errors are also shown, together with inductor (L_2), which limits the current slope during thyristor commutations. In L_1, the line impedance is also included. Branch (R_2, C_2) shown in Fig. 1 indicates one of the possible configurations to smooth filter resonance. In fact, as in this case, it can be substituted by active damping obtained by a proper control of the active filter [12], [13], since oscillation frequency falls within the active filter bandwidth.

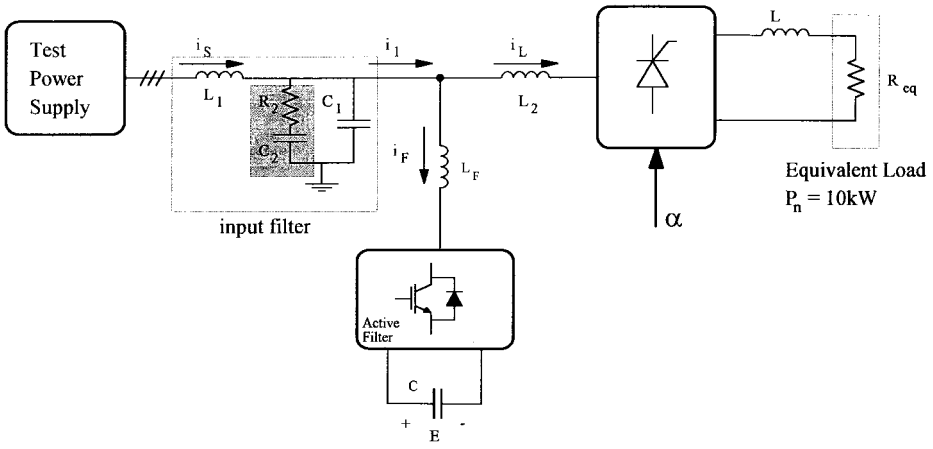


Fig. 1. Basic scheme of the system with the parallel active filter.

Finally, it is worth noting that the considered voltage source is a specific test power supply; as required by IEC standards, it provides a sufficiently low impedance along the frequency range of interest.

III. Control Technique

In the compensation system of Fig. 1, the control of the active filter's current is performed by means of the dead-beat control technique [7]–[9]. As is well known, in a dead-beat controller, the control algorithm calculates the phase voltage, so as to make the phase current reach its reference by the end of the following modulation period [10], [11]. Here, the calculations are performed in the α, β frame, and the space vector modulation (SVM) strategy, which suits the digital implementation very well, is applied to the switching converter. This is essentially the situation depicted in Fig. 2. An important advantage of the dead-beat technique is that it does not require the line voltage measurement in order to generate the current reference. The dead-beat control's algorithm, in fact, allows an estimation of the line voltage instantaneous value, which can, therefore, be used also for the current reference generation. On the other hand, the inherent delay due to the calculation time is, indeed, a serious drawback in active filter applications. In particular, when compensating for thyristor rectifier loads, it produces appreciable errors in correspondence of thyristor commutations. Thus, additional provisions to get to a satisfactory performance level are required. In the more recent versions [9] of the dead-beat controller, the delay may be reduced by sampling the control variables and executing the control routines twice in a modulation period. The turn-on and turnoff times of the power converter switches may be decided separately in two successive control periods. As a consequence, the aforementioned delay in current reference tracking can be reduced to a single modulation period. Due to limitations in the adopted modulator, this technique has not been used in the implementation discussed in this paper.

In any case, the residual compensation errors can be reduced by a suitable value of limiting inductor L_2 and a proper sizing of the input passive filter.

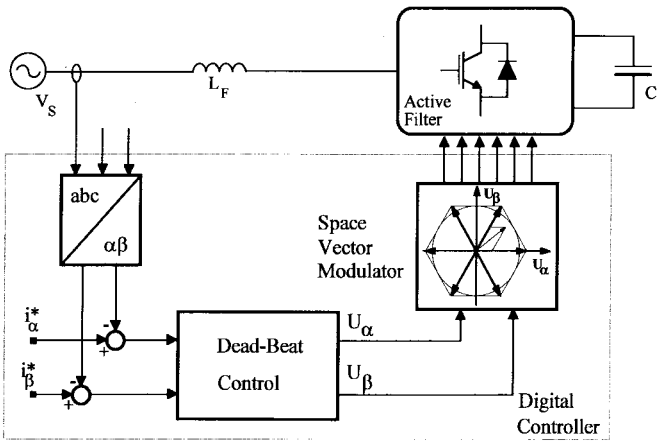


Fig. 2. Basic scheme of the digital dead-beat current regulator.

IV. Input Filter Effects

A. Control Problems

Deadbeat control of three-phase inverters has been widely investigated by many researchers in recent years [7]–[11], especially for drive applications. The application of this control technique to active filters is almost straightforward; however, the effect of the input filters, commonly used to eliminate high-frequency harmonic components due to the inverter's modulation, must be carefully considered. These filters, in fact, are not normally accounted for in the control algorithm, which refers to an "ideal" load model, where only inverter inductances L_F are taken into account, as shown in Fig. 3. Therefore, the dynamic behavior of the current loop changes and may bring the overall system to instability. Similar problems arise also when there is a parameter mismatch between the modeled inverter inductance and the actual one [9].

In order to analyze the overall closed-loop system, Fig. 1 can be represented as shown in Fig. 3, where the load can be assumed to be a current generator. Stability analysis is performed using the discrete-time equations of the real system and using a deadbeat control, based on a first-order model, given by a modeled inductance L_{Fm} and u_s.

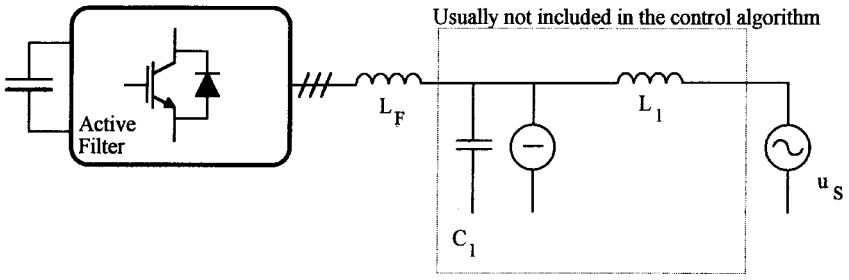


Fig. 3. Simplified representation of Fig. 1.

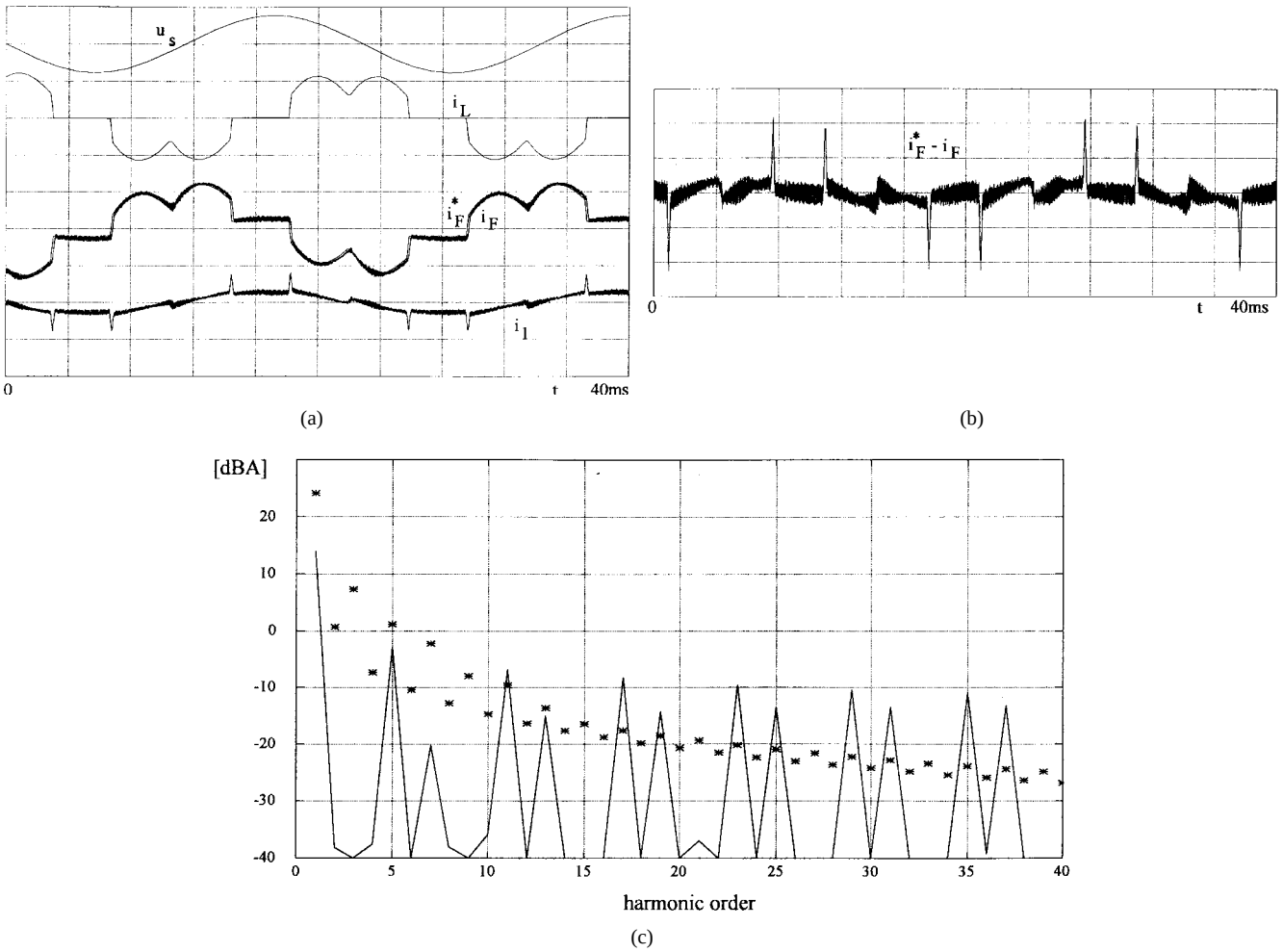


Fig. 4. (a) Simulated active filter behavior with $L_1 = 0$ and $L_2 = 0.06$ pu: u_s (400 V/div), i_L, i_1, i_F, i_F^* (20 A/div). (b) Residual line current with $L_1 = 0$ and $L_2 = 0.06$ pu: (5 A/div). (c) Spectrum of line current i_1 with $L_1 = 0$ and $L_2 = 0.06$ pu—Symbols "*" represent IEC 1000-3-2 harmonic limits for class A equipment.

Details of this analysis will be reported in a future paper. We have eventually seen that, especially when the grid voltage is estimated and used to derive the line current reference waveform, instabilities easily occur if the ideal model is not adequate (i.e., nonnegligible dynamic effects of L_1 and C_1) or there are parameter mismatches (i.e., L_F different from $L_{\rm Fm}$). Some oversizing of the filter capacitor is recommended in order to avoid oscillatory response in the current loop, which would otherwise deteriorate the effectiveness of the active filter. Further work is currently in progress to improve system performance.

B. Design Issues

In order to get some indication of the filtering action required by the input filter, the effect of limiting inductor L_1 alone is considered first. Fig. 4(a) and (b) shows the achievable performance when no significant filters ($L_1 = 0, L_2 = 0.06$ pu) are used and the thyristor firing angle α is set to 75°. Although the active filter is able to replicate its reference with a two-modulation period delay (100 μs), the current error exhibits a harmonic content which is beyond the standard limitations, especially for the high-order harmonics, as shown in the line current spectrum of Fig. 4(c). Thus, unless

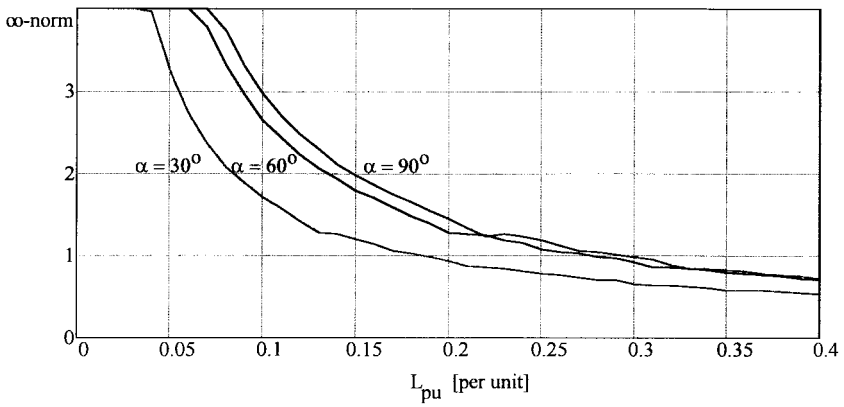


Fig. 5. ∞ norm of the ratio between line current harmonics and harmonic limits imposed by standards, as a function of inductive passive filter L_{pu}.

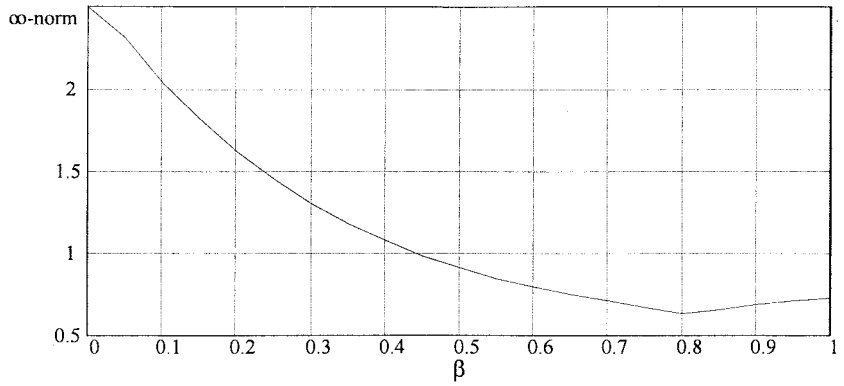


Fig. 6. ∞ norm of the ratio between line current harmonics and the harmonic limits imposed by standards, as a function of parameter β.

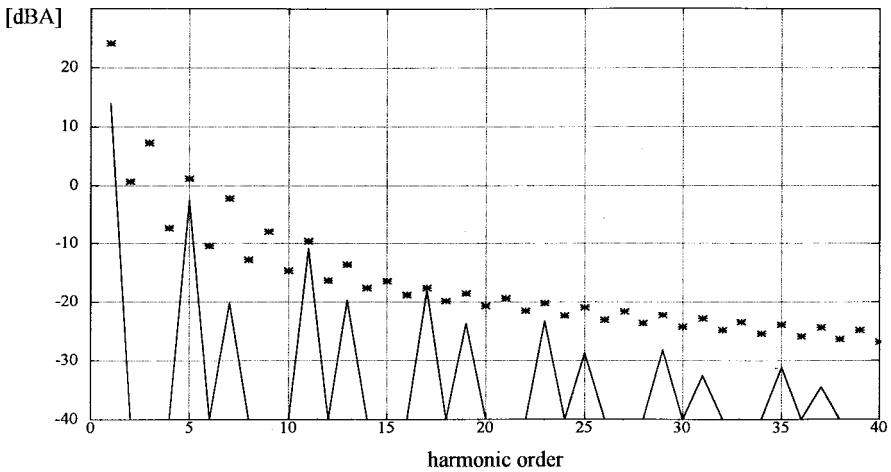


Fig. 7. Spectrum of line current i_S with $L_1 = 0.05$ pu, $L_2 = 0.06$ pu, and $C_1 = 0.15$ pu—Symbols "*" represent IEC 1000-3-2 harmonic limits for class A.

passive filter L_2 is extremely large, the use of an active filter alone, even if properly designed, is not enough to meet the IEC 1000-3-2 standard requirements. This may not be true for loads with a higher power level, which should comply with IEEE-519 recommended practices. We found, in fact, such standard to be less demanding. Moreover, the compensation of diode rectifiers is also less problematic, due to the slower di/dt exhibited by the load current.

When input filter (L_1, C_1) is added, preliminary design criteria can be derived as follows. Filter L_2 limits the di/dt during thyristor commutation, so as to reduce the residual errors due to the control delay and to avoid inverter saturation; series inductance L_1 and capacitor C_1 provide the required filtering action, especially in the high-frequency range. In order to avoid or to limit inverter saturation, basic design guidelines for inductors L_2 and L_F can be found in [2]. However, IEC 1000-3-2 compliance cannot be achieved, with a dead-beat current control strategy simply by limiting or eliminating the occurrence of inverter saturation. This is mainly due to the intrinsic delay of the digital dead-beat control, which

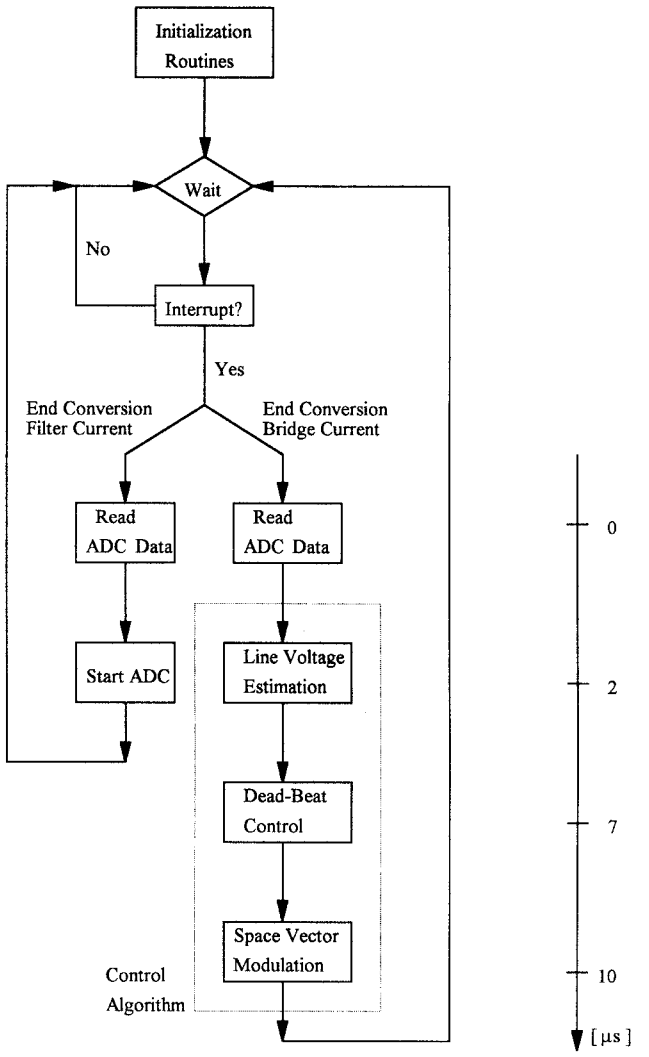


Fig. 8. Flow chart of control algorithm.

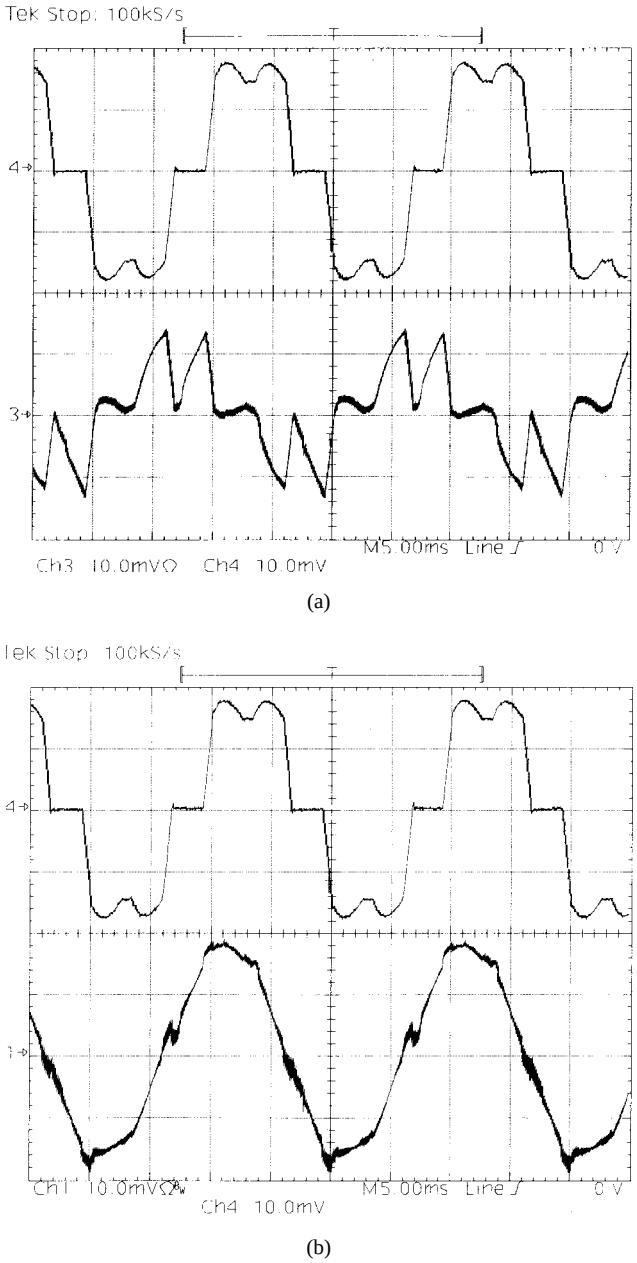


Fig. 9. (a) Bridge (top) and active filter (bottom) current (10 A/div, 5 ms/div). (b) Bridge (top) and line (bottom) current (10 A/div, 5 ms/div).

represents the main issue of the system analysis performed in this paper. Thus, in the following, a design procedure considering the additional constraint of the IEC standard and the peculiarities of the dead-beat control is given.

In order to quantify the design procedure, the residual current has been derived in a simplified way, assuming that the active filter replicates the reference current with a two-cycle delay, unless inverter saturation occurs. In order to quantify the "distance" of the considered setup from the limit imposed by standards, the ∞ norm of the ratio between the line current harmonics and limits imposed by IEC 1000-3-2 has been evaluated. Values lower than one mean standard fulfillment. This parameter has been considered, instead of the typical total harmonic distortion (THD), since this does not give any indication with respect to the standards, which impose specific limits for each harmonic up to 2 kHz.

The above calculation has been first used to determine the size of L_2 required to fulfil IEC 1000-3-2, when acting alone. Fig. 5 shows the aforementioned ∞ norm as a function of the inductive passive filter L_2 ($L_2 = L_{\rm pu}$), with a firing angle set to 30°, 60°, and 90° (worst case) and with peak-to-peak current ripple on the dc side set to 40% of the dc value. Note that a value $L_2 = 0.30$ pu is needed in order to meet the standard requirements in the worst case condition. This is due to the low harmonic level imposed by the standards (57 mA for the thirty-ninth harmonics, in spite of a fundamental up to 16 A).

Great reduction in the L_2 value can be achieved when the filter (L_1, C_1) is considered. Also, by increasing filter capacitor C_1, both L_1 and L_2 can be reduced while meeting the standard requirement. Without going into the details of an optimal design procedure for such filters, which is beyond the scope of this paper, we directly show a possible solution, which ensures large stability margin. If we consider $C_1 = 0.15$ pu and $L_{\rm tot} = L_1 + L_2 = 0.11$ pu, Fig. 6 shows the aforementioned ∞ norm as a function of a linear partition factor between $L_1 (= \beta * L_{\rm tot})$ and $L_2 (= (1 - \beta) * L_{\rm tot})$, putting

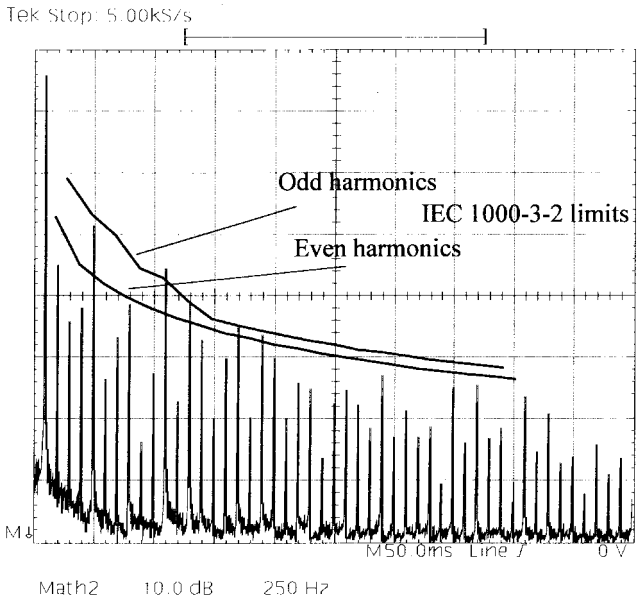


Fig. 10. Line current spectrum (10 dBA/div, 250 Hz/div).

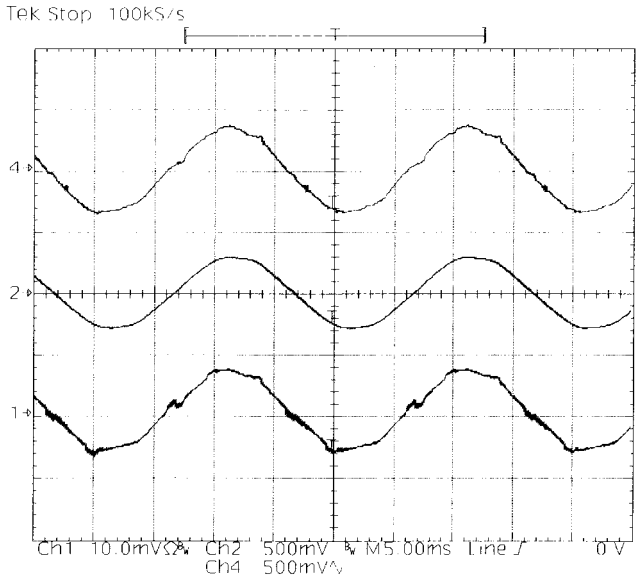
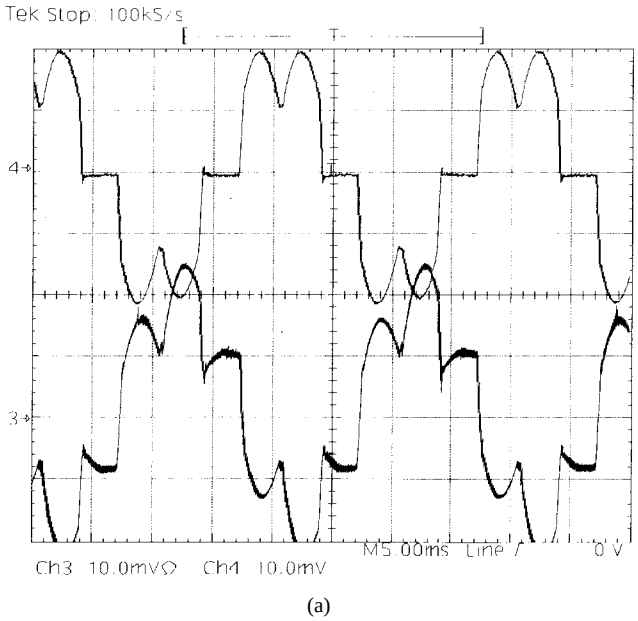


Fig. 11. From top to bottom: estimated line voltage (500 mV/div, 5 ms/div); measured line voltage (500 V/div, 5 ms/div); line current (25 A/div, 5 ms/div).

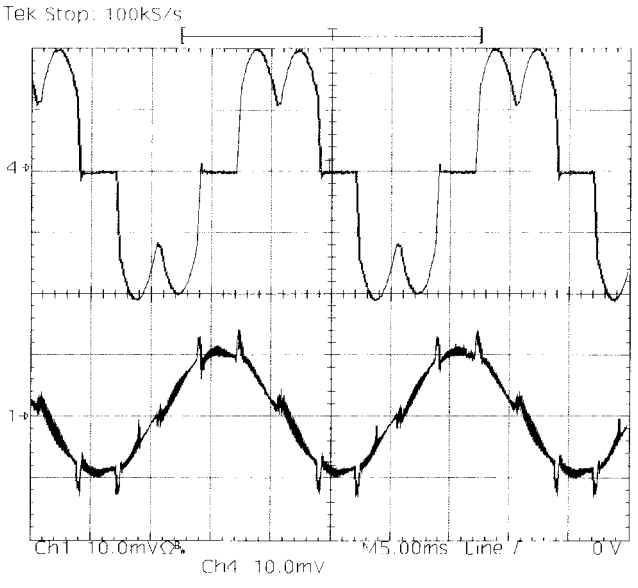
TABLE I
PROTOTYPE RATINGS

Line to Neutral Voltage (RMS)	220 V
Bridge Output Power	10 kW
DC Link Voltage	750 V
Active Filter Inductance	1.2 mH (0.027pu)
Bridge inductance	2.6 mH (0.06pu)
Switching Frequency	20 kHz

into evidence that values of β above 0.44 allow standard fulfilment. The same simulation of Fig. 4 has been run under these conditions, and the line current spectrum, depicted in Fig. 7, is now within standard limitations. Similar values have been chosen for the experimental setup.



(a)



(b)

Fig. 12. (a) Bridge (top) and active filter (bottom) current (10 A/div, 5 ms/div). (b) Bridge (top) and line (bottom) current (10 A/div, 5 ms/div).

V. CONTROL IMPLEMENTATION

The dead-beat control strategy which was previously described has been practically implemented by means of a floating-point DSP (ADSP21020). This DSP unit represents a powerful tool for digital control implementations due to the fast arithmetic unit (40-ns cycle) and its floating-point architecture (32/40 b). The interface between the processor and the power converter has been implemented exploiting the ADMC200 motion control board. This includes all the necessary facilities for implementing a current control loop in a three-phase voltage-source inverter, from the pulsewidth modulation (PWM) modulator to the A/D converter. Unfortunately, being specifically designed for drive applications, it lacks some useful features for more complicated applications, such as an

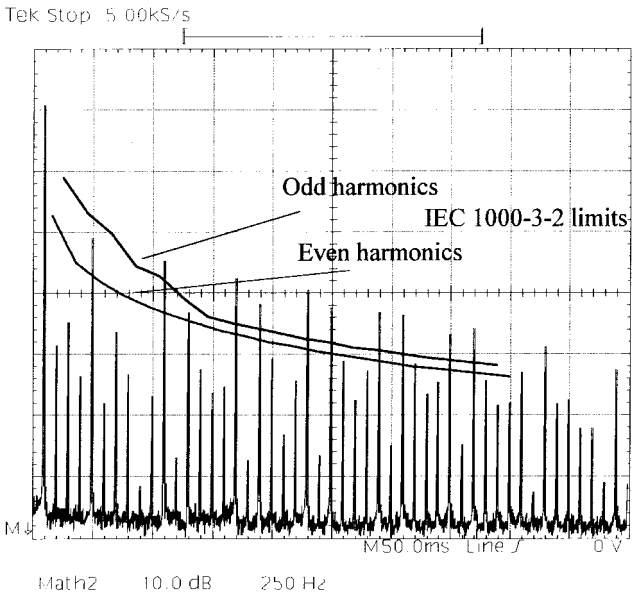


Fig. 13. Line current spectrum (10 dBA/div, 250 Hz/div).

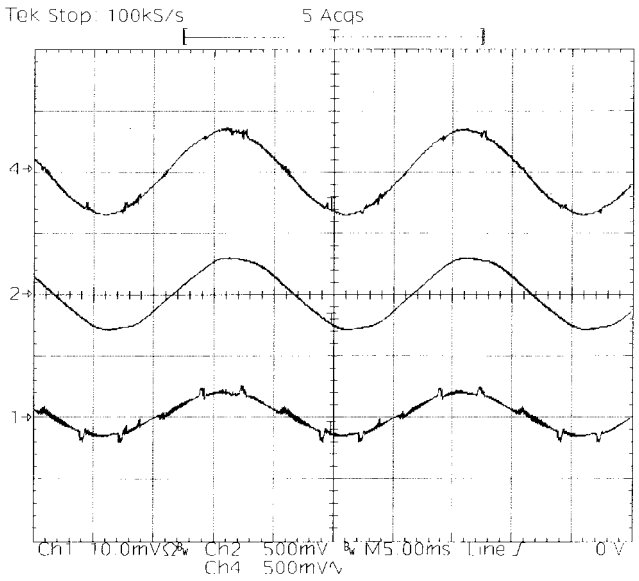
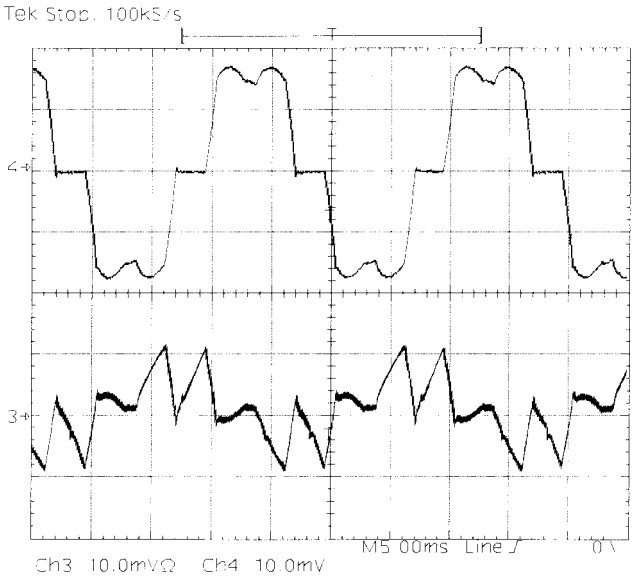
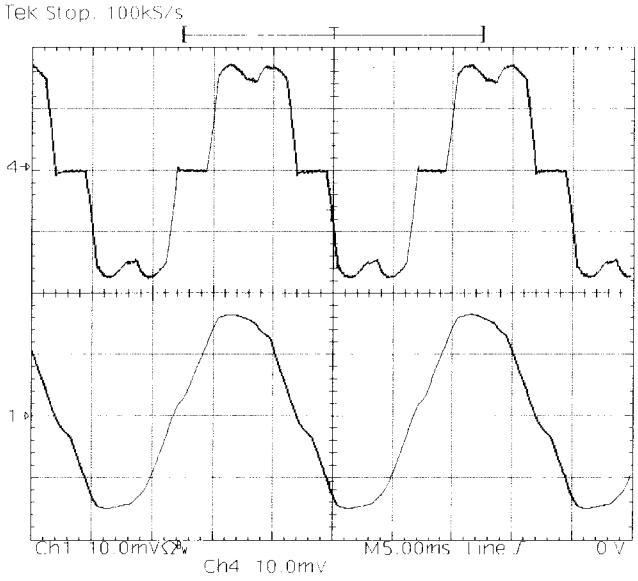


Fig. 14. From top to bottom: estimated line voltage (500 mV/div, 5 ms/div); measured line voltage (500 V/div, 5 ms/div); line current (25 A/div, 5 ms/div).



(a)



(b)

Fig. 15. (a) Bridge (top) and active filter (bottom) current (10 A/div, 5 ms/div). (b) Bridge (top) and line (bottom) current (10 A/div, 5 ms/div).

input multiplexer for the A/D converter or a more flexible PWM modulator, allowing, for instance, separate calculation of turn-on and turnoff times for the power switches. The input multiplexer has been externally implemented, so as to allow the sampling both of the rectifier's and of the active filter's current.

The flow chart of the implemented algorithm is represented in Fig. 8. The program starts initializing the ADMC200 board. Then, the PWM modulator is started. The beginning of the modulation process automatically triggers the active filter currents' A/D conversion. When this is over, after about 4 μs, an interrupt is generated for the DSP. The corresponding service routine stores the converted data in memory and triggers the bridge's currents' conversion.

The next interrupt is again generated after 4 μs and is served by a different routine. This one performs all the required control functions, from the line voltage estimation and the dead-beat control of the active filter currents to the space vector modulation of the power converter. As can be seen, the control routines require, on the whole, about 10 μs.

VI. Experimental Results

The system of Fig. 1 has been experimentally tested to evaluate the control performance. The ratings of the laboratory prototype are given in Table I.

The first considered operating condition is characterized by a small thyristor bridge firing angle $(25^\circ \div 30^\circ)$, with $L_1 = 0$ and $L_2 = 2.6$ mH $= 0.06$ pu. Fig. 9(a) shows the thyristor

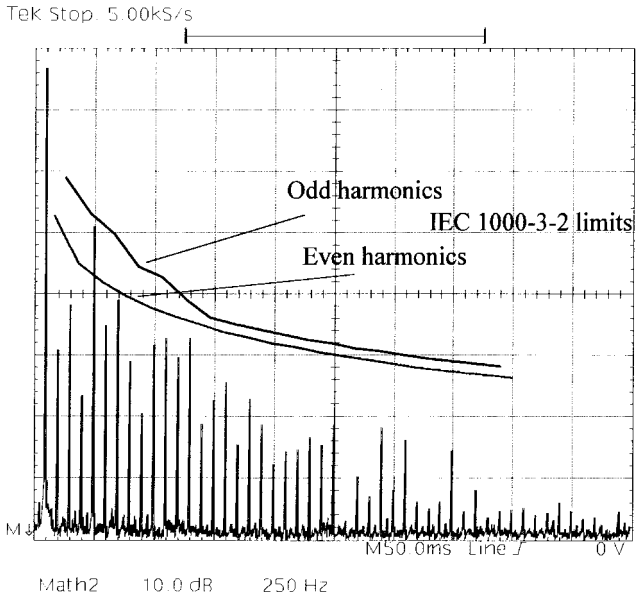


Fig. 16. Line current spectrum (10 dBA/div, 250 Hz/div).

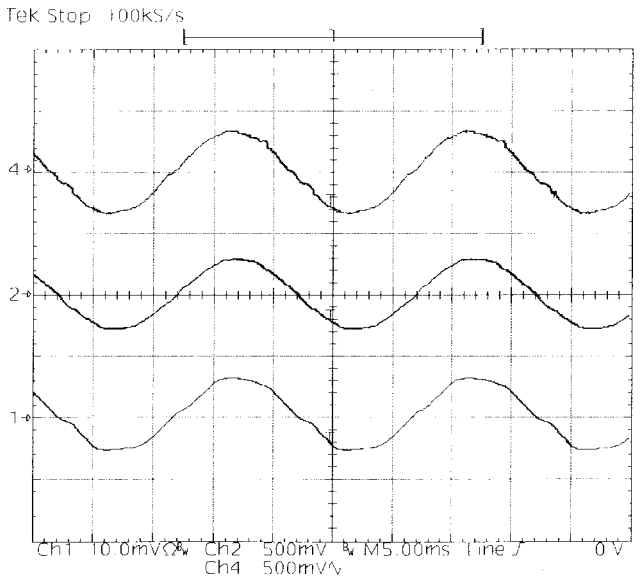
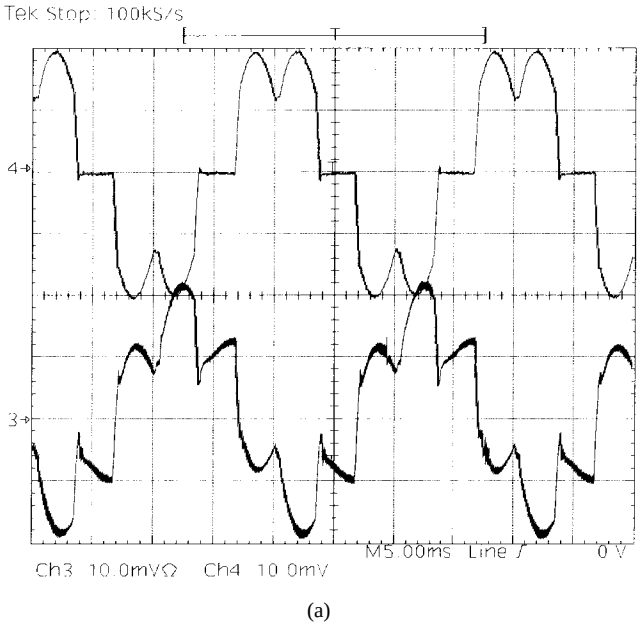
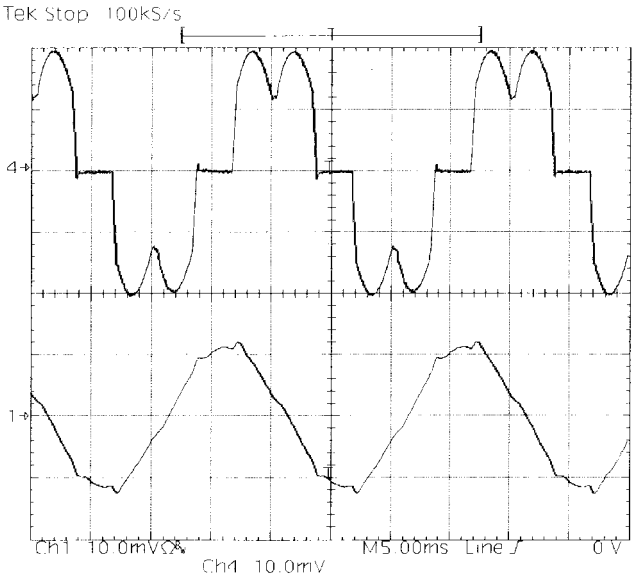


Fig. 17. From top to bottom: estimated line voltage (500 mV/div, 5 ms/div); measured line voltage (500 V/div, 5 ms/div); line current (25 A/div, 5 ms/div).



(a)



(b)

Fig. 18. (a) Bridge (top) and active filter (bottom) current (10 A/div, 5 ms/div). (b) Bridge (top) and line (bottom) current (10 A/div, 5 ms/div).

bridge (i_L) and active filter currents (i_F). Fig. 9(b) instead shows the thyristor bridge (i_L) and the line compensated currents (i_S). It is possible to see that the main effect of the calculation delay of the dead-beat controller is the presence of compensation errors corresponding to any bridge commutation. This effect is evaluated by calculating the line current spectrum, which is depicted in Fig. 10. As can be seen, in the case of the small firing angle and the consequent reduced current slope at the thyristors' turn-on, the harmonic content is fairly close to the standard limitations. Fig. 11 shows the estimated line voltage, the actual line voltage, and line current. As can be seen, the estimation of the line voltage is precise and almost unaffected by the inverter current transients, revealing a good tuning of control parameters.

The same set of experimental tests is performed in a different operating condition in which the thyristor bridge firing angle is increased up to about $65° \div 75°$, so that the slope of the bridge currents at turn-on is almost at its maximum. Note that, as shown in Fig. 5, the difference between this condition and the worst case (90°) is small. To maintain a similar power absorption from the grid, the bridge load has been accordingly reduced. Due to the steeper current slope, the quality of the compensation is much lower than in the preceding condition, as shown by Fig. 12(a) and (b). This is further confirmed by the line current harmonic content measurement, which is clearly outside the limitations imposed by the standards, as shown by Fig. 13. Again, Fig. 14 shows a good agreement between the effective and the estimated line voltage.

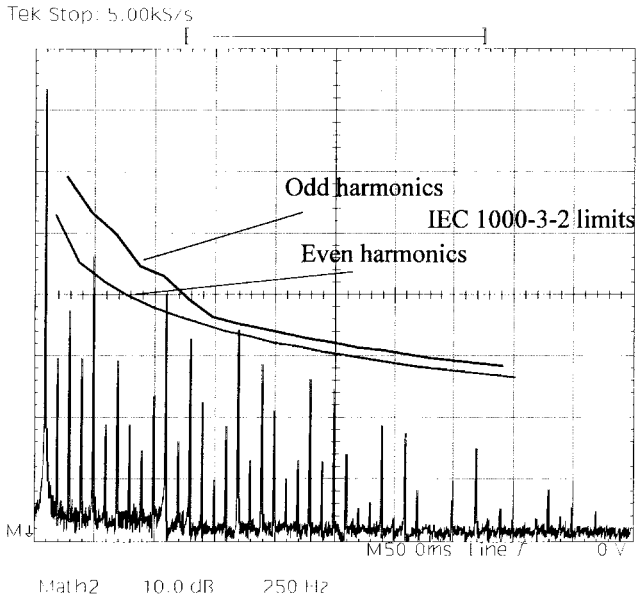


Fig. 19. Line current spectrum (10 dBA/div, 250 Hz/div).

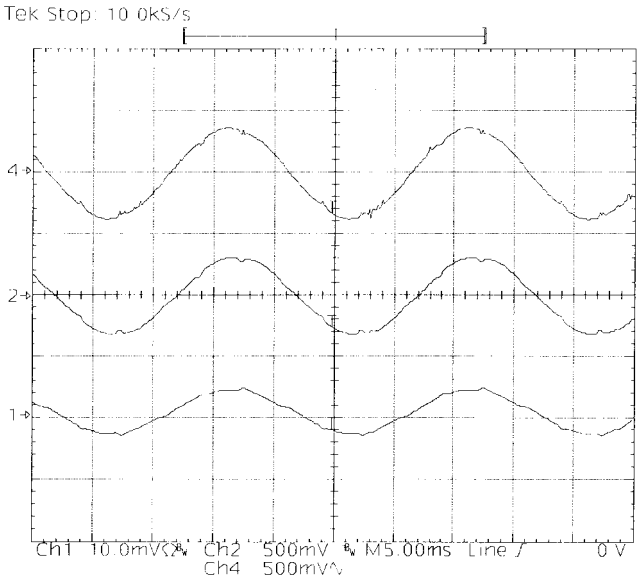


Fig. 20. From top to bottom: estimated line voltage (500 mV/div, 5 ms/div); measured line voltage (500 V/div, 5 ms/div); line current (25 A/div, 5 ms/div).

To make meeting the IEC standards possible, passive filters have been inserted between the line and the active filter according to the previously discussed criteria ($L_1 = 2.4$ mH $= 0.055$ pu, $C_1 = 23\ \mu$F $= 0.1$ pu, $L_2 = 2.6$ mH $= 0.06$ pu). Then, the experimental tests have been repeated in similar operating conditions of the thyristor rectifier load. At first, a small thyristor bridge firing angle has been considered (25° ÷ 30°). Figs. 15–17 show the measured waveforms for this case. As can be seen, the line current, which is now filtered by the inserted passive filters, exhibits a reduced high-frequency harmonic content. This keeps the current spectrum within the standard limits. Fig. 17, in particular, shows that, with the chosen passive filter parameters, no stability problems arise in the voltage estimation algorithm.

Finally, Figs. 18–20, describe the compensation system behavior with an increased firing angle (65° ÷ 75°). Again, the bridge resistive load has been modified to maintain a similar power absorption with respect to the previous situation. As can be seen in Fig. 19, the line current spectrum is now within the standard limits.

VII. Conclusion

The harmonic and reactive power compensation for a thyristor bridge rectifier pertaining to the IEC 1000-3-2 standard class A equipment has been shown to be an extremely difficult task for a digitally controlled parallel active filter. The dead-beat control strategy, in fact, being affected by calculation delays, turned out to be inadequate for the task, even when control refinements and a considerably high switching and sampling frequency were adopted. The main problem was shown to be the high-frequency harmonic content, which is very difficult to keep within the very strict standard limitations. The addition of passive filters to reduce this harmonic content in the line current was, therefore, investigated. The main problems concerning this solution were shown to be, on the one hand, the control sensitiveness to the passive filters, which may cause instability problems and, on the other hand, the identification of a suitable design procedure. Both of these problems were addressed in this paper. The implementation of the digital dead-beat control with a floating-point DSP was then illustrated and, finally, some experimental results, coming from laboratory tests on a prototype of the compensation system, were given to validate the analysis of the problem.

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Simone Buso (M'98) received the Dr. and the Ph.D. degrees from the University of Padova, Padova, Italy, in 1992 and 1996, respectively, both in electronic engineering.

Since 1998, he has been a Researcher in the Department of Electronics and Informatics, University of Padova. His major fields of interest include analysis and control of power converters, digital control techniques, and computer simulation of power electronic circuits.

Luigi Malesani (M'63–SM'93–F'94) was born in Lonigo, Vicenza, Italy, in 1933. He received the Dr. degree in electrical engineering, with honors, from the University of Padova, Padova, Italy, in 1962.

From 1963 to 1964, he was a Researcher in the Centro Gas Ionizzati of CNR. At the University of Padova, from 1964 to 1975, he was an Assistant Professor of Electrical Engineering, from 1968 to 1975, he was an Associate Professor of Electronic Components, and, since 1975, he has been a Professor of Applied Electronics. His interests include power electronics, circuit design, electrical machines, and automatic control. He is the author of several published technical papers on these subjects.

Prof. Malesani is member of the Italian Association of Electrical and Electronic Engineers (AEI).

Paolo Mattavelli (S'95-A'96) received the Dr. degree (with honors) and the Ph.D. degree from the University of Padova, Padova, Italy, in 1992 and 1995, respectively, both in electrical engineering.

He has been a Researcher with the Department of Electrical Engineering, University of Padova, since 1995. His major fields of interest include static power conversion, control techniques, and digital simulation.

Dr. Mattavelli is a member of the IEEE Power Electronics, IEEE Industry Applications, and IEEE Power Engineering Societies and the Italian Association of Electrical and Electronic Engineers.

Roberto Veronese was born in Legnago, Verona, Italy, in 1971. He received the Dr. degree in electronic engineering from the University of Padova, Padova, Italy, in 1996.

From 1996 to 1997, he collaborated with the Power Electronics Laboratory, University of Padova, where he worked in the field of digital control of power converters. He is currently with the Department of Electronics and Informatics, University of Padova. His interests are digital control and power electronic systems.