# Robust Dead-Beat Current Control for PWM Rectifiers and Active Filters

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***Abstract*— This paper analyzes the stability limitations of the digital dead-beat current control applied to voltage-source three-phase converters used as pulsewidth modulation rectifiers and/or active filters. In these applications, the conventional control algorithm, as used in drive applications, is not sufficiently robust, and stability problems may arise for the current control loop. The current loop is, indeed, particularly sensitive to any model mismatch and to the possibly incorrect identification of the model parameters. A detailed analysis of the stability limitations of the commonly adopted dead-beat algorithm, based on a discrete-time state-space model of the controlled system, is presented. A modified line voltage estimation technique is proposed, which increases the control's robustness to parameter mismatches. The results of the theoretical analysis and the validity of the proposed modification to the control strategy are finally verified both by simulations and by experimental tests.**

***Index Terms*— Active filters, pulsewidth modulation rectifiers, voltage-source inverter current control.**

## I. Introduction

THE use of fully digital control techniques for pulsewidth modulation (PWM) converters is, more and more often, the preferred design choice, thanks, on the one hand, to the well-known advantages of the digital controls in terms of flexibility, insensitivity to aging effects and/or thermal drifts, ease of implementation and upgrade, and, on the other hand, to the availability of powerful, low-cost microcontrollers ($\mu$C's) and digital signal processors (DSP's).

This paper investigates the stability limits of the dead-beat current control technique [1]–[3], which is now probably the most widely applied digital current control technique for power converter applications, such as power active filters and PWM rectifiers. The conventional dead-beat current control technique can provide a quite satisfactory dynamic performance when the converter's load is exactly identified, both in the structure and in the parameters [1]–[4]. In case of an incorrect load identification, instead, stability problems may arise. Indeed, the presence of tuned filters for the reduction of the high-frequency harmonic content of the line currents and the potential occurrence of resonances between such filters and the line impedance represent a serious limitation to the achievable control's performance. More generally, the presence of model mismatches or, in case of a correctly identified model's structure, of parameter uncertainties and/or variations can cause stability problems to the current control loop, in particular, when a line voltage estimation strategy is adopted, as reported in [2]. This paper extends the analysis of the problem, originally presented in [5], deriving a generalized discrete-time state-space representation of the controlled converter and its load. The analysis procedure reveals the stability margins of the algorithm considering its typical implementation, which employs a conventional line voltage estimation technique, and gives the possibility of predicting the occurrence of oscillations in the current loop by mapping the closed-loop plant's eigenvalues. In addition, a modified estimation technique for the line voltage is proposed, which is shown to increase the control's robustness. All the theoretical forecasts are verified by means of simulations and experimental tests on a reduced-scale power converter.

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## II. Basic Scheme of the System

The basic scheme of the PWM converter application which is discussed in this paper is shown in Fig. 1. As can be seen, the power converter directly feeds an equivalent resistive load $R_L$ on the dc side, but, of course, by suitably calculating the reference for its current control loop, the harmonic and reactive power compensation of a possible distorting load can also be achieved. If this is the case, the resistive load $R_L$ is normally not present. The current generator $i_{\mathrm{Load}}$ is introduced to model a generic distorting load connected in parallel to the PWM converter. Therefore, the depicted situation allows us to describe in a unified manner both the case in which the PWM converter works as a rectifier and the case in which the same converter works as an active power filter. The passive components $L_1$, $C_1$ are required to filter the current high-frequency harmonic components due to the modulation and must be suitably damped to avoid undesired resonant oscillations of the line current $i_S$. Branch $R_2$, $C_2$, shown in Fig. 1, indicates one of the possible configurations to smooth the resonance of the input filter. Actually, it may be substituted by an active damping obtained by a proper control of the PWM converter [6], if the oscillation frequency falls within the current control bandwidth. Finally, it may be worth noting that, in $L_1$, the line impedance is also included.

## III. Control Technique

In the system of Fig. 1, it is assumed that the control of the PWM converter's current is performed by means of the dead-

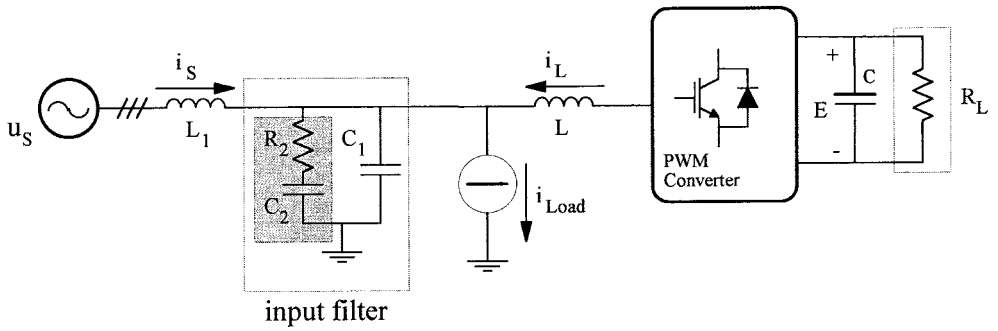


Fig. 1. Basic scheme of the system with the PWM converter.

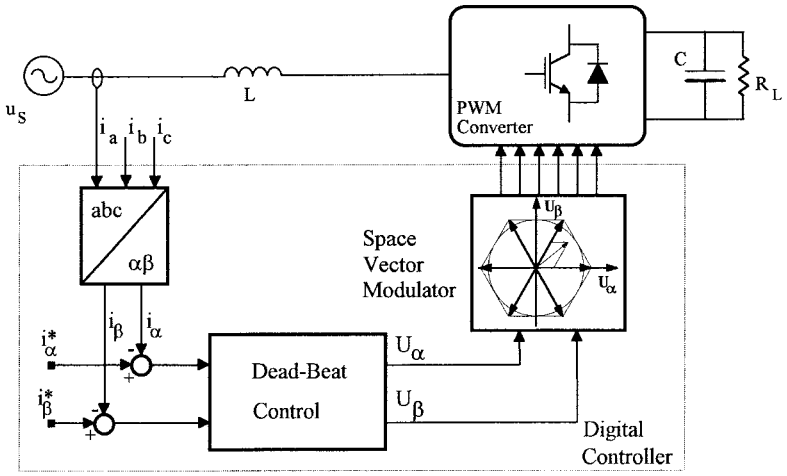


Fig. 2. Basic scheme of the digital dead-beat current regulator.

beat control technique [1]–[7]. As it is well known, in a dead-beat controller the control algorithm calculates the voltage to be generated by the power converter so as to make the phase current reach its reference by the end of the following modulation period. Here, the calculations are performed in the $\alpha$, $\beta$ frame, and the space-vector modulation (SVM) strategy, which very well suits the digital implementation, is adopted for the switching converter. This is essentially the situation depicted in Fig. 2. An important advantage of the dead-beat technique is that it does not require the line voltage measurement in order to generate the current reference. The dead-beat control's algorithm, in fact, allows an estimation of the line voltage instantaneous value, based on the previous modulation periods, which can, therefore, be used also for the current reference generation. On the other hand, the inherent delay due to the calculation time is, indeed, a serious drawback in active filter applications. In particular, when compensating distorting loads, it produces appreciable errors in correspondence of fast current variations. Thus, additional provisions to get to a satisfactory performance level are required [8]. In the more recent versions [2] of the dead-beat controller, the delay may be reduced by sampling the control variables and executing the control routines twice in a modulation period. The turn-on and turn-off times of the power converter switches may be independently decided in two successive control intervals. As a consequence, the aforementioned delay in current reference tracking can be reduced to a single modulation period.

## IV. Stability Analysis of the Dead-Beat Algorithm

Dead-beat control of three-phase inverters has been widely investigated by many researcher in recent years [1]–[5], in particular, for drive applications. The application of this control technique to active filters or PWM rectifiers is almost straightforward; however, the effect of the input filters, commonly used to eliminate the high-frequency harmonic currents generated by the inverter's modulation, must be carefully considered. These filters, in fact, are not normally accounted for in the control algorithm, which refers to an "ideal" load model, where only inverter inductances $L$ are taken into account, as shown in Fig. 3. This is what can be called a *model mismatch*. Due to the presence of the input filters, the dynamic behavior of the current loop changes and may even reach instability. Indeed, a suitable design of the input filters may reduce the occurrence of instabilities, as discussed in [8]. Anyway, similar problems arise also when there is a *parameter mismatch* between the modeled inverter inductance and the actual one [2]. In the following, we restrict our analysis to this last issue. Therefore, in the analysis, the presence of the line impedance, of the input filters, and of the distorting

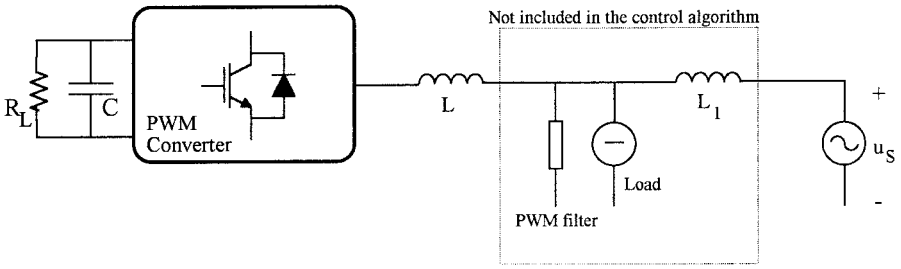


Fig. 3. Simplified representation of Fig. 1.

load are neglected, as shown in Fig. 3. As a consequence, the considered system can also represent a typical drive application where $L$ can be considered the motor inductance and $u_s$ the back electromotive force.

Stability analysis is performed using the discrete-time state-space equations of the remaining first-order system, given by the actual converter inductances $L$. Note the three-phase system is assumed to be balanced and symmetrical. As a consequence, the discrete-time system equations, developed in the $\alpha, \beta$ fixed reference frame, have the following expression:

$$i(k+1) = \frac{T_{\rm sw}}{L}[u_{\rm av}(k) - u_s(k)] + i(k) \tag{1}$$

where $i(k)$ is the inverter current, $u_{\rm av}(k)$ the average phase voltage, generated by the active filter, and $u_s(k)$ the supply voltage, all of them evaluated at the sampling instant $kT_{\rm sw}$.

The control algorithm, which ensures a dead-beat response for the first-order system based on the modeled inductance $L_m$ is given by [1]–[6]

$$u_{\rm av}(k+1) = \frac{L_m}{T_{\rm sw}}[i_{\rm ref}(k) - i(k)] + 2u_s(k) - u_{\rm av}(k) \tag{2}$$

where the line voltage $u_s$ is either measured or estimated. The line voltage estimation can be obtained using the algorithm

$$e_s(k-1) = u_{\rm av}(k-1) + \frac{L_m}{T_{\rm sw}}[i(k-1) - i(k)] \tag{3}$$

and then substituting in (2) $u_s(k)$ with $e_s(k-1)$ [1]–[5].

The stability analysis of the closed-loop system can be performed by applying the $Z$ transform to (1), (2), and possibly (3), by deriving the characteristic polynomial of the closed-loop system, and by mapping the closed-loop poles. If the magnitude of the closed-loop poles is equal or greater than one, the resulting system is, of course, unstable. The instability condition results in oscillations of the system's state variables occurring at the Nyquist frequency.

Following this procedure, it can be found that, if the line voltage is measured, the poles of the closed-loop system given by (1) and (2) are

$$p_{1,2} = \pm\sqrt{\Delta L_{\%}} \tag{4}$$

where $\Delta L_{\%} = 1 - L_m/L$ is the relative error between the actual and the modeled inductance. Equation (4) shows that system stability is ensured up to 100% error in the modeled inductor $L_m$, revealing a considerable robustness to parameter mismatches for this condition. It is worth noting that only positive values of $\Delta L_{\%}$ will be presented throughout the analysis, since this reveals that negative values always imply a somewhat higher stability margin. Therefore, positive errors (implying an underestimation of $L$) have been considered as the worst case.

Instead, if the line voltage is estimated using (3), it turns out that the characteristic polynomial of the closed-loop system, determined by (1)–(3), is

$$\lambda(z) = z^3 - 3\Delta L_{\%} z + 2\Delta L_{\%}. \tag{5}$$

The closed-loop poles, obtained solving $\lambda(z) = 0$, show that only a 20% error is allowed before the system instability occurs. It is worth noting this result is independent of switching frequency, since (5) is only a function of the relative error $\Delta L_{\%}$.

A significant change in the system behavior is obtained when the active filter current reference $i_{\rm ref}(k)$ is a function of the line voltage estimation $e_s(k-1)$

$$i_{\rm ref}(k) = -G_{\rm eq} e_s(k-1) + K_{\rm af} \cdot i_{\rm Load}(k). \tag{6}$$

Indeed, this provision, which avoids the use of the line voltage sensors, is peculiar to active filters and high-quality rectifiers, where the line current reference is related to the line voltage, and does not occur in drive applications. Note that $K_{\rm af}$ is one when the converter is operating as an active filter and is equal to zero when the converter operates as a rectifier. Being an external independent input, the presence of $i_{\rm Load}$ does not affect the stability limits of the system. Using (6) into (2) and applying the $Z$ transform to (1)–(3), we derived that the closed-loop poles are given by the following characteristic polynomial:

$$\lambda(z) = z^3 - \Delta L_{\%}(3-K)z + \Delta L_{\%}(2-K) = 0 \tag{7}$$

where $K = G_{\rm eqpu}/2m\Delta i_{\max\%}$, and $G_{\rm eqpu}$ is the per-unit equivalent conductance of the compensated load, directly related to the active power absorbed by the load, $m$ is the maximum inverter modulation index $(m = 2\hat{U}_s/E)$, and $\Delta i_{\max\%}$ is the maximum relative ripple of the inverter currents. Equation (7) shows that the closed-loop poles are strongly dependent on the conductance $G_{\rm eqpu}$ and, thus, on the operating condition of the load. When $G_{\rm eqpu}$ is zero, (7) reduces to (5) and the 20% margin on the inductance error still applies. Instead, when $G_{\rm eqpu}$ is greater than zero, the stability limits change and depend also on the system parameters. Assuming that the maximum modulation index

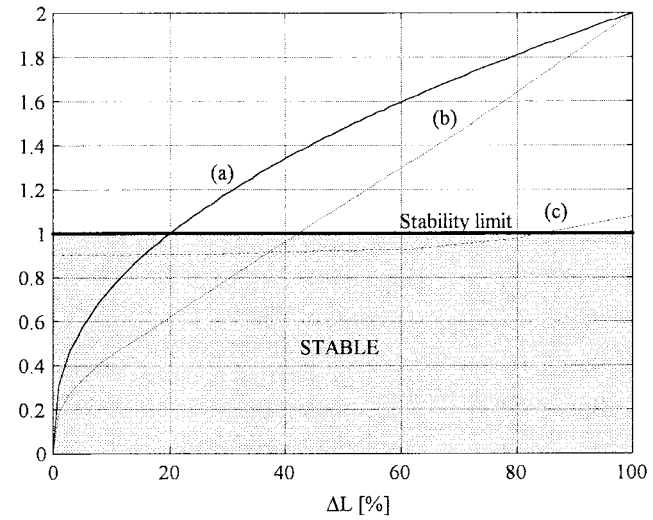


Fig. 4. Absolute value of the maximum closed-loop plant eigenvalue as a function of the relative estimation error on $L$. Solid line (a): line voltage conventional estimation; dashed line (b): reference calculation based on voltage estimation; dash-dotted line (c): proposed estimation technique.

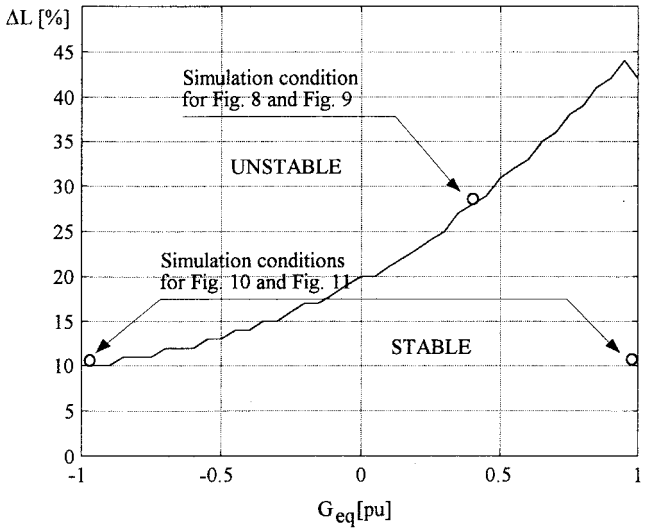


Fig. 5. Absolute value of the maximum relative error on the converter inductance $L$ as a function of the $G_{\mathrm{eqpu}}$. The simulated conditions, which give the results reported in Section V, are explicitly indicated.

is 0.9 and $\Delta i_{\max\%}$ is 10%, it can be found that the use of (6) improves the stability limit up to a 43% margin on the inductance error when $G_{\mathrm{eqpu}}$ is close to its maximum value, which is, of course, unity. Fig. 4 shows the maximum absolute value of the closed-loop poles for the aforementioned conditions as a function of the relative error $\Delta L_{\%}$. Trace (a) refers to $G_{\mathrm{eqpu}}$ equal to zero, and trace (b) refers to $G_{\mathrm{eqpu}}$ equal to one. Note that the system robustness is increased in the last condition since the maximum error $\Delta L_{\%}$, which is allowed before instability occurs, moves from 20% to 43%. Indeed, this result is not general and strongly depends on the system parameters (dc-link voltage, supply voltage, inductance $L$, switching frequency). Moreover, it is worth noting that, for applications where the power converters are injecting active power into the line, which correspond to negative values for $G_{\mathrm{eqpu}}$, the maximum allowed error $\Delta L_{\%}$ is drastically reduced. This may be the case of PWM rectifiers feeding ac or dc drives, during motor braking; stability problems may be encountered if the converter inductance is not very precisely determined, as shown by Fig. 5.

In order to improve the system's stability, a modified algorithm for the estimation of the line voltage $u_s(k)$ is proposed here. This modification is based on the fact that the aforementioned instabilities occur at half the switching frequency, which is, of course, much higher than the supply frequency, mainly because of the interaction between the estimation algorithm (3) and the control law (2). However, it is possible to eliminate the aforementioned interaction using a filter on the estimated voltage $e_s(k)$ which provides attenuation at high frequency and, at the same time, maintains the same low-frequency content. The block diagram corresponding to the proposed control implementation is shown in Fig. 6. It is worth noting that the other possible solution to the problem, that is, the filtering of the current reference, provides only a partial improvement. This is due to the fact that, while the filtered current reference is decoupled by the estimation algorithm, the oscillations in the estimated voltage can still affect the current control algorithm (2) and destabilize the system. Consequently, with $G_{\mathrm{eqpu}} > 0$, the actual stability margin of the system is reduced, since the situation is almost equivalent to the independent generation of the current reference, which, as shown by Fig. 4 [trace (a)] exhibits a lower stability margin compared to the case when the current reference is proportional to the estimated line voltage [trace (b)]. On the other hand, when $G_{\mathrm{eqpu}}$ becomes negative, this solution improves the stability margin to the level characterizing the independently generated reference. In conclusion, the stability margin is kept at the level of the independently generated reference, no matter the sign of $G_{\mathrm{eqpu}}$. This, of course, represents an improvement only in the case of negative values of $G_{\mathrm{eqpu}}$. Filtering the estimated voltage, instead, decouples both the reference generation and the current control from the possible oscillations of the estimation algorithm, ensuring, in principle, a superior robustness to the system's stability.

Since the line voltage $u_s(t)$ can be considered almost sinusoidal at a fixed frequency, a proper choice for the aforementioned filter is a digital bandpass filter centered at the supply frequency, the expression of which is given by (8), where $\lambda = 2\pi f_B T_s$, $f_B = 50$ Hz (filter frequency equal to the line frequency), $T_s = 100$ $\mu$s (sampling period), and $m$ is the resonant poles' magnitude

$$W(z^{-1}) = \frac{2\cos\lambda(1-m)z^{-1} + (m^2-1)z^{-2}}{1 - 2m\cos\lambda z^{-1} + m^2 z^{-2}}. \quad (8)$$

This solution minimizes the phase shift at the supply frequency compared to low-pass-filter solutions, being simple to implement and not time consuming.

The improvement given by this provision is shown by trace (c) of Fig. 4, obtained using $G_{\mathrm{eqpu}} = 0$ and the second-order bandpass filter (8) with a resonant pole couple having a magnitude of 0.9. We can see that, with this provision, the maximum relative error $\Delta L_{\%}$ moves from 20% [trace (a)] to 84% [trace (c)]. A smaller improvement can be achieved by reducing the

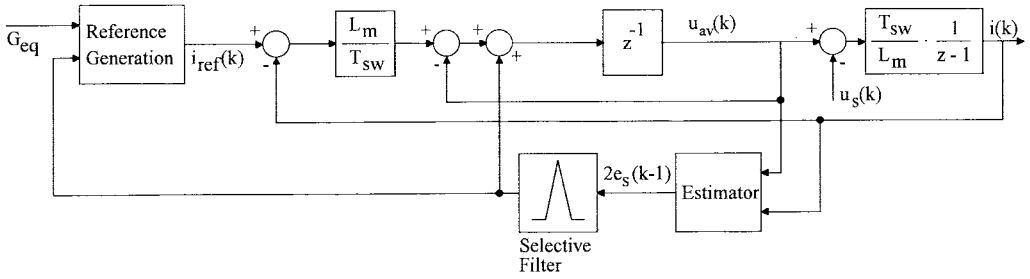


Fig. 6. Block diagram of the proposed control solution.

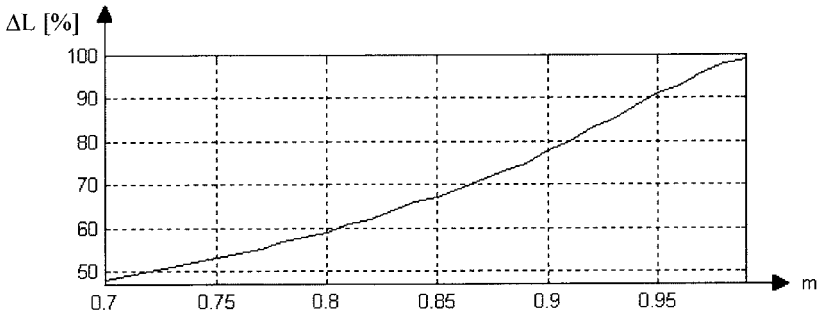


Fig. 7. Relationship between the stability margin $\Delta L_{\%}$ and the magnitude of the bandpass filter poles $m$.

TABLE I
PROTOTYPE RATINGS

| | |
|---|---|
| Phase Voltage (RMS) | 85 V |
| Output Power | 1 kW |
| DC Link Voltage | 300 V |
| Active Filter Inductance | 1.8 mH |
| Switching Frequency | 10 kHz |

magnitude of the bandpass filter poles, thus achieving a faster transient response and a lower sensitivity to possible supply frequency variations. The relationship between the stability margin and the magnitude of the filter's resonant poles is given by Fig. 7. The figure has been derived considering $G_{\mathrm{eqpu}} = 1$; the plot has also been calculated for different $G_{\mathrm{eqpu}}$ values, exhibiting only slight differences. It is worth noting that, in the presence of sudden variations of the line voltage, e.g., during voltage sags, the current control response is delayed by the bandpass filter dynamics, which, in principle, may determine a certain degradation in the performance of the current loop.

## V. SIMULATION RESULTS

The results of the described mathematical analysis and the effectiveness of the suggested modification to the line voltage estimation strategy have been verified by means of numerical simulations. The system of Fig. 1 has been simulated considering for the PWM converter both a simple rectifier and an active filter operating mode. The system's parameters are shown in Table I. The internal model inductance $L_m$ has been altered on purpose with respect to the actual value $L$ in order to generate the predicted stability problems. Figs. 8 and 9 describe the effect of the filtering of the estimated voltage in the active filter operating mode. The altered $L$ value is 1.275

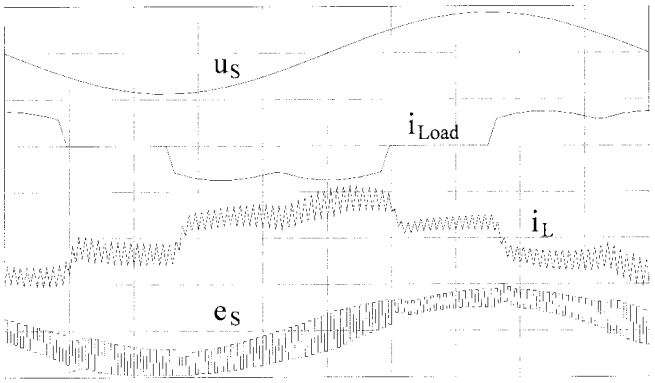


Fig. 8. Simulated active filter behavior with the classical estimation technique: $u_s$(80 V/div), $i_{\mathrm{Load}}$ (12 A/div), $i_L$ (12 A/div), $e_s$ (150 V/div), time scale (2 ms/div).

mH, which corresponds to $\Delta L_{\%} = 29\%$. Since the adopted $G_{\mathrm{eqpu}}$ is quite small (0.41), the stability margin results in being slightly larger than 20%, which is the minimum margin with independent generation of the current reference. This is in good agreement with Fig. 5, where the simulated points are highlighted. Therefore, in Fig. 8, the active filter current and the estimated line voltage oscillate at half the sampling frequency. As theoretically predicted, the oscillating behavior of the system's variables is removed by filtering the estimated voltage, as can be seen in Fig. 9. The same verification is done for the rectifier operating mode. As can be seen in Fig. 10, the rectifier is operated with $G_{\mathrm{eqpu}} > 0$ (active power is absorbed from the utility grid) for 10 ms, then the power flux is reversed for 20 ms $(G_{\mathrm{eqpu}} < 0)$ with $\Delta L_{\%} = 11\%$, when the rectifier works as a generator, oscillations appear on the current and

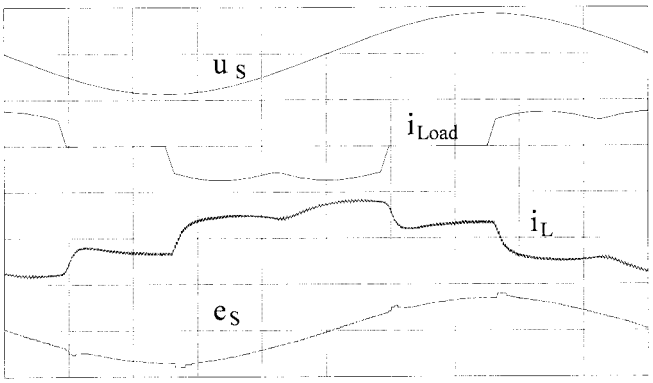


Fig. 9. Simulated active filter behavior with a bandpass filter in the estimation algorithm: $u_s$ (80 V/div), $i_{\mathrm{Load}}$ (12 A/div), $i_L$ (12 A/div), $e_s$ (150 V/div), time-scale (2 ms/div).

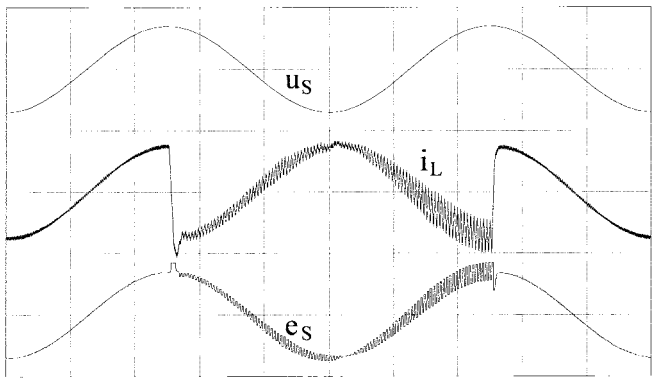


Fig. 10. Simulated PWM rectifier behavior with the classical estimation technique: $u_s$ (100 V/div), $i_L$ (12 A/div), $e_s$ (150 V/div), time-scale (4 ms/div).

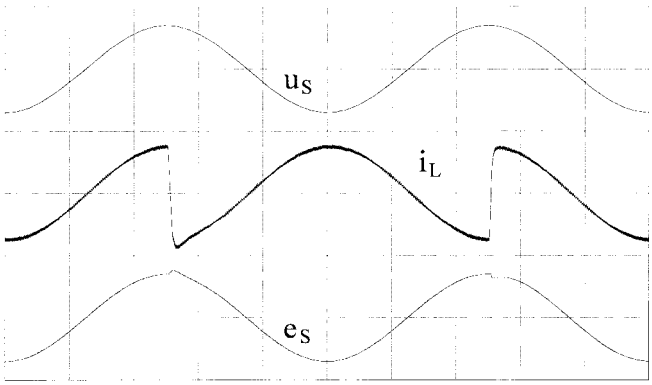


Fig. 11. Simulated PWM rectifier behavior with a bandpass filter in the estimation algorithm: $u_s$ (100 V/div), $i_L$ (12 A/div), $e_s$ (150 V/div), time-scale (4 ms/div).

estimated voltage. The reduction of the stability margin is due to the negative value of $G_{\mathrm{eqpu}}$, as predicted by Fig. 5. Again, as shown by Fig. 11, the oscillatory behavior is removed, as expected, when the estimated voltage is filtered. It is important to note that the simulations fully confirm the validity of the theoretical forecasts and reveal the generality of the analytical approach, which equally applies to PWM rectifiers and active filters.

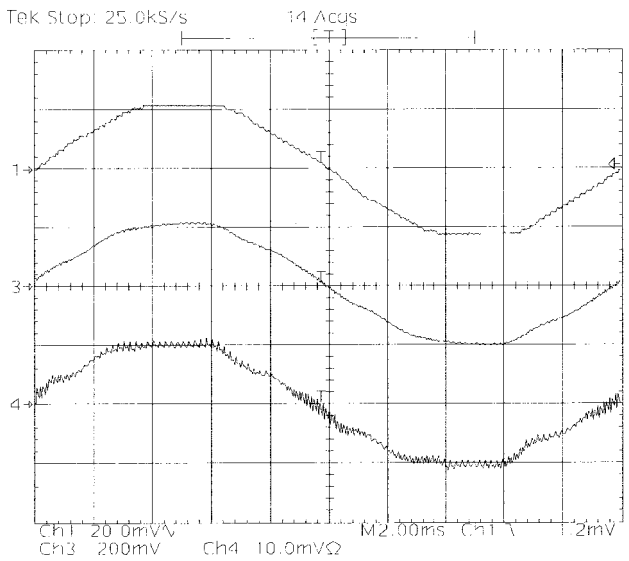


Fig. 12. Test conditions: no filter on the estimated line voltage; $V_{\mathrm{dc}} = 120$ V; $\Delta L_{\%} = 0$; time scale: 2 ms/div; rectifier mode;Upper trace: estimated line voltage (200 mV/div). Middle trace: line to neutral measured voltage (40 V/div). Lower trace: phase current (1 A/div).

## VI. Experimental Results

The considered system has been experimentally tested, in a PWM rectifier operating mode, with the inverter inductance and switching frequency reported in Table I. Fig. 12 shows the system variables when a correct identification of the inverter inductance $L$ is achieved. No filter is adopted for the estimated line voltage, but, thanks to the absence of parameter mismatches, both the line current and the estimated voltage are stable and free of oscillations. When a different inductance value is inserted in the control algorithm, corresponding to $\Delta L_{\%} = 12\%$, the system begins oscillating, as shown by Figs. 13 and 14. The oscillations take place at half the sampling frequency, as expected. The low stability margin is due to the presence of unavoidable unsymmetries in the converter phases which further deteriorate the stability margin. It can also be found that the effect of the converter dead times, particularly evident in the low current operating condition that has been chosen, is a factor which reduces the stability margin.

Fig. 15, instead, shows the system's behavior in the case of a reversal in the power flow. The power flows now from the dc side of the converter to the line, as can be typical in drive applications, when the motor is reducing its rotation speed (regenerative braking). As can be seen, the system is stable, but, when a small error in the inductor value is inserted in the control algorithm, the system goes unstable, as shown by Fig. 16. Note that $\Delta L_{\%}$ is now equal only to 5%.

This reveals the potential problems that can be encountered using the conventional dead-beat current control for bidirectional power flow converters. The use of some decoupling technique, such as the one suggested in this paper, seems, in this case, to be mandatory. Finally, Fig. 17 shows the behavior of the system when the filter on the estimated line voltage is adopted. The occurrence of oscillations is also removed in case of very high values of $\Delta L_{\%}$, which, in this case, could

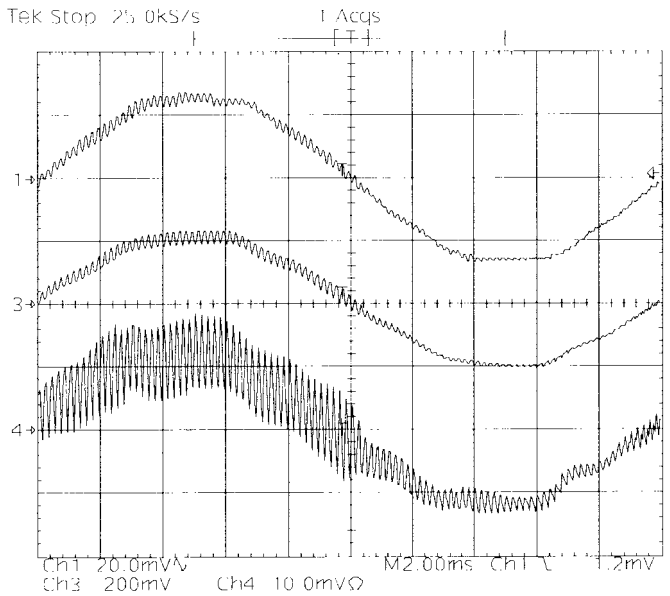


Fig. 13. Test conditions: no filter on the estimated line voltage; $V_{\rm dc} = 120$ V; $\Delta L_{\%} = 12\%$; time-scale: 2 ms/div; rectifier mode. Upper trace: estimated line voltage (200 mV/div). Middle trace: line-to-neutral measured voltage (40 V/div). Lower trace: phase current (1 A/div).

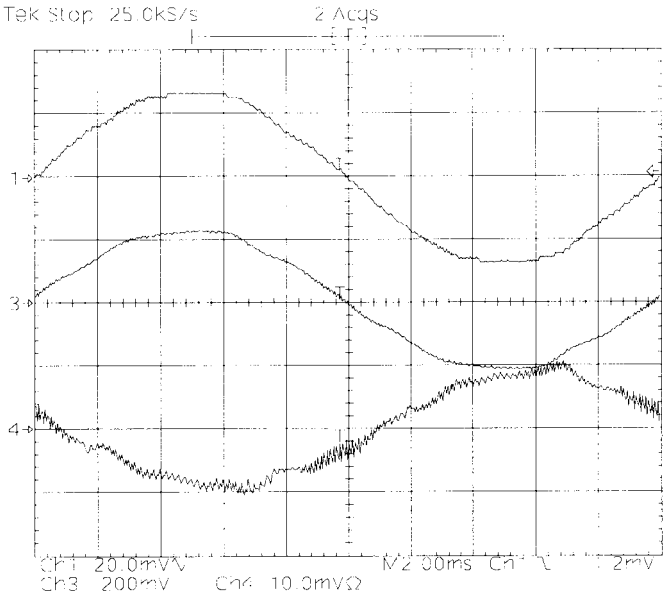


Fig. 15. Test conditions: no filter on the estimated line voltage; $V_{\rm dc} = 120$ V; $\Delta L_{\%} = 0$; time scale: 2 ms/div; generator mode. Upper trace: estimated line voltage (200 mV/div). Middle trace: line-to-neutral measured voltage (40 V/div). Lower trace: phase current (1 A/div).

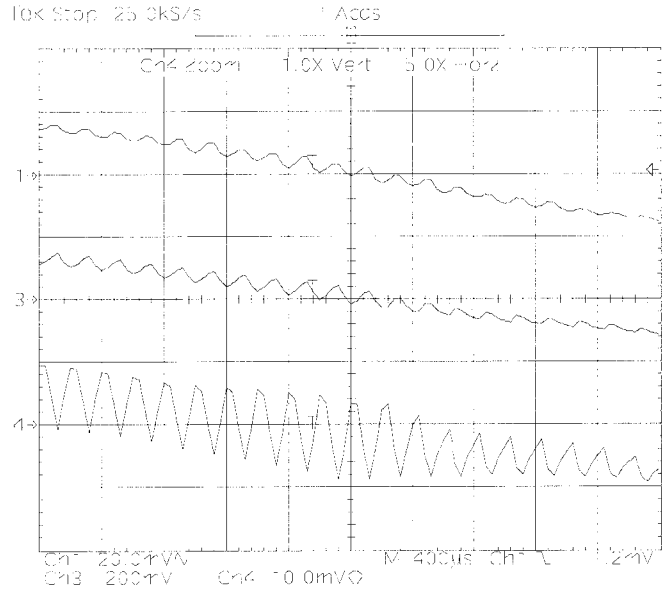


Fig. 14. Test condition: no filter on the estimated line voltage; $V_{\rm dc} = 120$ V; $\Delta L_{\%} = 12\%$; time scale: 400 $\mu$s/div; rectifier mode. Upper trace: estimated line voltage (200 mV/div). Middle trace: line-to-neutral measured voltage (40 V/div). Lower trace: phase current (1 A/div).

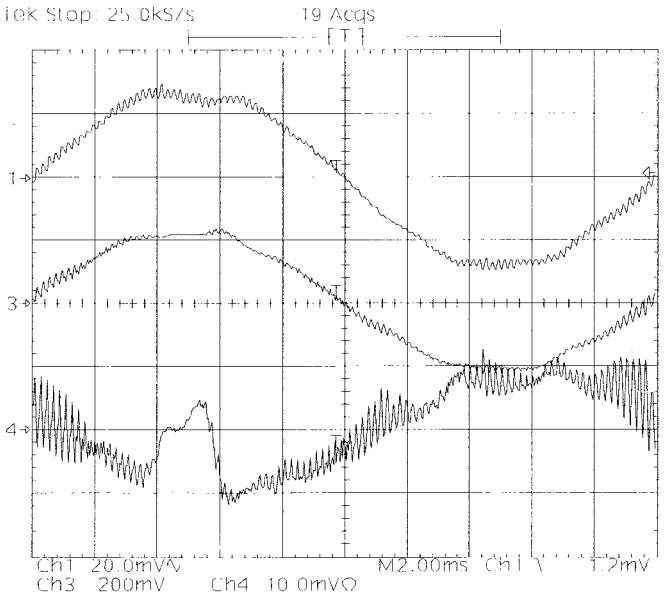


Fig. 16. Test conditions: no filter on the estimated line voltage; $V_{\rm dc} = 120$ V; $\Delta L_{\%} = 5\%$; time scale: 2 ms/div; generator mode. Upper trace: estimated line voltage (200 mV/div). Middle trace: line-to-neutral measured voltage (40 V/div). Lower trace: phase current (1 A/div).

reach 45%, without generating any instability in the system, even for regenerative braking mode of operation (worst case condition). The depicted situation refers to $\Delta L_{\%} = 30\%$.

## VII. Conclusion

This paper has presented a theoretical analysis of the stability robustness of the digital dead-beat current control technique with respect to parameter mismatches. These are very likely to be encountered when considering active filter and rectifier applications of current-controlled voltage-source converters. The paper proposes an effective analysis technique which enables one to predict the occurrence of instability problems, revealing the different robustness levels of the possible implementations of the converter's dead-beat control. The key role of the line voltage estimation technique in determining the control's robustness is evidenced, and a novel estimation strategy, which guarantees a superior performance level, is proposed. This solution consists of decoupling the estimation

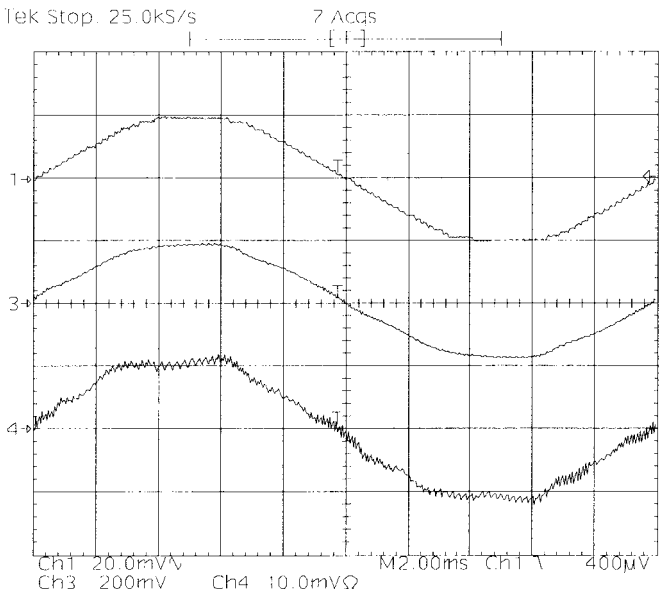


Fig. 17. Test condition: filter on the estimated line voltage both for reference and dead-beat calculations; $V_{\rm dc} = 120$ V; $\Delta L_{\%} = 30\%$; time scale: 2 ms/div; rectifier mode. Upper trace: estimated line voltage (200 mV/div). Middle trace: line to neutral measured voltage (40 V/div). Lower trace: phase current (1 A/div).

algorithm, both from the current reference generation and from the dead-beat modulation algorithm. The effect is achieved by means of a simple bandpass digital filter on the estimated voltage. The effectiveness of the theoretical analysis and of the proposed improvements has been verified by simulations and experimental tests on a laboratory PWM rectifier.

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