Single-phase ac/dc integrated PWM converter

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Abstract **- The paper proposes a new topology of a boost type ac/dc PWM converter featuring high power factor, full control of the output dc voltage and high-frequency line filter inductor and insulation transformer. Its main advantage is the complete integration of a rectifier and an inverter stage, so that a compact converter with only four IGBT's and six diodes is obtained. The integration poses some constraints on the line current control capability of the converter, which is limited. Nevertheless, the compliance with EMC standards (IEC 61000-3-2) is possible for a wide load range. The paper presents a detailed analysis of the topology, highlighting the design constraints and proposes a possible design procedure, which is then verified by means of numerical simulations.**

I. Introduction

The industrial interest for compact ac/dc converter topologies integrating an high quality rectifier and a dc/dc or dc/ac stage is very high and has motivated several topology proposals, widely described in the literature both for low power applications, up to 200 – 300 W [1]-[4], and for higher power levels [5]-[7]. The goal of such integrated converters is to obtain both power factor correction and load voltage regulation with a reduced number of components with respect to conventional two-stage solutions, thus minimising the cost and the size of the power converter and increasing its efficiency. In general, the integration of the two stages constrains the achievable performance, either on the load side or on the line side so that a limited control of the input current or of the output voltage must be accepted. This paper proposes an integrated ac/dc PWM converter capable of providing an high quality input current, compliant with IEC 61000-3-2 low frequency EMC standard, and to guarantee a fast dynamic control of the load side voltage. The structure integrates a diode bridge rectifier and a full bridge inverter. As a consequence, it appears to be particularly suitable for applications in the medium to high power range (up to some kW's). Employing only four IGBT's, six diodes and high frequency input inductor and insulation transformer, the converter is potentially capable of ensuring high power densities. The paper initially describes the converter operation. Then, it discusses the design criteria to achieve a satisfactory performance both on the load and on the line side. The constraints on the power converter control capability are finally analysed and a suitable control strategy is proposed to shape the input current and control the output voltage. The design procedure and the proposed control strategy are verified and tested by means of detailed numerical simulations, whose results are reported in the final part of the paper.

II. Converter Structure

A. Converter Scheme and Operating Modes

The basic scheme of the proposed converter is shown in Fig. 1. As can be seen, the converter employs four IGBT switches, which are arranged in a typical full-bridge inverter configuration, and six diodes. The two upper diodes (D_1 and D_2) are the free-wheeling diodes needed by the inductive load of the inverter, while the four lower diodes (D_{3a} to D_{4b}) act both as free-wheeling diodes and line current rectifiers. It must be noted that this topology also allows standard IGBT modules (comprising the free-wheeling diodes) to be adopted, provided that the four rectifier bridge diodes are externally added. Filter capacitor C_f ensures a constant dc voltage for

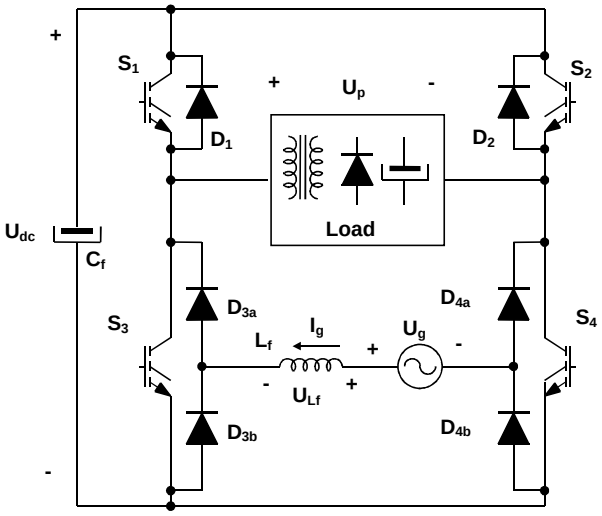

Fig. 1 – Converter basic scheme

the inverter operation. Input inductor L_f provides the necessary filtering action on the input current. Finally, the converter load, which is only schematically represented in Fig. 1, includes the insulation transformer, the rectifier stage and the inductive-capacitive filter needed to smooth the output voltage.

The converter operation is now explained assuming that a stable dc voltage U_{dc} is maintained across capacitor C_f all along the modulation period, that the input voltage U_g is positive and suitably lower than U_{dc} and that an almost unity power factor is achieved so that the line frequency harmonic component of the input current can be considered practically in phase with the input voltage U_g. In these conditions, the line current will flow through diodes D_{3a} and D_{4b} of the rectifier stage. When the diagonal S_1 - S_4 is turned on a positive voltage equal to U_{dc} is applied to the load, while a negative voltage (equal to U_g - U_{dc}) is applied to the input inductor. The line current I_g is therefore forced to decrease. When the opposite diagonal is turned on (S_2 - S_3), a negative voltage (-U_{dc}) is applied to the load while a positive voltage (equal to U_g) is applied to the input inductor. The input current is now forced to increase. These are the powering phases of the converter. Clearly, because of the transformer used the to isolate the load, the duration of these two phases in a modulation period must always be the same, so as to allow the magnetising current reset. By varying the duration of the powering phases it is possible to regulate the average value U_o of the rectified output voltage, in principle between 0 and U_{dc} (assuming a unity turns ratio for the transformer). Two free-wheeling phases are also possible, both imposing a zero voltage across the load: by turning on switches S_1 and S_2 a negative voltage is applied to the input inductor (equal to U_g - U_{dc}) which forces the input current to decrease, while, by turning on switches S_3 and S_4 a positive voltage (equal to U_g) is applied to the input inductor, which forces the input current to increase. As a consequence, control of the input current is possible during the free-wheeling phase of the load by properly selecting the switch combination (S_1 - S_2 or S_3 - S_4) to use. Of course, similar considerations are possible in the case of a negative input voltage U_g. Table I sums up all of the considered switch combinations, highlighting their effect on the transformer primary side voltage U_p and input current I_g.

B. Structural Constraints

The converter exhibits some structural constraints that limit its capability to fully control the input current waveform. As previously explained, the control of the input current only takes place during the free-wheeling phases of the load. This implies that, when the modulation index of the converter M, defined as the ratio between the average, in the modulation period, of the rectified output voltage U_o, and the DC link voltage U_{dc} (1), is close to unity, very little time is available to control the input current.

$$M = \frac{U_o}{U_{dc}} \tag{1}$$

This implies that the input current can be successfully controlled and forced to be proportional to the input voltage only during a fraction of the line period. To better clarify this point we now consider the average inductor voltage as a function of the sinusoidal input voltage $U_g(\theta)$ and dc link voltage U_{dc}. The following equation (2), states that, in order to control the input current, it must be possible to force a zero

TABLE I – CONVERTER OPERATING MODES

Switches ON	Diodes ON	U_g	U_p	I_g
S_1-S_2	D_1, D_{3a}, D_{4b}	>0	0	decrease
S_1-S_2	D_2, D_{3b}, D_{4a}	<0	0	increase
S_3-S_4	D_{3a}, D_{4b}	>0	0	increase
S_3-S_4	D_{3b}, D_{4a}	<0	0	decrease
S_1-S_4	(D_1), D_{3a}, D_{4b}	>0	+U_{dc}	decrease
S_1-S_4	D_{3b}, D_{4a}	<0	+U_{dc}	decrease
S_2-S_3	D_{3a}, D_{4b}	>0	-U_{dc}	increase
S_2-S_3	(D_2), D_{3b}, D_{4a}	<0	-U_{dc}	increase

average voltage across the input inductor. Imposing this condition, we obtain:

$$U_{dc} \cdot [M/2 + \delta(\theta) \cdot (1 - M)] = \left| U_g(\theta) \right|, \tag{2}$$

where $\delta(\theta)$ represents the duty-cycle used in the input current control. The independent variable θ is the instantaneous line angle, equal to $2 \cdot \pi \cdot f_{line} \cdot t$, f_{line} being the line frequency and t the time variable.

Equation (2) implies that the duty-cycle $\delta(\theta)$, required to control the input current, has to satisfy the following conditions:

$$\begin{cases} \delta(\theta) = \dfrac{\dfrac{\left|U_g(\theta)\right|}{U_{dc}} - \dfrac{M}{2}}{1 - M} \\ 0 \le \delta(\theta) \le 1 \end{cases} \tag{3}$$

It is then possible to see that (3) can only be satisfied in the fraction of the line period when:

$$U_{gmin} < |U_g(\theta)| < U_{gmax}, \tag{4}$$

where U_{gmin} and U_{gmax} are given by the following relations:

$$\begin{aligned} U_{g\,min} &= \frac{M}{2} \cdot U_{dc} \\ U_{g\,max} &= \left(1 - \frac{M}{2}\right) \cdot U_{dc} \end{aligned} \tag{5}$$

Based on (2), (3), (4) and (5) Fig. 2 has been computed. Defining the current control angle ϕ as the fraction of the line half-period where current control is possible (expressed in degrees), Fig. 2 shows two quantities as functions of ϕ. One is the maximum allowed converter modulation index M_{max},

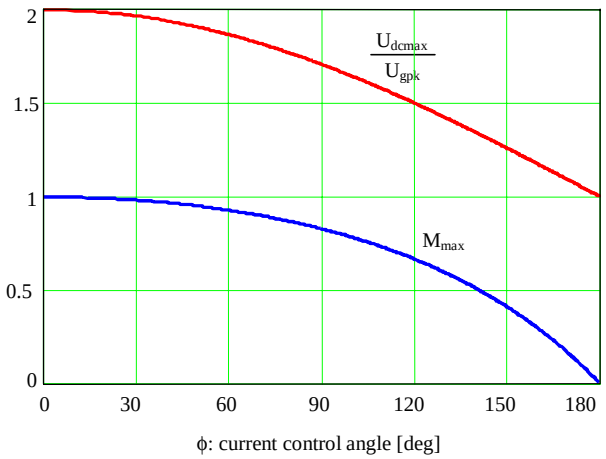

Fig. 2 – Upper trace: ratio between U_{dc} and line voltage peak value U_{gpk} as a function of the line control angle. Lower trace: maximum modulation index M_{max} as a function of the line control angle.

while the other is the ratio between the maximum allowed dc link voltage U_{dcmax} and the line voltage peak value U_{gpk}. Given the desired control angle, using Fig. 2 it is possible to determine what are the maximum modulation index M and dc link voltage U_{dc} compatible with that angle.

Fig. 2 also shows that it is not possible to achieve simultaneously an high modulation index M and the full control of the line current. Moreover, increasing the dc link voltage also implies a reduction of the current control angle.

When the input voltage does not satisfy (4), two situations are possible: if $|U_g(\theta)| < U_{gmin}$ (2) shows that the line current will be forced to decrease to zero and the converter will operate in discontinuous conduction mode at the input side. Instead, if $|U_g(\theta)| > U_{gmax}$ the input current amplitude will be forced to steadily increase. In both cases the line current waveform will significantly differ from the ideal sinusoidal waveform exhibiting a certain distortion. A careful design, anyway, allows to achieve a satisfactory line side behaviour, as it will be shown in section V.

Finally, we must observe that, during each modulation period, one of the two load powering phases implies the absorption of power from the line. This means that the converter cannot operate in no-load conditions, because the power flow from the line to the converter in each modulation period cannot be reduced to zero nor even reversed, due to the presence of the input diode bridge. In other words, a minimum load must always be guaranteed to ensure the power balance. Moreover, when the output power gets close to the minimum level, the control of the input current is lost. Anyway, we will show that for our design, acceptable operation is possible down to 10% of the nominal output power.

III. Power Converter Design

A. Preliminary considerations

Assuming the basic specifications which are listed in Table II, a possible design procedure is as follows. We select first of all a convenient value for the dc link voltage U_{dc}. A suitable choice is 500 V, which allows the use of 600 V switches. From this value and the peak line voltage, (5)

Table II – Design Specifications

Line voltage	U_g	240 ± 10%	V_{RMS}
Output power	P_o	5	kW
Switching frequency	f_{sw}	20	kHz
Expected efficiency	η	0.8	

allows to calculate the maximum allowed modulation index, that can also be determined using Fig. 2. A 0.64 value is obtained. It is important to observe that, again from Fig. 2, a minimum current control angle of about 120° is expected, which can be considered acceptable to get a sufficiently low input current harmonic distortion.

B. Converter design

Based on an estimated efficiency of about 80% the average input power absorbed from the grid is about 6.25 kW. Therefore the expected input current is about 27 A_{RMS}. To limit the peak to peak current ripple ΔI_{Lpp} to about 20% of the peak input current a suitable value for the input inductor can be selected according to the following equation:

$$L = \frac{U_{dc}}{4 \cdot f_{sw} \cdot \Delta I_{Lpp}} \tag{6}$$

Equation (6) is derived calculating, based on (2) and (3), the maximum of the input current ripple as a function of the instantaneous line angle θ. In our design, a value of 1 mH was selected.

As far as the dc link filter capacitor is concerned, the selection of its value can be made imposing a suitable voltage ripple across it. As in any PFC, the dc link capacitor works as an energy tank supplying power to the load when the pulsating input power is lower than the power required by load and accumulating energy when the input power exceeds the output demand. This power exchange determines a voltage fluctuation at twice the line frequency, whose amplitude is directly determined by the size of the filter capacitor. Considering an instantaneous power balance, the following equation can be derived:

$$C = \frac{I_{inv\_dc}}{2 \cdot \pi \cdot f_{line} \cdot \Delta U_{dcpp}}, \tag{7}$$

which relates the capacitor value to the desired peak to peak voltage ripple. Current I_{inv_dc} represent the average inverter current needed to produce the required output power and the losses. In our case, a voltage ripple lower than 10% of the

nominal U_{dc} value is desired, which requires a capacitor value of about 800 μF. We note that the capacitor current due to the low frequency ripple turns out to be about 9 A_{RMS}, which seems to be an acceptable value.

As far as switches and diodes are concerned, it is only required to estimate the current stress, since the voltage stress is evident from the schematic of Fig. 1 and is equal to U_{dc} for each device. The current stress of the upper switches is only due to the load current and is therefore lower than the lower switches' stress. For the lower switches, the input current add to the load current, determining the required rating of the devices. To give an example, in our design, which assumes a unity transformer turns ratio, the switches need to be rated for a maximum peak current of about 65 A.

The design of the output side of the converter is quite straightforward, since it is based on a conventional forward structure. Given the desired output voltage, the transformer turns ratio can be determined. The inductive-capacitive output filter, instead, can be designed considering the maximum allowed inductor current and output voltage ripples.

IV. Control Strategy

We propose now two different control strategies for the converter of Fig. 1, the former inherently analog and relatively simple to implement, the latter fully digital in nature and, for some aspects, more advantageous. It is worth noting that, in the following presentation, we consider in detail only the input current control and the modulation strategy, since the control of the output voltage and, possibly, current is completely conventional. This can be any kind of standard voltage mode or current mode control applicable to a forward converter. Note, however, that the dynamic variations of the modulation index of the converter M, defined in (1), which may be required by the output voltage control, may cause the input current controller's saturation, since this only operates during the load free-wheeling phase. In general, to cope with this situation, it is possible either to limit the variations of M, so as to preserve input current control, or to sacrifice the input current control in the presence of dynamic load variations, in the case output voltage regulation is considered more important. Anyway, in the following presentation we will not take into account the interaction between the two controllers, practically assuming the modulation index M to be a constant.

A. Analog control strategy

A possible analog control strategy for the converter can be based on a typical two-loop PFC control, with a customised PWM modulator. As usual, the outer loop controls the dc link voltage U_{dc} and determines the amplitude of the input current reference. This is obtained by multiplying the rectified line voltage and the U_{dc} voltage controller output. The inner regulator, instead, processes the line current error and

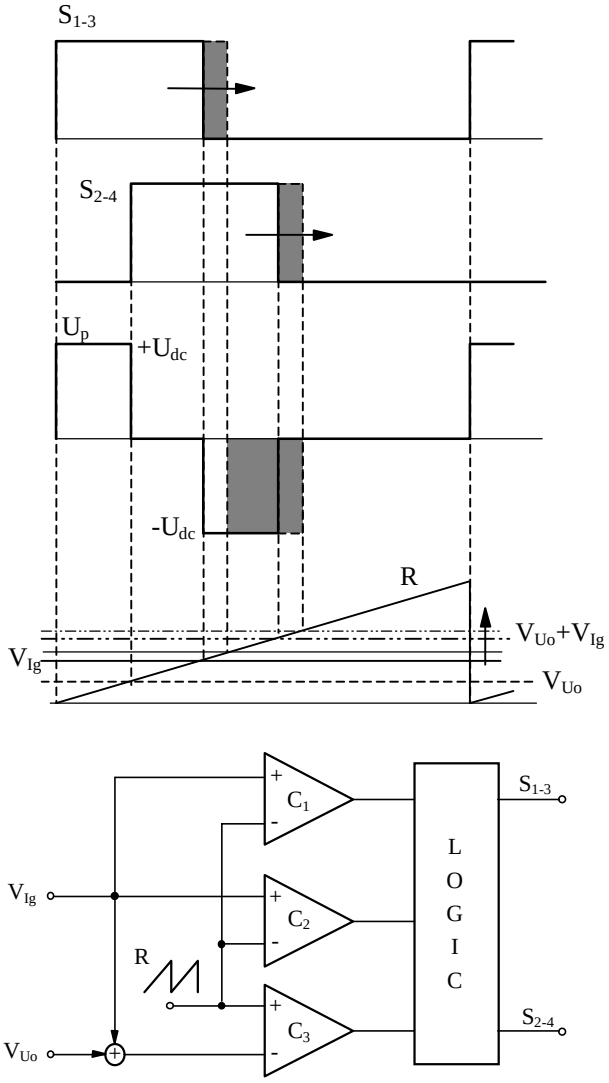

Fig. 3 – Scheme and operation of the analog PWM modulator for the proposed topology.

provides the input signal V_{Ig} for the modulator, whose operation is described by Fig 3.

The modulator is actually derived by modifying a conventional phase-shift PWM controller. The logic state of the inverter legs (variables $S_{1\text{-}3}$ and $S_{2\text{-}4}$) is determined by two PWM signals, phase-shifted proportionally to signal V_{Uo}, which is generated by the output voltage controller and, as previously said, is assumed to be constant in this analysis. The pulse width, instead, is independently adjusted proportionally to signal V_{Ig}, generated by the above described input current controller. This way, as shown in the upper part of Fig. 3, a three level voltage U_p is obtained, whose load powering phases have always equal durations, as required by the insulation transformer. The two free-wheeling phases instead, have, in general, different durations, as required by the input current control. In particular, Fig. 3 shows the effect of a variation of signal V_{Ig}, which modifies the input current

duty-cycle δ, without affecting the modulation index M. Fig. 3 also shows a possible practical implementation, requiring only three comparators and simple logic circuitry.

This control strategy provides the minimum number of switch commutations, but presents an unsymmetry in the allocation of the powering phases within the modulation period. This implies an harmonic component at the modulation frequency on the load side inductor current, that could be eliminated if the powering phases were symmetrically located with respect to the half of the modulation period. In order to do this, a different modulator is needed and, moreover, additional switch commutations in each modulation period are unavoidable.

B. Digital control strategy

We focus now on a fully digital input current control strategy. As it was explained above, during the powering phases of the load, no control of the input current is possible. It will increase or decrease depending on which diagonal of the bridge is turned on and on the sign of the input voltage. The free-wheeling interval, instead, allows the control of the input current. The current controller has to select the duration of each of the two free-wheeling states of the converter so as to make the current track its reference.

A possible strategy to achieve this result, which is suited for a digital implementation by means of a microcontroller and dedicated PWM modulator exploits the following discrete-time equation:

$$i_g(k+1) - i_g(k) = U_g(k) \cdot \frac{T_{sw}}{L} + \\ -\left[\frac{M}{2} - \delta(k)\cdot(1-M)\right] \cdot U_{dc}(k) \cdot \frac{T_{sw}}{L} \quad (8)$$

which relates the duty-cycle of current control δ(k) to the input current variation in a modulation period, going from the generic instant $k \cdot T_{sw}$ to the following sampling instant $(k+1) \cdot T_{sw}$. Equation (8) assumes that all variables are sampled at the beginning of each modulation period. A predictive control law [8] can then be based on (8) and used to determine the value of δ(k+1), assuming that $i_g(k+2)$ is given by:

$$i_g(k+2) = g_{eq} \cdot U_g(k) , \quad (9)$$

where g_{eq} is the equivalent input conductance of the converter. This can be automatically adjusted by a simple regulator (typically of PI type) controlling the dc link voltage U_{dc}, again as in any PFC. It is worth noting that (9) assumes that the input voltage does not change significantly from a modulation period to the following so that $U_g(k) \cong U_g(k+1) \cong U_g(k+2)$. This hypothesis is normally verified, thanks to the high ratio between the input voltage frequency and the sampling (and modulation) frequency. The final control equation can be directly computed as follows:

$$\delta(k+1) = -\delta(k) - \left[g_{eq} \cdot U_g(k) - i_g(k)\right] \cdot \frac{L}{T_{sw} \cdot U_{dc} \cdot (1-M)} + \\ + \frac{2}{(1-M)\cdot U_{dc}} - \frac{M}{1-M} . \quad (10)$$

It is worth noting that, to avoid a division and further simplify the control algorithm, the variation of the dc link voltage $U_{dc}(k)$ has been neglected and its nominal value U_{dc} has been used as a constant factor in (10). This implied no particular worsening of the control performance, as it will be shown in section V. It is also worth noting that (10) allows to compute the duty-cycle δ for the modulation period following the one in which the calculations are performed. This means that a complete modulation period is the allowed computation time for the microprocessor implementing control equation (10). Moreover, being a dead-beat type of control, this technique guarantees an excellent dynamic performance; provided that all the parameters of (10) are exactly known, the controller is able to respond to variations of the current reference with a delay equal to two modulation periods [8], and so with minimum tracking error.

In order to avoid the necessity of a division, when the algorithm operates on a variable M instead that on a constant value as supposed by (10), the control equation can be re-written considering a new control variable for the input current which is defined as follows:

$$\gamma(k) = \left[1 - M(k)\right] \cdot \delta(k) . \quad (11)$$

The substitution of δ(k) with γ(k) greatly simplifies the control equation in the case of a variable M. Clearly, the control of the converter switches has now to be based on variable γ(k), which implies a proper organisation of the modulator.

A suitable PWM modulation strategy has been devised, which allows to properly operate the control of the load and

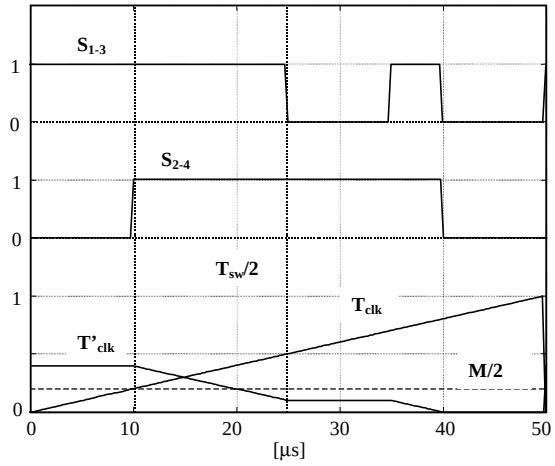

Fig. 4 – Operation of the digital PWM modulator. State of the inverter legs (S_{1-3} and S_{2-4}). Main counter T_{clk} and auxiliary counter T'_{clk}.

of the input current, once the modulation index M and the control variable γ are provided by the above described external controllers. Fig. 4 describes the modulation process showing the fundamental modulator variables that is: the logic state of each inverter leg, the counter implementing the main clock which defines the modulation period (T_{clk}) and the counter which implements the secondary clock (T'_{clk}), enabled only during the load free-wheeling phase. As can be seen, the modulation period begins turning on the bridge diagonal which forces a positive voltage on the load. The duration of this interval is $T_{sw}\cdot M/2$. Then, a free-wheeling phase for the load begins which forces on the input inductor a negative voltage. The duration of this phase is $T_{sw}\cdot\gamma$. The secondary counter is loaded with the γ value and starts its count-down at instant $T_{sw}\cdot M/2$. In case γ exceeds the duration on interval $T_{sw}/2\cdot(1-M)$, as in Fig. 3, the execution of the free-wheeling phase is suspended and the opposite load powering phase begins, at instant $T_{sw}/2$. Note that in this condition the secondary counter also suspends its count-down. After another interval of duration $T_{sw}\cdot M/2$, the execution of the interrupted free-wheeling phase is resumed in order to complete the period of duration $T_{sw}\cdot\gamma$, required by the input current control. When T'_{clk} gets to zero the first free-wheeling phase is over. To complete the modulation period, the opposite free-wheeling phase is activated, whose duration is clearly $T_{sw}\cdot(1-M-\gamma)$. Of course, this phase can be started before instant $T_{sw}/2$, in case γ does not exceed $T_{sw}/2\cdot(1-M)$ and T'_{clk} gets to zero before instant $T_{sw}/2$.

Another important feature of this modulator is that the logic states of the inverter legs are switched when the input voltage reverses ($S_{1\text{-}3}$ becomes $S_{2\text{-}4}$ and $S_{2\text{-}4}$ becomes $S_{1\text{-}3}$). This way it is possible to achieve a perfectly symmetrical input current ripple, minimising the low frequency input current distortion.

Clearly, this type of modulation scheme is not immediately available in any micro-controller. Therefore a micro-controller with a significant counter programmability has to be selected in order to implement this function. As an alternative, an FPGA based custom PWM modulator should be developed. The main advantage of this scheme is to allow the symmetrical allocation of the load powering phases with respect to the half of the modulation period, reducing the ripple on the output side current and voltage. As mentioned above, its main drawback is the increase in the number of switch commutations per period.

V. Simulation Results

The converter and the digital control strategy discussed so far have been tested by means of numerical simulations, performed in the Matlab© environment using the Simulink© tool. The main goals of the simulations are the verification of the design procedure and the test of the control strategy. The parameters of the simulated converter are the ones presented in Section III, and summed-up in Table III. Note also that a constant modulation index M = 0.4 was assumed in all the following simulations.

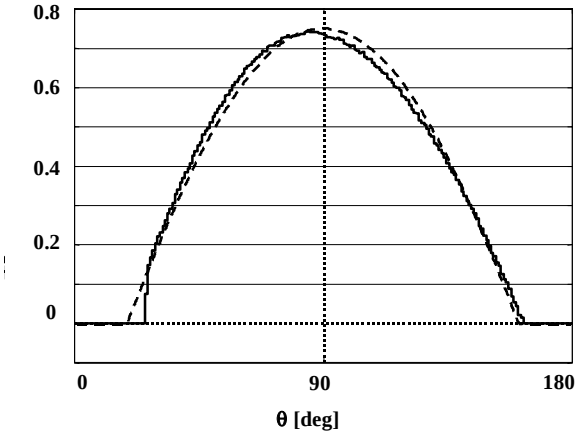

Fig. 5 – Comparison between the duty-cycle δ(θ) given by (3) (dashed line) and the actual $\delta_a(\theta)$ (solid line) determined by simulating the converter and its control.

Fig. 5 shows the comparison between the duty-cycle of current control δ(θ) as given by (3) and the actual $\delta_a(\theta)$ coming from the implementation of the proposed current control strategy. As can be seen, several differences between the theoretical and actual waveform can be noted. The distortion of the actual waveform is due both to the dc link voltage ripple and to the line frequency voltage drop across the input inductor L_f, which have been neglected in the derivation of (3). The step variation of $\delta_a(\theta)$ is due to the converter operation in discontinuous conduction mode (DCM) which has also been neglected in the derivation of (3). Practically, when current regulation becomes possible, the converter still operates in DCM, which keeps δ lower than the expected value. When the converter starts to operate in CCM the difference between the waveforms becomes very small. It is worth noting that there is not a similar step variation for δ_a when the converter re-enters the DCM close to 180°. Since the signal δ_a presents a practically constant slope, it seems to be following the ideal waveform. The current control angle is anyway quite close to the expected one as given by Fig. 2 for M = 0.4, i.e. slightly lower than 140°.

TABLE III – Converter Parameters

Line voltage	U_g	240 ± 10%	V_{RMS}
Output power	P_o	5	kW
Switching frequency	f_{sw}	20	kHz
Input inductor	L	1	mH
Dc link capacitor	C	800	μF

Fig. 6 shows the input current in line half period. It is possible to see that the instantaneous current ripple is limited to less of the 20% of the current peak value, as it was

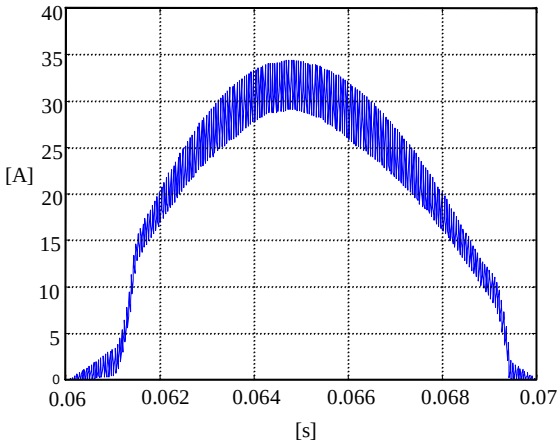

Fig. 6 – Input current in a line half-period.

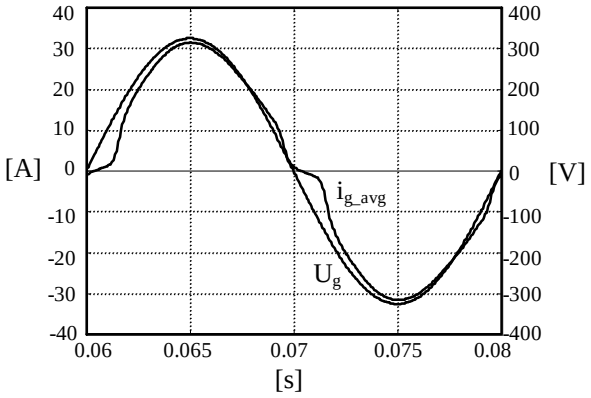

Fig. 7 – Filtered line current i_{g_avg} and line voltage U_g at nominal output power.

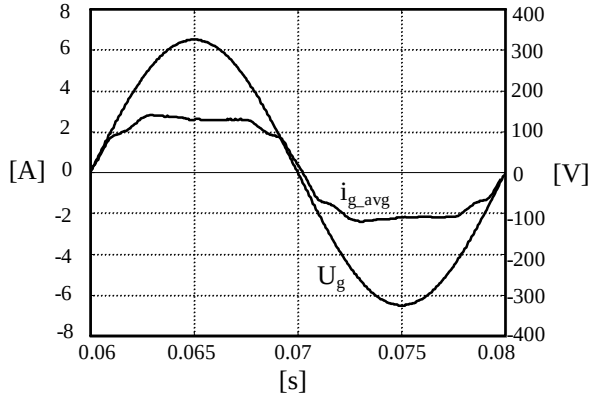

Fig. 8 – Filtered line current i_{g_avg} and line voltage U_g at reduced output power (10% of the nominal value).

expected. The suggested design procedure is therefore capable of providing the expected performance.

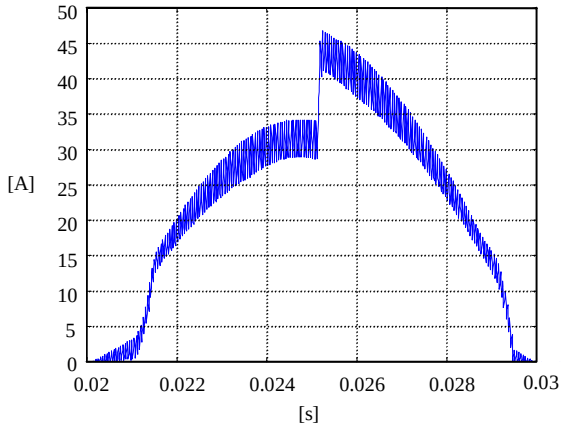

Fig. 9 – Line current control step response.

As far as the line side behaviour of the converter is concerned, Fig. 7 shows the average input current and the line voltage in a line period. The current total harmonic distortion (THD_I), calculated considering harmonic components up to 2 kHz, is about 8.9%. The power factor (PF) is practically unity (0.989). Clearly the converter is capable of complying with low-frequency EMC standards. The same waveforms are shown in Fig. 8 for operation at 10% of the nominal output power. This is very close to the theoretical minimum power (470 W) allowing the proper converter operation. In this case the THD_I turns out to be 17.96%, while PF is again practically unity (0.981). Only above this minimum load level the converter can be successfully controlled according to the strategy we described.

Finally, to describe the dynamic behaviour of the proposed predictive input current controller, we suppose that a step variation in the g_{eq} parameter of (9) is generated by the dc-link voltage controller. As shown by Fig. 9, the controller shows an excellent dynamic performance, rapidly increasing the input current amplitude and exhibiting no stability problems.

VI. Conclusions

The paper presented a new compact, integrated ac-dc converter. The topology integrates an high-quality rectifier, which is capable of providing high power factor and low distorted input currents in a wide load range, and a conventional full bridge inverter. The converter is described in detail, the structural limitations of its operation are highlighted and a design procedure is given. The paper then focuses on the converter control strategy, describing both a simple analog controller and a fully digital predictive control technique suitable for microcontroller or digital signal processor (DSP) implementation. In both cases a custom modulation strategy is proposed which allows simultaneous input current and output voltage control. Simulation results are described which validate the design procedure and illustrate the achievable converter performance.

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