Digitally-Controlled Single-Phase AC/DC Integrated PWM Converter

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***Abstract* - The paper presents the implementation of a fully digital controller for a boost type integrated AC/DC PWM converter. The considered converter has the following basic features: high power factor, full control of the output dc voltage, high-frequency line filter inductor and insulation transformer. Its main advantage is the complete integration of a rectifier and an inverter stage requiring only four IGBT's and six diodes. The converter is described in detail and the structural limitations of its operation are highlighted. The paper focuses on the converter control strategy describing in detail the implementation, by means of the TMS320F240 digital signal processor, of a fully digital predictive input current control technique. An application specific modulation strategy is also developed that allows simultaneous input current and output voltage control. The control system is finally tested on a 0.5 kVA laboratory converter prototype, so as to validate the design procedure and illustrate the achievable converter performance.**

I. INTRODUCTION

The industrial interest for compact AC/DC converter topologies integrating a high quality rectifier and a DC/DC or DC/AC stage is very high and has motivated several topology proposals, widely described in the literature [1]-[7]. Their goal is to obtain power factor correction and load voltage regulation while minimising the converter's component count, cost and size and increasing its efficiency. In general, the integration of the two stages constrains the achievable performance either on the load side or on the line side so that a limited control of the input current or of the output voltage must be accepted. This paper focuses on the integrated AC/DC PWM converter topology originally presented in [8]. It is aimed at providing experimental validation of the existing theoretical analysis and promising simulation results. Indeed, the considered converter is potentially capable of providing a high quality input current, fully compliant with EN 61000-3-2 low frequency EMC standard, and to guarantee a fast dynamic control of the load side voltage [8]. Therefore, based on the analysis and simulation results presented in [8], the paper briefly presents the converter operation and the basic design constraints. Then, a fully digital control strategy is considered to shape the input current. Its implementation with the TMS320F240 digital signal processor (DSP) is described in detail. The design procedure and the proposed control strategy are then experimentally tested on a 0.5 kVA laboratory prototype.

II. SYSTEM DESCRIPTION

A. Converter Scheme and Operating Modes

The basic scheme of the proposed converter is shown in Fig. 1. As can be seen, the converter employs four IGBT switches, which are arranged in a typical full-bridge inverter configuration, and six diodes. The two upper diodes (D_1 and D_2) are the free-wheeling diodes needed by the inductive load of the inverter, while the four lower diodes (D_{3a} to D_{4b}) act both as free-wheeling diodes and line current rectifiers. It must be noted that this topology also allows standard IGBT modules (comprising the free-wheeling diodes) to be adopted, provided that the four rectifier bridge diodes are externally added. Filter capacitor C_f ensures a constant dc voltage for

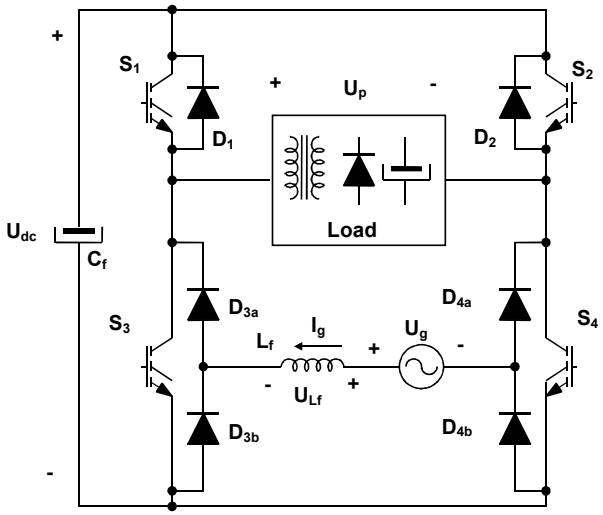


Fig. 1 – Converter basic scheme

the inverter operation. Generator U_g represents the line voltage, while input inductor L_f provides the necessary filtering action on the input current. Finally, the converter load, which is only schematically represented in Fig. 1, includes the insulation transformer, the rectifier stage and the inductive-capacitive filter needed to smooth the output voltage.

The converter operation is now explained assuming that a stable dc voltage U_{dc} is maintained across capacitor C_f all along the modulation period, that the input voltage U_g is positive and suitably lower than U_{dc} and that an almost unity power factor is achieved so that the line frequency harmonic component of the input current can be considered practically in phase with the input voltage U_g. In these conditions, the line current will flow through diodes D_{3a} and D_{4b} of the rectifier stage. When the diagonal S_1 - S_4 is turned on a positive voltage equal to U_{dc} is applied to the load, while a negative voltage (equal to U_g - U_{dc}) is applied to the input inductor. The line current I_g is therefore forced to decrease. When the opposite diagonal is turned on (S_2 - S_3), a negative voltage (-U_{dc}) is applied to the load while a positive voltage (equal to U_g) is applied to the input inductor. The input current is now forced to increase. These are the powering phases of the converter. Clearly, because of the transformer used the to isolate the load, the duration of these two phases in a modulation period must always be the same, so as to allow the magnetising current reset. By varying the duration of the powering phases it is possible to regulate the average value U_o of the rectified output voltage, in principle between 0 and U_{dc} (assuming a unity turns ratio for the transformer). Two free-wheeling phases are also possible, both imposing a zero voltage across the load: by turning on switches S_1 and S_2 a negative voltage is applied to the input inductor (equal to U_g - U_{dc}) which forces the input current to decrease, while, by turning on switches S_3 and S_4 a positive voltage (equal to U_g) is applied to the input inductor, which forces the input current to increase. As a consequence, control of the input current is possible during the free-wheeling phase of the load by properly selecting the switch combination (S_1 - S_2 or S_3 - S_4) to use. Of course, similar considerations are possible in the case of a negative input voltage U_g. Table I sums up all of the considered switch combinations, highlighting their effect on the transformer primary side voltage U_p and input current I_g.

B. Structural Constraints

The converter exhibits some structural constraints that limit its capability to fully control the input current waveform. As previously explained, the control of the input current only takes place during the free-wheeling phases of the load. This implies that, when the modulation index of the converter M, defined as the ratio between the average, in the modulation period, of the rectified output voltage U_o, and the DC link voltage U_{dc} (1), is close to unity, assuming again unity turn ratio for the transformer, very little time is available to control the input current.

$$M = \frac{U_o}{U_{dc}} \tag{1}$$

This implies that the input current can be successfully controlled and forced to be proportional to the input voltage only during a fraction of the line period. To better clarify this point we now consider the average inductor voltage as a function of the sinusoidal input voltage $U_g(\theta)$ and dc link voltage U_{dc}. The following equation (2), states that, in order to control the input current, it must be possible to force a zero

TABLE I – CONVERTER OPERATING MODES

Switches ON	Diodes ON	U_g	U_p	I_g
S_1-S_2	D_1, D_{3a}, D_{4b}	>0	0	decrease
S_1-S_2	D_2, D_{3b}, D_{4a}	<0	0	increase
S_3-S_4	D_{3a}, D_{4b}	>0	0	increase
S_3-S_4	D_{3b}, D_{4a}	<0	0	decrease
S_1-S_4	(D_1), D_{3a}, D_{4b}	>0	+U_{dc}	decrease
S_1-S_4	D_{3b}, D_{4a}	<0	+U_{dc}	decrease
S_2-S_3	D_{3a}, D_{4b}	>0	-U_{dc}	increase
S_2-S_3	(D_2), D_{3b}, D_{4a}	<0	-U_{dc}	increase

average voltage across the input inductor. Imposing this condition, we obtain:

$$U_{dc} \cdot [M/2 + \delta(\theta) \cdot (1 - M)] = \left|U_g(\theta)\right|, \tag{2}$$

where $\delta(\theta)$ represents the duty-cycle used in the input current control. The independent variable θ is the instantaneous line angle, equal to $2 \cdot \pi f_{line} \cdot t$, f_{line} being the line frequency and t the time variable.

Equation (2) implies that the duty-cycle $\delta(\theta)$, required to control the input current, has to satisfy the following conditions:

$$\begin{cases} \delta(\theta) = \dfrac{\dfrac{\left|U_g(\theta)\right|}{U_{dc}} - \dfrac{M}{2}}{1 - M} \\ 0 \le \delta(\theta) \le 1 \end{cases} \tag{3}$$

It is then possible to see that (3) can only be satisfied in the fraction of the line period when:

$$U_{gmin} < |U_g(\theta)| < U_{gmax}, \tag{4}$$

where U_{gmin} and U_{gmax} are given by the following relations:

$$\begin{aligned} U_{g\,min} &= \frac{M}{2} \cdot U_{dc} \\ U_{g\,max} &= \left(1 - \frac{M}{2}\right) \cdot U_{dc} \end{aligned} \tag{5}$$

Based on (2), (3), (4) and (5) Fig. 2 and Fig. 3 have been computed. Defining the input current control angle ϕ as the

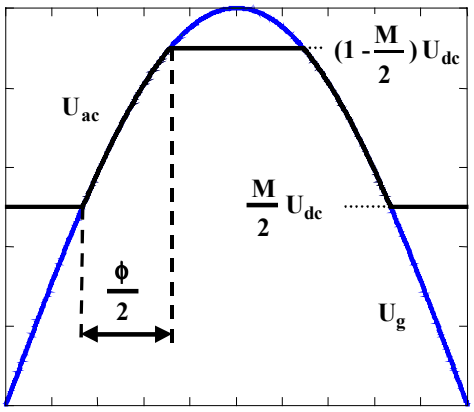


Fig. 2 – Converter's average input voltage U_{ac} and line voltage U_g. Current control is possible only within an angle ϕ of the line voltage half-period.

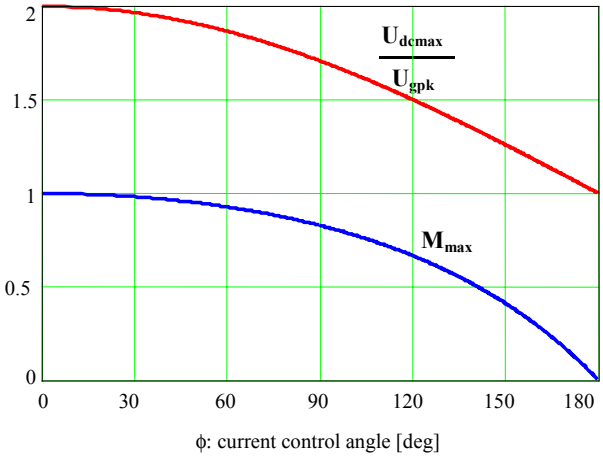


Fig. 3 – Upper trace: ratio between U_{dc} and line voltage peak value U_{gpk} as a function of the line control angle. Lower trace: maximum modulation index M_{max} as a function of the line control angle.

fraction of the line half-period where current control is possible (expressed in degrees), Fig. 2 shows the achievable average converter input voltage U_{ac} to underline the fact that current control is possible only when U_{ac} can be made equal to U_g, as stated by (2). Fig. 3 instead, shows two quantities as functions of ϕ. One is the maximum allowed converter modulation index M_{max}, while the other is the ratio between the maximum allowed dc link voltage U_{dcmax} and the line voltage peak value U_{gpk}, which ensures the largest control angle. Given the desired control angle, using Fig. 3 it is possible to determine what are the maximum modulation index M and dc link voltage U_{dc} compatible with that angle.

Fig. 3 also shows that it is not possible to achieve simultaneously an high modulation index M and the full control of the line current. Moreover, increasing the dc link voltage also implies a reduction of the current control angle.

When the input voltage does not satisfy (4), two situations are possible: if $|U_g(\theta)| < U_{gmin}$ (2) shows that the line current will be forced to decrease to zero and the converter will operate in discontinuous conduction mode at the input side. Instead, if $|U_g(\theta)| > U_{gmax}$ the input current amplitude will be forced to steadily increase. In both cases the line current waveform will significantly differ from the ideal sinusoidal waveform exhibiting a certain distortion. A careful design, anyway, allows to achieve a satisfactory line side behavior, as it will be shown in Section IV.

Finally, we must observe that, during each modulation period, one of the two load powering phases implies the absorption of power from the line. This means that the converter cannot operate in no-load conditions, because the power flow from the line to the converter in each modulation period cannot be reduced to zero and cannot be reversed, due to the presence of the input diode bridge. In other words, a minimum load must always be guaranteed to ensure the power balance. Moreover, when the output power gets close to the minimum level, the control of the input current is lost. Anyway, we verified that for our design, acceptable operation is possible down to 10% of the nominal output power [8].

III. Control Strategy and Implementation

The above described converter can be effectively controlled in a fully digital manner. Although analog control is also possible [8], we experimentally investigated only the digital approach, which is described in the following. The controller we developed includes a suitable PWM modulator, an input current controller, based on a predictive algorithm, and a DC link voltage PI regulator. It is worth noting that in the following presentation we consider in detail only the input current control and the modulation strategy, since the control of the output voltage and, possibly, current is completely conventional, provided that the filter capacitor C_f is large enough to exchange energy with the load without significant voltage variations. The output voltage control can be any kind of standard voltage mode or current mode control applicable to a forward converter. It is worth noting that the dynamic variations of the converter's modulation index M, defined in (1), which may be required by the output voltage control, may cause the input current controller's saturation, since this only operates during the load free-wheeling phase. This is not what happens in a conventional two stage power factor corrector (PFC), where the load side and line side controls are dynamically de-coupled. However, with our converter it is possible either to limit the variations of M, so as to preserve input current control, or to sacrifice the input current control in the presence of dynamic load variations, if output voltage regulation is considered more important. Anyway, in the following presentation we will not take into account the interaction between the two controllers, practically assuming the modulation index M to be a constant. In Section IV instead, step variations of the modulation index M will be discussed.

A. Input current predictive control strategy

We begin our discussion with the input current control strategy. As it was explained above, during the powering phases of the load, no control of the input current is possible. It will increase or decrease depending on which diagonal of the bridge is turned on and on the sign of the input voltage. The free-wheeling interval, instead, allows the control of the input current. The current controller has to select the duration of each of the two free-wheeling states in each modulation period of the converter so as to make the current track its reference.

A possible strategy to achieve this result, exploits the following discrete-time equation (9), which is directly derived from (2) by considering a zero-order hold discretization of the input current dynamic equation (8).

$$i_g(t) = \frac{1}{L_f} \cdot \int_0^t U_{Lf}(\tau) d\tau = \frac{1}{L_f} \cdot \int_0^t U_g(\tau) - U_{ac}(\tau)\, d\tau \qquad (8)$$

$$i_g(k+1) - i_g(k) = \\ = U_g(k) \cdot \frac{T_{sw}}{L_f} - \left[\frac{M}{2} - \delta(k) \cdot (1-M) \right] \cdot U_{dc}(k) \cdot \frac{T_{sw}}{L_f} \qquad (9)$$

Equation (9) relates the duty-cycle of current control $\delta(k)$ to the input current variation in a modulation period, going from the generic instant $k \cdot T_{sw}$ to the following sampling instant $(k+1) \cdot T_{sw}$. Equation (8) assumes that all variables are sampled at the beginning of each modulation period and that input voltage $U_g(\theta)$ is positive. Of course a similar equation can be written for the negative half-period of the input voltage. A predictive control law [8] can then be based on (9) and used to determine the value of $\delta(k+1)$, assuming that $i_g(k+2)$ is given by:

$$i_g(k+2) = g_{eq} \cdot U_g(k), \qquad (10)$$

where g_{eq} is the equivalent input conductance of the converter. In our implementation, as it will be explained in the following, this is automatically adjusted by a simple regulator (of PI type) controlling the dc link voltage U_{dc}, as in any conventional PFC. It is worth noting that (10) assumes that the input voltage does not change significantly from a modulation period to the following one so that $U_g(k) \cong U_g(k+1) \cong U_g(k+2)$. This hypothesis is normally verified, thanks to the high ratio between the sampling (and modulation) frequency and the input voltage frequency. The predictive control equation (11) can now be derived by substituting (10) into (9) computed one step forward, i.e. evaluated between instants $(k+1) \cdot T_{sw}$ and $(k+2) \cdot T_{sw}$, and solving for $\delta(k+1)$.

$$\delta(k+1) = -\delta(k) - \left[g_{eq} \cdot |U_g(k)| - |i_g(k)| \right] \cdot \frac{L_f}{T_{sw} \cdot U_{dc} \cdot (1-M)} + \\ + \frac{2 \cdot |U_g(k)|}{(1-M) \cdot U_{dc}} - \frac{M}{1-M}. \qquad (11)$$

It is important to underline that the absolute value for the input voltage sample $U_g(k)$ and input current sample $i_g(k)$ is introduced when the control equation for the positive half period and that for the negative one are combined to get (11). Equation (11) is thus valid for the whole line period and represents the actual input current control equation. Its physical interpretation is the following: $\delta(k+1)$ represents the duty-cycle required in the next modulation period to force the input current tracking error to zero, i.e. to get the input current to its reference in instant $(k+2) \cdot T_{sw}$. Of course, being the current reference a time varying signal, the tracking error will never get to zero; the average input current will lag its reference by a two sampling period delay. It is worth noting that, being essentially a dead-beat type of control, this technique guarantees an excellent dynamic performance; provided that all the parameters of (11) are exactly known, the controller is capable of replicating the current reference with a two cycle delay also in the presence of step variations or other transients.

It is finally worth noting that (11) inherently takes into account the computation delay of the microprocessor and the A/D conversion time. The output of the control equation refers in fact to the modulation period following the one when calculations are performed. This means that a complete modulation period is the maximum allowed time to sample and convert the input variables and to compute (11). As a consequence, being the computation time not so critical, the solution is attractive also for a medium level microcontroller implementation, especially once the control complexity is further reduced, as explained in the following.

B. Implementation related issues

Though theoretically correct, (11) is not so immediate to implement in a microprocessor. First of all, it is important to notice that its derivation is based on average quantities, i.e. the modulation process is totally neglected. To make the controller work properly, it is therefore necessary that the input variables in (11) represent the average value in the modulation period of the corresponding physical quantities. While this is inherently true for slowly varying quantities like U_g or U_{dc}, particular care must be taken for the input current i_g. In order to eliminate the current ripple and to sample only the average current value, synchronization is required between the modulation and sampling processes. By sampling the input current properly, filtering of the high frequency ripple can be avoided. It is possible to verify that with our modulation strategy, explained in the following section, sampling the input current at the beginning of each

modulation period inherently guarantees the required filtering action, but implies also a low frequency (namely the current reference frequency) error. This is compensated by the outer control loop.

Another problem concerning (11) is the presence of several input quantities as fraction denominators. The implementation of (11) would therefore require the execution of divisions, which are always computationally very heavy. Consequently, to avoid a division and further simplify the control algorithm, the variation of the dc link voltage $U_{dc}(k)$ has been neglected and its nominal value U_{dc} has been used as a constant factor in (11). This implied no particular worsening of the control performance, as it will be shown in Section IV.

Moreover, in order to avoid another division when the algorithm operates on a variable M instead that on a constant value as supposed by (11), the control equation can be re-written considering a new control variable for the input current which is defined as follows:

$$\gamma(k) = [1 - M(k)] \cdot \delta(k) . \tag{12}$$

This leads to the following modified control equation:

$$\gamma(k+1) = -\gamma(k) - \left[g_{eq} \cdot |U_g(k)| - |i_g(k)|\right] \cdot \frac{L_f}{T_{sw} \cdot U_{dc}} + \frac{2 \cdot |U_g(k)|}{U_{dc}} - M(k). \tag{13}$$

As can be seen, the substitution of $\delta(k)$ with $\gamma(k)$ greatly simplifies the control equation in the case of a variable M. Therefore, (13) has been used instead of (11) in our implementation. Clearly, the control of converter's switches has now to be based on variable $\gamma(k)$, which implies a proper organization of the modulator.

C. Pulse Width Modulator Implementation

A suitable PWM modulation strategy has been devised, which allows to properly operate the control of load voltage and input current, once the modulation index M and the control variable γ are provided by the above described external controllers. Fig. 4 describes the modulation process in dynamic conditions. The plotted variables are the logical states of the two inverter legs, from top to bottom $S_{1\text{-}3}$ and $S_{2\text{-}4}$ respectively. Fig. 4 shows the effect of a sudden change in the modulation index M, as could be required by the output voltage controller. As in any naturally sampled PWM process, we have an inherent one period delay (worst case) in the response of the modulator. In practice, the modulator updates the duration of the load powering phases at the beginning of the first modulation period following the step variation of the reference signal. Of course the duration of the two free-wheeling phases is also modified by the current controller to maintain the input current close to its reference.

In order to implement the modulator, we took advantage of the flexibility of the internal PWM modulator, provided by the selected hardware platform. We programmed three PWM

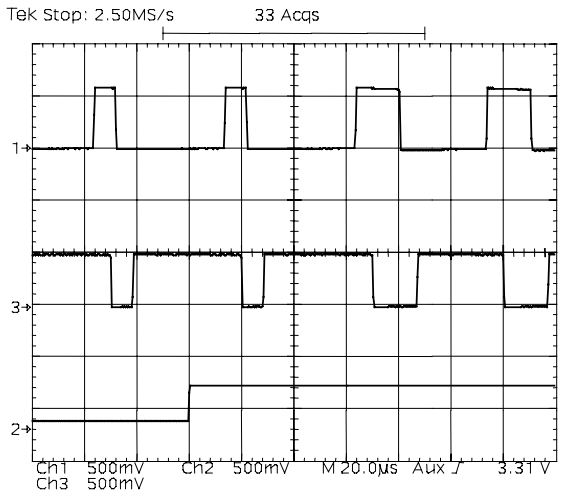


Fig. 4 – Operation of the digital PWM modulator.

compare registers, namely PWM1, PWM2 and PWM3 respectively with M(k), $\gamma(k) + M(k)$ and $\gamma(k) + 2M(k)$, immediately obtaining from the PWM2 output the logic state of inverter leg $S_{1\text{-}3}$. By AND-ing the negated PWM1 output (directly provided by the modulator) and the PWM3 output signal, we obtained also the logic state of leg $S_{2\text{-}4}$. This required only an external AND gate. It is worth noting that this organization of the modulator allows an easy synchronization of the input current sampling with modulation process. The interrupt generated by the period counter, associated with the modulator, can automatically be used to trigger the A/D conversion process with minimum delay. Moreover, the sequence of powering and free-wheeling phases implied by this organization, allows us to sample the current exactly at its valley, as can be verified with the help of Table I. This way, the high frequency ripple is filtered, but we have an error on the average current equal to a half of the current ripple amplitude. This is anyway inherently compensated by the outer voltage loop.

D. DC link voltage control

As already mentioned, in our controller the reference for the current control loop is derived, as in any PFC controller, by multiplying the input voltage samples and the output of a suitably designed DC link voltage controller. The idea is to absorb a current from the utility grid as proportional as possible to the line voltage, so as to maximize the power factor. The amplitude of the current reference has to be adjusted to balance the power flow through the converter. This is easily done by keeping the DC link voltage to a prescribed level. A simple PI regulator, whose design is straightforward, can achieve this result. The only point which is worth underlining is the need for a quite low regulator bandwidth, well below the line frequency. This is necessary to filter the DC link voltage ripple from the feedback signal and so to avoid input current distortion. In our implementation the

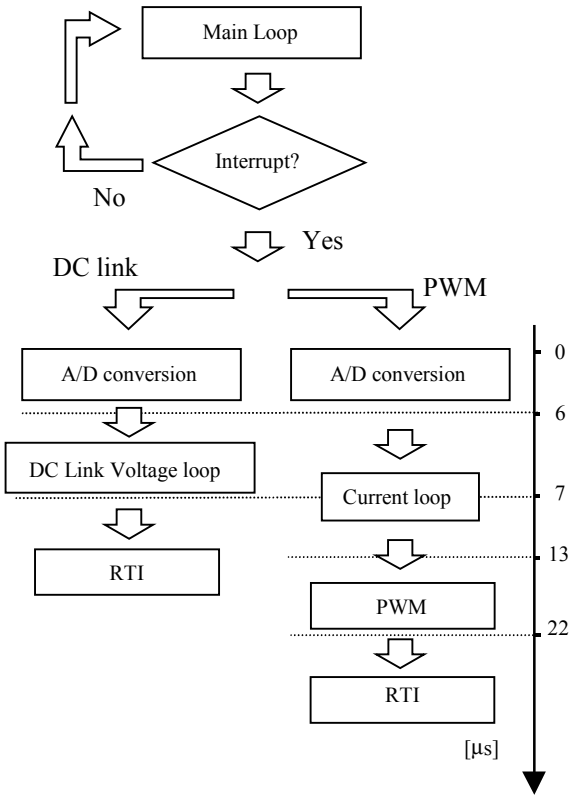


Fig. 5 – Flow chart of the control program

PI regulator was designed for a 10 Hz bandwidth and 60° phase margin. Given the reduced bandwith requirements the sampling frequency for this controller can be fairly low, allowing a considerable reduction of the computational effort.

IV. Experimental Measurements

The above described controller has been implemented using a TMS320F240 digital signal processor (DSP) by Texas Instruments. The device allowed us to implement the PWM modulator almost directly, offering significant counter programmability and a large number of independent PWM channels. In case of a less flexible architecture it is our opinion that a FPGA based custom modulator could be a good solution. The current control algorithm and the DC link voltage controller are implemented by an assembly program, whose flow-chart and timing are shown in Fig. 5. As can be seen, the control program is organized in two interrupt service routines. The DC link voltage control routine is performed at a reduced frequency, namely 1 kHz. It requires 7 µs, including A/D conversion. The PWM routine, including the line current controller, is instead executed at the modulation frequency, i.e. 20 kHz. This requires 22 µs, again including A/D conversion. As can be seen, the execution time of the routines is much smaller than the modulation period, so that the possible implementation of the output voltage controller would not represent a problem.

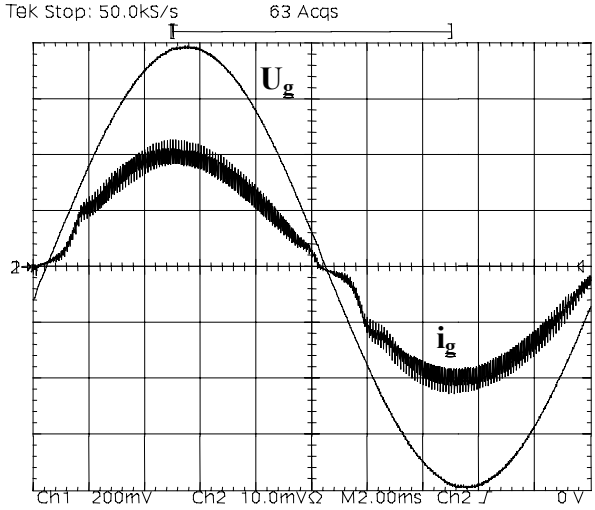


Fig. 6 – Input voltage U_g (40 V/div) and current i_g (2 A/div). Horizontal: 2 ms/div

Following the design procedure outlined in [8] and directly derivable from the discussion presented in Section II, a converter prototype was designed, whose main parameters are given in Table II. With a regulated DC link voltage of 250 V

TABLE II – Converter Parameters

Line voltage	U_g	110 ± 10%	V_{RMS}
Output power	P_o	0.5	kW
Switching frequency	f_{sw}	20	kHz
Input inductor	L	1.8	mH
Dc link capacitor	C	500	µF

and a 110 V_{RMS} input voltage the input current control angle is expected from Fig. 2 and Fig. 3 to be higher than 120°, so that a good power factor and THD are expected. The output

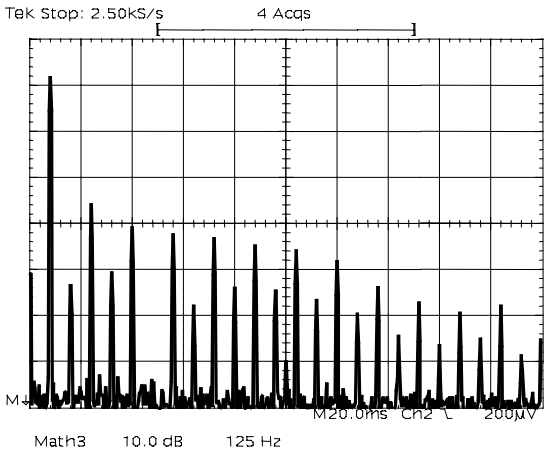
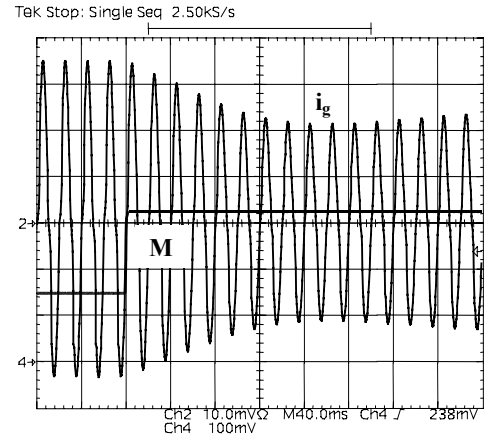
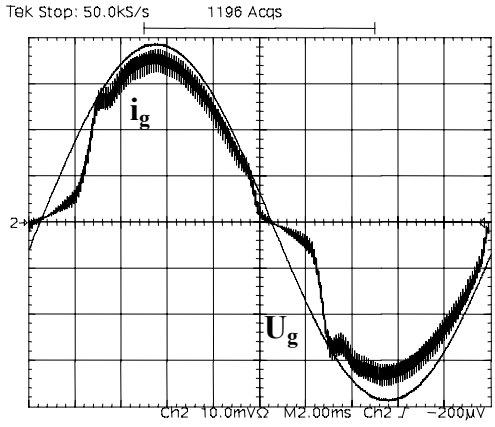


Fig. 7 – Input current i_g spectrum (10 dB/div). Horizontal: 125 Hz/div



a)



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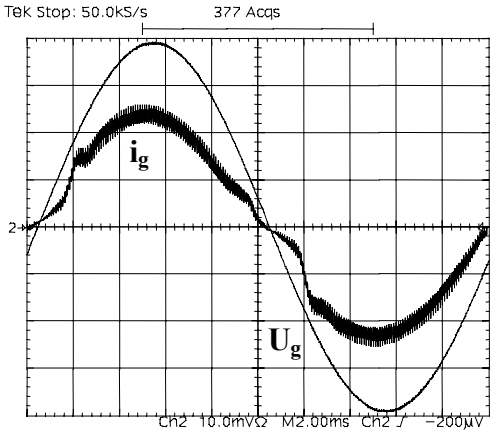

c)

Fig. 8 – a) Transient in the M parameter from 0.5 to 0.4. Input current i_g (2 A/div) and M signal. Horizontal: 40 ms/div b) Detail of the input current i_g (2 A/div) and input voltage U_g (40 V/div) with M = 0.5. Horizontal: 2 ms/div. c) Detail of the input current i_g (2 A/div) and input voltage U_g (40 V/div) with M = 0.4. Horizontal: 2 ms/div.

voltage was not regulated and a constant M = 0.3 was set for these experimental tests.

Fig. 6 shows the line side behavior of the converter, with an output power of 300 W. As can be seen the filtered current is close to be proportional to the input voltage. The input current THD, evaluated considering harmonic components up to order 20, is 15% in these conditions. The measured power factor is 0.98. As can be seen, the approximations made to simplify the controller implementation, as described in the previous section, do not affect stability and do not cause a significant error in the current waveform generation.

Fig. 7 shows the low frequency harmonic spectrum measured in the same conditions of Fig. 6. As can be seen the third harmonic is about 28 dB lower than the fundamental. A worse harmonic content can be encountered if the current control angle lowers. An example of the achievable current waveform can be seen in Fig. 8b, where the input power is almost at the nominal value. In that case, we estimated a THD value slightly lower than 35%, while the power factor remained above 0.96.

Fig. 8 shows the dynamic behavior of the control system in the presence of a step variation of the M value, from 0.5 to 0.4, which implies a variation of the converter's output voltage. As can be seen in Fig. 8a no stability problem is revealed, both in the current controller and in the DC link voltage controller. The transient determines a significant variation of the input current waveform. Reducing the M value widens the current controller operation angle, thus making the current waveform closer to an ideal sinusoid and improving the power factor. This can be noted comparing Fig. 8b and Fig. 8c, where the estimated THD varies from almost 35% to 25%. In addition, the output power decrease implied by the M variation, from 500 W to about 350 W, calls for the consequent reduction of the current reference amplitude, so as to balance the input-output power flow. This takes places according to the dynamic response of the DC link voltage controller, which is thus revealed, as if in the presence of a load change.

V. Conclusions

A compact, integrated ac-dc converter is discussed. The topology integrates an high-quality rectifier and a conventional full bridge inverter. The converter is described in detail, the structural limitations of its operation are highlighted and design criteria are derived. The paper focuses on the converter control strategy describing in detail the implementation, by means of the TMS320F240 digital signal processor, of a fully digital predictive controller for the input current and of a dedicated pulse width modulator. Experimental results are described, which validate the control strategy and illustrate the achievable converter performance.

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