Uninterruptible Power Supply Multiloop Control Employing Digital Predictive Voltage and Current Regulators

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***Abstract*—A digital control technique for the inverter stage of uninterruptible power supplies (UPSs) is described, which is based on voltage and current predictive regulators. Its aim is to achieve a deadbeat dynamic response for the controlled variables (output voltage and inverter current). The controller maintains the advantageous conventional multiloop structure and is capable of guaranteeing a high-quality dynamic performance. Moreover, its design is extremely simple and requires only a reasonably accurate knowledge of the output filter parameters. Finally, the only sensed variables are the output voltage and the converter output current. The validity of the proposed strategy is demonstrated by means of simulation and experimental results referring to a single-phase UPS laboratory prototype (1 kVA).**

***Index Terms*—Digital control, digital signal processor, uninterruptible power supply.**

I. Introduction

UNINTERRUPTIBLE power supplies (UPSs) are nowadays widely adopted for the protection of sensitive loads, like PCs or medical equipment, against line failures or other ac mains' perturbations. A large number of products, with different topologies and power ratings, are available on the market, making the UPS a quite mature product. As a consequence, the competition among the manufacturers is very high. The capability of guaranteeing a low level of voltage distortion in the presence of nonlinear and distorting loads, e.g., diode rectifiers with capacitive filters, represents a fundamental feature for this kind of product. The need for high dynamic performance and excellent static regulation of the load voltage has stimulated considerable research activity. Different control strategies have been identified to tackle the problem and can now be found in the literature [1]–[9]. On the one hand, digital control techniques based on the repetitive control concept [8], [9] or on discrete Fourier transform (DFT)-based harmonic elimination technique [7] have been shown to offer low distortion levels in the steady state, but also slow speed of response to dynamic variations of the operating conditions. On the other hand, digital techniques like deadbeat or predictive control schemes [1], [2], optimal state feedback [3], or sliding-mode control [4] have also been investigated, and their capability of providing a reduced level of distortion and a fast dynamic response has been demonstrated.

This paper focuses on a digital control technique based on predictive voltage and current controllers, suitable for application to single- and three-phase UPS systems. The approach maintains the advantages of conventional multiloop solutions [5], [6], e.g., the possibility of implementing an overcurrent protection for the power converter, but guarantees the high performance level typical of deadbeat controllers. This is the main property of the proposed controller, which guarantees significant advantages in terms of complexity and ease of design.

The first consequence of the controller's organization is that the voltage and current regulators have the same structure, which simplifies design and implementation. This result is achieved using, for the voltage regulator, a sampling frequency equal to half of the one used for the current loop. Thanks to this provision, both controllers have to compensate a system which consists of an integrator and a delay and, consequently, they can have the same structure. Moreover, the design of controller parameters can be directly derived from a rough knowledge of the converter's output filter parameters. The proposed solution, based on the output voltage and converter's output current sensing, i.e., without load current measurement, guarantees an excellent large-signal behavior and low harmonic distortion in the presence of a typical nonlinear load.

The validity of the approach is demonstrated by simulations and experimental tests performed on a single-phase UPS laboratory prototype (1 kVA). It is worth noting, however, that the control concept can also be applied to three-phase converters by means of the stationary frame (α–β) transformation. The digital control is implemented on a custom board employing an ADSP21062 floating-point digital signal processor (DSP), as the main processor, and an ADMC401 motion control DSP, as an interface with the power converter.

II. Control Technique

The continuous-time dynamic behavior of the second-order filter (Fig. 1) can be simply represented in the following matrix form:

$$\frac{d}{dt}x(t) = Ax(t) + B_1 v_m(t) + B_2 i_o(t) \tag{1}$$

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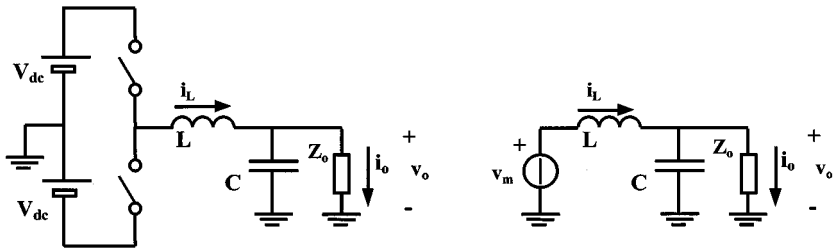

Fig. 1. Single-phase scheme of the UPS system. (a) Instantaneous. (b) Averaged.

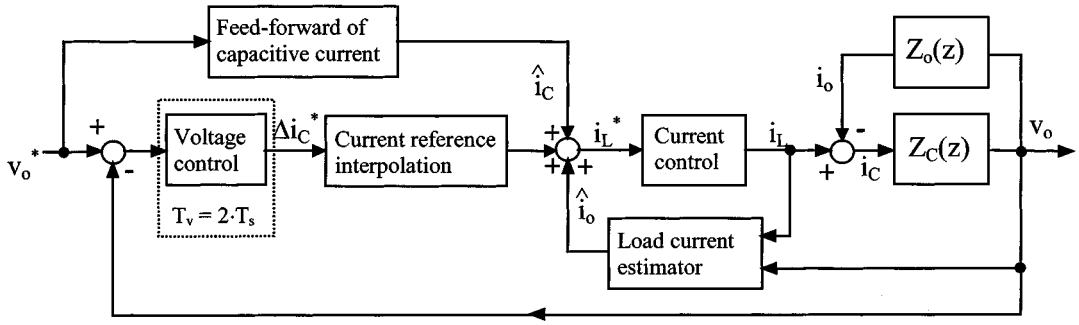

Fig. 2. Simplified control scheme. $ZC(z)$ is the discrete-time equivalent of the converter's intrinsic output impedance, due to the output filter capacitor.

where $x(t) = [v_o(t) i_L(t)]^T$ is the state vector, average inverter voltage $v_m(t)$ and output current $i_o(t)$ are considered system inputs, and

$$A = \begin{bmatrix} 0 & 1/C \\ -1/L & 0 \end{bmatrix} \quad B_1 = \begin{bmatrix} 0 \\ 1/L \end{bmatrix} \quad B_2 = \begin{bmatrix} -1/C \\ 0 \end{bmatrix}. \quad (2)$$

Assuming that the inverter voltage $v_m(t)$ and output current $i_o(t)$ are constant between sampling instants (zeroth-order-hold sampling of the system), the discrete-time dynamic equations can be written as

$$x(k+1) = \Phi x(k) + \Gamma_1 v_m(k) + \Gamma_2 i_o(k) \quad (3)$$

where

$$\Phi = e^{AT_s} = \begin{bmatrix} \cos(\omega_o T_s) & \frac{1}{\omega_o C}\sin(\omega_o T_s) \\ -\frac{1}{\omega_o L}\sin(\omega_o T_s) & \cos(\omega_o T_s) \end{bmatrix} \approx \begin{bmatrix} 1 & \frac{T_s}{C} \\ -\frac{T_s}{L} & 1 \end{bmatrix} \quad (4a)$$

$$\Gamma_1 = (e^{AT_s} - I_2)A^{-1}B_1 = \begin{bmatrix} 1-\cos(\omega_o T_s) \\ \frac{1}{\omega L}\sin(\omega_o T_s) \end{bmatrix} \approx \begin{bmatrix} 0 \\ \frac{T_s}{L} \end{bmatrix} \quad (4b)$$

$$\Gamma_2 = (e^{AT_s} - I_2)A^{-1}B_2 = \begin{bmatrix} -\frac{1}{\omega_o C}\sin(\omega_o T_s) \\ 1-\cos(\omega_o T_s) \end{bmatrix} \approx \begin{bmatrix} -\frac{T_s}{C} \\ 0 \end{bmatrix}. \quad (4c)$$

In (4), I_2 is the 2×2 identity matrix, T_s is the sampling period, and $\omega_o = \sqrt{1/LC}$ is the angular resonance frequency of the second-order L–C filter. Moreover, under the assumption that the sampling frequency $f_s = 1/T_s$ is much greater than the resonance frequency of the L–C filter (i.e., $\omega_o T_s \ll 1$), the approximations shown in (4) hold and, thus, the following discrete-time dynamic equations can be derived:

$$v_o(k+1) = v_o(k) + \frac{T_s}{C} \cdot [i_L(k) - i_o(k)] \quad (5a)$$

$$i_L(k+1) = i_L(k) + \frac{T_s}{L} \cdot [v_m(k) - v_o(k)]. \quad (5b)$$

Using (5), we developed a predictive control strategy with a typical multiloop structure where an internal current loop is controlled by an external voltage loop, as schematically represented in Fig. 2. It aims at achieving a deadbeat type of dynamic response from both the loops, as described in the following.

A. Current Loop

Firstly, we note that the assumption $\omega_o T_s \ll 1$ is verified when the output capacitive filter presents a negligible impedance with respect to the inductive one, at the control frequency. A possible physical interpretation of (5b) is that, in the system of Fig. 1, it is possible to consider the output voltage independent from the injected converter current. Thus, we neglect the second-order dynamics of the output L–C filter (Fig. 1) and consider only its inductive component. Doing this, the control algorithm ensuring a deadbeat response, as demonstrated in [10], can be written as

$$v_m(k+1) = \frac{L}{T_s} \cdot [i_L^*(k) - i_L(k)] - v_m(k) + v_o(k) + v_o(k+1) \quad (6)$$

where a sampling period equal to the modulation period T_s is assumed.

At the beginning of any switching period, e.g., at instant $k \cdot T_s$, the control system samples the inductor current $i_L(k)$ and the output voltage $v_o(k)$ and calculates, based on (6), the average

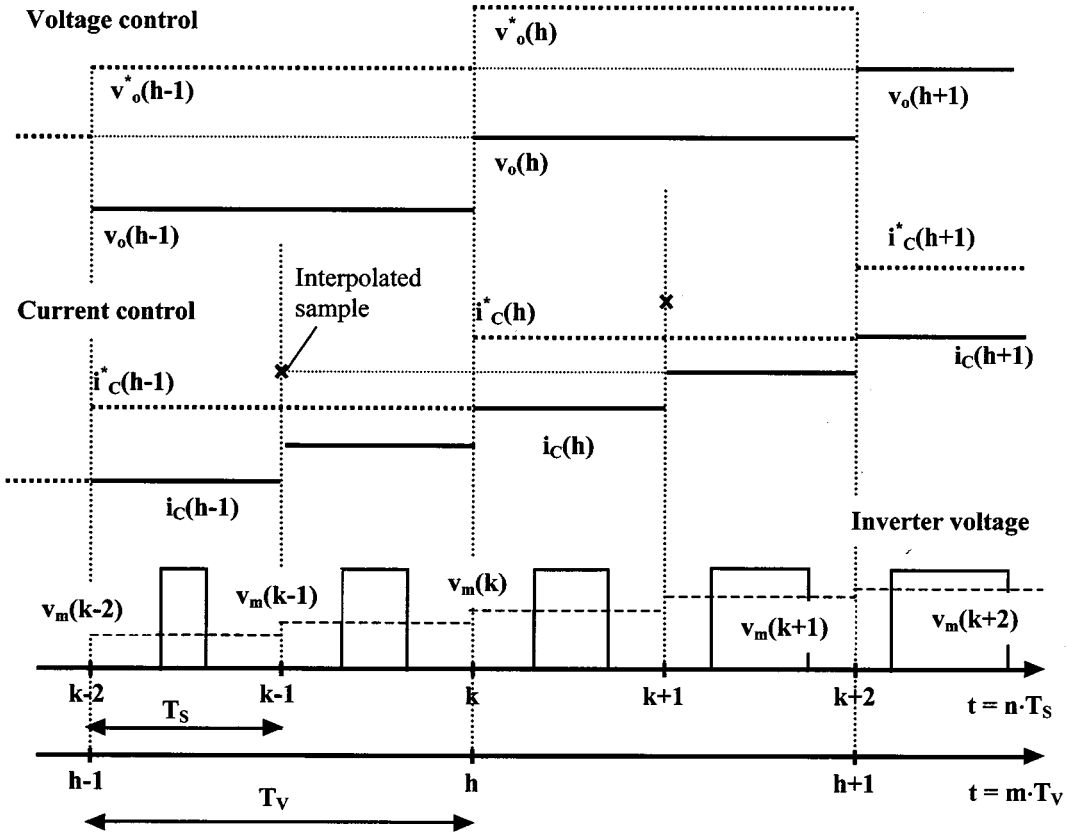

Fig. 3. Proposed digital control. From top to bottom: timing of voltage controller, current controller, and converter instantaneous and average output voltage.

output voltage $v_m(k+1)$ the inverter needs to generate in the following modulation period to make the current error $(i_L^*-i_L)$ go to zero at instant $(k+2)\cdot T_s$. A schematic of the control timing is given by Fig. 3. Clearly, the quantity $v_o(k+1)$ is not known to the control system at instant $k\cdot T_s$, but can be approximated in different ways (e.g., with a linear interpolation of previous samples). In this way, the control equation can be made causal and computable. The average voltage $v_m(k+1)$ will then be generated by a suitable modulation routine. Although Fig. 1 represents a single-phase system, the control strategy can be easily extended to a three-phase system by means of the usual (a, b, c) to (α, β) coordinate transformation. Because of the approximation of the output capacitor with an independent voltage source, the closed loop response of the system is not exactly deadbeat; in addition to the expected two-cycle delay directly implied by (6), the output current shows a residual error which depends on the output filter design and, in general, gets bigger when the resonance frequency of the output filter gets closer to the sampling frequency (e.g., when the output capacitor is decreased).

B. Voltage Loop

The same approach we described so far can also be applied to control the output voltage. Firstly, as shown in the scheme of Fig. 2, we operate the feedforward compensation of the component of the inductor current reference $i_L^*(k)$ related to the load current, $\hat{i}_o(k)$. This is computed by means of an estimator, which we will discuss in the following. Then, according to (5a), the discrete-time dynamic equation of the output voltage can be written as

$$\begin{aligned} v_o(k+2) &= v_o(k+1) + \frac{T_s}{C}\cdot i_C^*(k-1) \\ &= v_o(k) + \frac{T_s}{C}\cdot [i_C^*(k-2) + i_C^*(k-1)] \end{aligned} \tag{7}$$

where the closed-loop control of capacitor current i_C is assumed to be equivalent to a pure two-control-cycle delay [i.e., $i_C(k) = i_C^*(k-2)$]. Updating the voltage control at half the sampling frequency and imposing the reference current to be constant between sampling instants $k-2$ and k, we obtain

$$v_o(h+1) = v_o(h) + \frac{2T_s}{C}\cdot i_C^*(h-1) \tag{8}$$

where with h we denote the sampling instant at a half of the original sampling frequency. Then, we also operate (Fig. 2) the feedforward compensation of the capacitor current term $\hat{i}_C(k)$, which is straightforwardly derived from the output voltage reference. As a consequence, the control algorithm, which ensures a deadbeat response, is simply given by

$$\Delta i_C^*(h) = \frac{C}{2\cdot T_s}\cdot [v_o^*(h) - v_o(h)] - \Delta i_C^*(h-1) \tag{9}$$

where we substituted $i_C^*(h)$ with $\Delta i_C^*(h)$, which represents the correction of the current reference, with respect to the feedforwarded one. Note that (9) has the same structure as (6), where the disturbance components $v_o(k)$ and $v_o(k+1)$ have been set

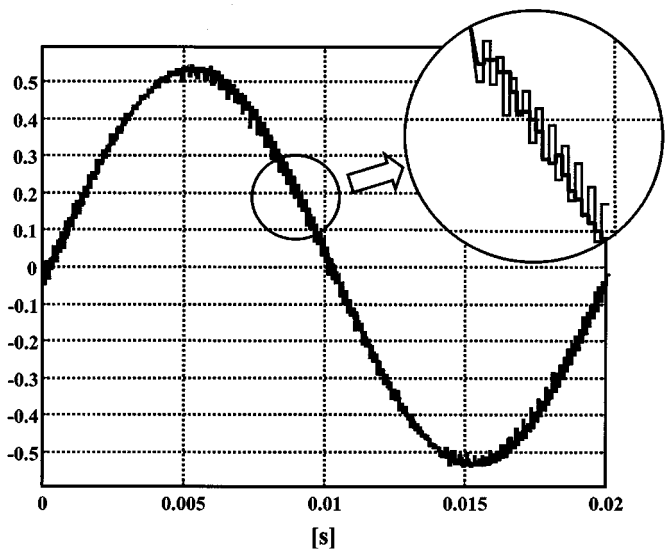

Fig. 4. Effect of interpolation on the current reference. Average converter output voltage (normalized to the dc-link voltage value), before and after (bold trace) the insertion of the interpolation routine.

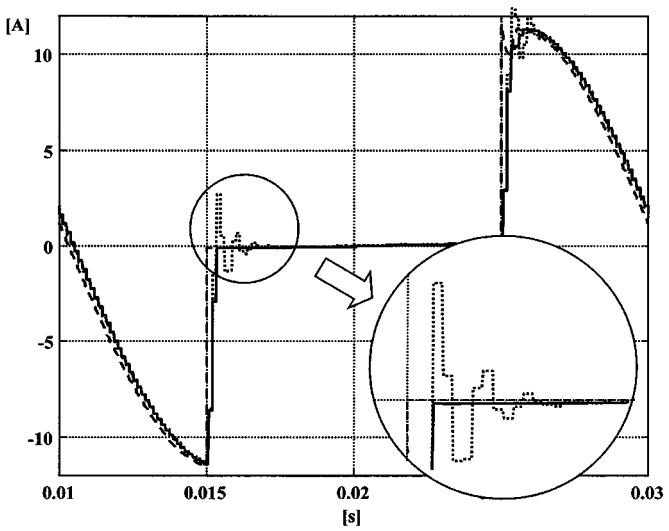

Fig. 5. Effect of integration method on load current estimation. Actual load current (dashed line), trapezoidal integration (solid line), and Euler integration (dotted line).

to zero. It is fundamental to underline that the control period T_v assumed for the predictive voltage controller is equal to *twice* the modulation period T_s, that is, double the current control period, whose reference is therefore updated only every two modulation periods. This avoids instabilities arising from the interaction between the internal current loop and the external voltage loop and, at the same time, gives us the highest possible speed of response. Again, since the current loop is not exactly a pure delay and the output current estimator dynamics are not totally negligible, the response of the voltage loop is not expected to be exactly deadbeat. Anyway, as we will show in the following, a very good approximation of the desired dynamic response is achieved, where the output voltage tracks the reference practically with only a four-cycle delay ($4 \cdot T_s$).

An important consequence of using half the sampling frequency on the external loop with respect to the internal one is that, from the internal loop standpoint, the variation of the current reference i_L^*, required by the voltage control is seen as a sequence of step reference variations. Therefore, a transient is started every time the current reference is updated. In order to smooth this transient, a very effective solution is to implement a linear interpolation of the current reference samples, to provide the internal loop with a reference closer to the ideal sinusoidal one. This is the aim of the interpolation block of Fig. 2, whose effect is described by Fig. 4. As can be seen, the control output v_m is much smoother when the interpolator is activated. The presence of the interpolator changes (8) as follows:

$$v_o(h+1) = v_o(h) + \frac{T_s}{C} \cdot \left[\frac{5}{2} i_C^*(h-1) - \frac{1}{2} i_C^*(h-2) \right]. \quad (10)$$

Accordingly, the deadbeat control algorithm is

$$\Delta i_C^*(h) = \frac{2}{5} \frac{C}{T_S} \cdot [v_o^*(h) - v_o(h)] - \frac{4}{5} \Delta i_C^*(h-1) + \frac{1}{5} \Delta i_C^*(h-2). \quad (11)$$

C. Load Current Estimator

An output current estimator ($\tilde{i}_o$) can be implemented considering the classical Luenberger structure. With only a slight deterioration of the control performance, this allows to avoid the load current sensing, while giving the well known advantages deriving from a full load current feed-forward compensation. By allocating the estimator eigenvalues in the origin (so as to get a deadbeat estimator) this simple derivative estimator equation can be obtained:

$$\tilde{i}_o(k-1) = -\frac{C}{T_S} \cdot [v_o(k) - v_o(k-1)] + i_L(k-1). \quad (12)$$

Actually, the structure of the estimator also includes a second-order low-pass filter. As a consequence, in the practical implementation, the estimation algorithm is followed by a moving average filter of order 4, whose finite-impulse response (FIR) behavior is highly preferable to that of classical infinite-impulse response (IIR) solutions. This finally generates the term $\hat{i}_o(k)$ appearing in Fig. 2.

Another important point concerning the implementation of the derivative estimator is the type of discretization algorithm to be used in the derivation of load current. This is given as the difference between the inductor current and the output capacitor current. Since the sampled inductor current exhibits linear variations during transients (being the integral of a stepwise varying voltage), a first-order-hold discretization seemed to us more suited to the physical behavior of the system. In order to highlight this point, we simulated the estimator basing the calculation of the inductor current both on a Euler integration method and on a trapezoidal (first-order hold) one. The results are shown in Fig. 5, in the case of a step load variation. It is possible to appreciate the better performance of the second solution.

III. Implementation Issues

A. Output L–C Filter Design

It is worth noting that the assumption we made to derive (6)–(11) is practically well verified, as long as the output filter

resonance frequency is sufficiently low ($\omega_o T_s \ll 1$) with respect to the sampling frequency, as shown in (2)–(5). Practically, we found that a ratio between the sampling frequency and the resonance frequency above 20 gives good results. In the case of a typical UPS design, where the output capacitor also serves as a partial reactive load compensator, this is typically verified.

B. Sensitivity to Noise and Accuracy of Regulation

The practical implementation of the controller requires some care in the conditioning of feedback control signals. Being an inherently wide-band controller, with a very quick speed of response, the controller is very sensitive to feedback noise and disturbances. For this reason, particular care must be taken in the controller layout definition. In case the noise level cannot be reduced enough or the control bandwidth has to be lowered for any other reason, we also considered the possibility of a different implementation of the voltage control loop. Equation (9) (or (11) if we consider the interpolation process) can be seen as a particular case of a more general controller structure, based on the estimation of the output voltage again by means of a deadbeat Luenberger estimator. In fact, considering the discrete-time equation (8) for the incremental terms

$$\Delta v_o(h+1) = \Delta v_o(h) + \frac{2T_s}{C} \cdot \Delta i_C^*(h-1) \qquad (13)$$

where $\Delta v_o(h) = v_o(h) - v_o^*(h)$, the control equation which ensures a deadbeat response is simply given by

$$\Delta i_C^*(h) = -\frac{C}{2T_S} \Delta \hat{v}_o(h+1) \qquad (14)$$

where $\Delta \hat{v}_o(h+1)$ can be estimated using the following Luenberger estimator:

$$\Delta \hat{v}_o(h+1) = \Delta \hat{v}_o(h) + \frac{2T_s}{C} \cdot \Delta i_C^*(h-1) + K_S\left(\Delta v_o(h) - \Delta \hat{v}_o(h)\right). \qquad (15)$$

When the estimator eigenvalue is allocated in the origin ($K_S = 1$), (9) is obtained. Instead, if the eigenvalue is allocated away from the origin ($K_S < 1$), a low-pass action is included in the controller, which practically "detunes" it with respect to the ideal deadbeat solution. This clearly reduces the speed of response, but also determines a lower sensitivity to control noise. Equations (13)–(15), reported here without the capacitor current interpolation, can be easily extended including the interpolation process.

As far as the accuracy of the regulation is concerned, we found that both inverter deadtime and dc-link voltage feedforward compensation play an important role. We used an offline deadtime compensation strategy based on the current reference zero crossings. This gave us an appreciable reduction of the total harmonic distortion (THD) (about 1%). Clearly, this result is totally dependent on our particular hardware, which required a relatively high deadtime (2 μs) for safe operation at 15 kHz. A different hardware, with shorter deadtimes, could take less benefit from this refinement.

The dc-link voltage compensation, instead, allowed us to reduce the tracking error on the output voltage fundamental component (especially its variation from light load to full load). Differently from the previous one, this provision is necessary because of the inherently limited low-frequency gain of our controller and is not related to any particular implementation aspect.

C. Robustness

Another important issue concerning the practical implementation of the proposed control algorithm is the estimation of its robustness against parameter mismatches. Due to the presence of two different sampling frequencies in the controller, the analytical evaluation of the robustness is quite complicated. Assuming that the inductive and capacitive part of the filter can be treated separately, which is fairly verified in the case we are considering, a separate robustness analysis can be performed for the voltage and current loop. As reported in [12], where only the current controller is considered, the robustness is quite high, and the controller tolerates parameter estimation errors up to 100% before going unstable. In our case, the situation is complicated by two factors: the two loops of the controller are not independent and the discretization we are using only approximates the exact system's behavior. We therefore expect a reduced robustness. In practice, we found that errors in the range of 20% for both the parameters do not cause severe stability problems in any load condition. Moreover, the system is more robust to underestimations than to overestimations of the filter parameters. This is extremely important in case capacitive loads are connected to the output. Being seen as underestimations of the capacitor value, they do not cause severe stability problems; however, the dynamic behavior of the controller is affected and a lower speed of response is achieved. It is worth noting that, as stated above, these results are achievable only if the inductive and capacitive part of the filter can be treated separately, i.e., if the current loop and voltage loop dynamics are sufficiently decoupled. This calls for a quite high ratio between the switching frequency and the filter resonance frequency. We practically verified that the stability robustness is adequate to the industrial standard only when this ratio is at least above 20. This may lead to oversizing the output capacitor, especially in the case of low-output-power applications.

D. Complexity

Finally, it is worth underlining that the controller we derived is practically very simple. Once the control and current estimation routines are implemented in a microcontroller (μC) or DSP, the design effort is reduced to zero, since only the output filter parameters have to be specified with the aforementioned accuracy. Moreover, the control complexity is fairly small too. As a comparison, we evaluated the execution time of this control algorithm and of a double proportional plus integral (PI) regulator (with antiwindup) on the same platform measuring a total time of 12 μs for the proposed control and of 8 μs for the conventional one. Note that the control code was written in C language with no particular optimization. The increment in the complexity is anyway limited to 50%. The control timing can be seen in Fig. 6. The implementation of the digital controller has been performed by means of the connection of two DSPs. An ADSP21062 floating-point DSP by Analog Devices has been connected through a dual-port RAM to an ADMC401, a fixed-point processor, by the same manufacturer. This gave us the possibility of minimizing the development time. Clearly, the

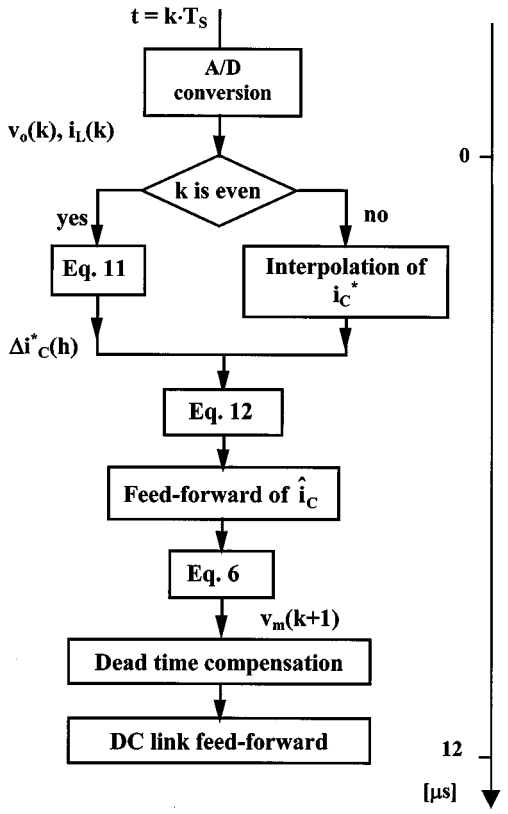

Fig. 6. Timing diagram of the proposed control algorithm.

TABLE I
EXPERIMENTAL PROTOTYPE'S PARAMETERS

Nominal output power	P_o	1	[kVA]
Nominal output voltage	V_{oRMS}	115	[V]
Minimum load DF	$\cos\phi$	0.8	
DC link voltage	V_{DC}	250	[V]
Output frequency	f_o	50	[Hz]
Output inductor	L	1.8	[mH]
Output capacitor	C	120	[μF]
Switching frequency	f_s	15	[kHz]

control complexity is perfectly compatible with the implementation on a less expensive μC unit. Further details concerning the implementation can be found in [11].

IV. EXPERIMENTAL RESULTS

The controller we propose has been extensively tested on a laboratory prototype of a single-phase UPS, whose basic parameters are given in Table I. Some of the results are now discussed. Figs. 7 and 8 describe the converter behavior when the nominal load is connected and then disconnected. As can be seen, the output voltage waveform exhibits only small deviations from the ideal sinusoidal waveform. This is due to the considerable tracking capability of the current reference; as can be seen in Fig. 7, the output current follows the reference at the maximum speed allowed by the power converter, reaching saturation. This can be seen in Fig. 8, where the average converter output voltage

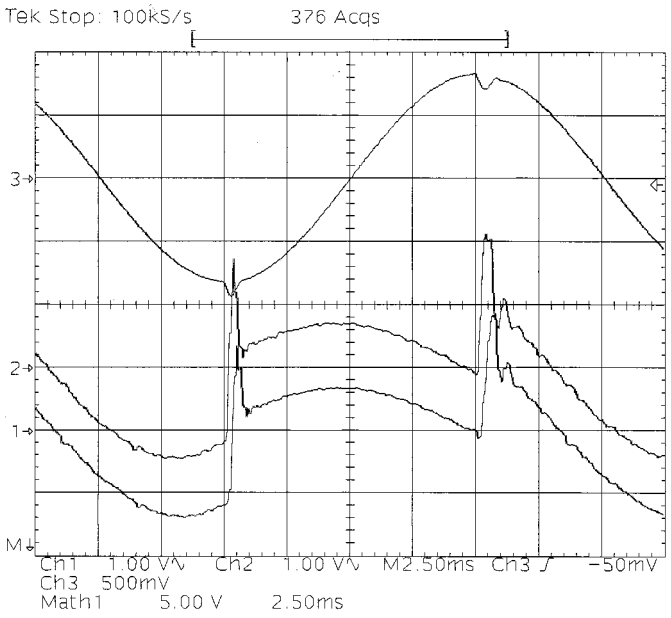

Fig. 7. Load step variations. Output voltage (channel 3) 100 V/div, current reference (channel 2) 10 A/div, and actual current (channel 1) 10 A/div; horizontal 2.5 ms/div.

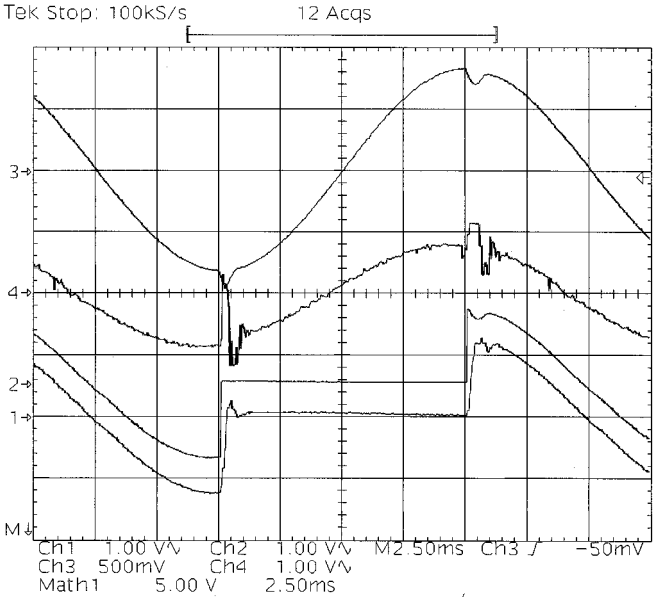

Fig. 8. Load step variations. Output voltage (channel 3) 100 V/div, inverter output voltage reference (channel 4) 200 V/div, actual load current (channel 2) 10 A/div, and estimated load current (channel 1) 10 A/div; horizontal 2.5 ms/div.

is shown. Fig. 8 also shows the dynamic behavior of the current estimator; as can be seen, the estimator guarantees a fairly good tracking of the actual load current waveform (which is sensed only to allow a comparison with the estimated one), with only a little delay and a very small transient in response to the step variations. This confirms the validity of the discussion of Section II-C.

A different situation is shown in Figs. 9 and 10, where the UPS behavior in the presence of a distorting load (diode bridge with capacitive filter: 470 μF filter and 25 Ω resistive load) is considered. Again, the results show good agreement with the

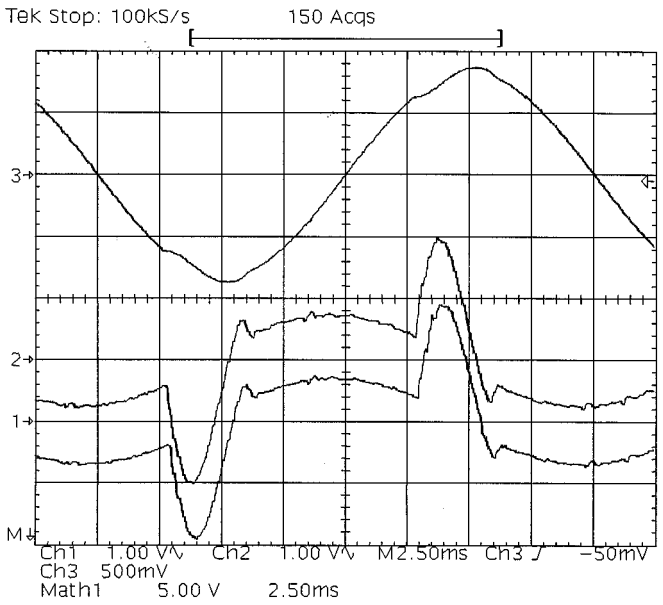

Fig. 9. Distorting load. Output voltage (channel 3) 100 V/div, current reference (channel 2) 10 A/div, and actual current (channel 1) 10 A/div; horizontal 2.5 ms/div.

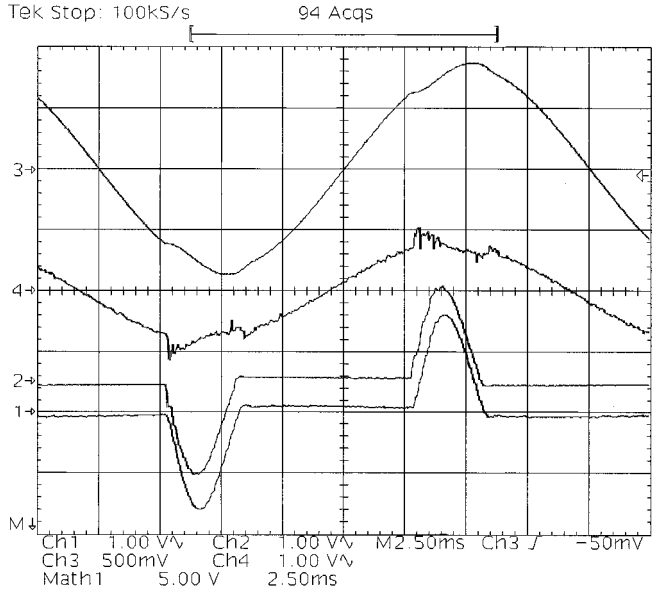

Fig. 10. Distorting load. Output voltage (channel 3) 100 V/div, inverter output voltage reference (channel 4) 200 V/div, actual load current (channel 2) 10 A/div, and estimated load current (channel 1) 10 A/div; horizontal 2.5 ms/div.

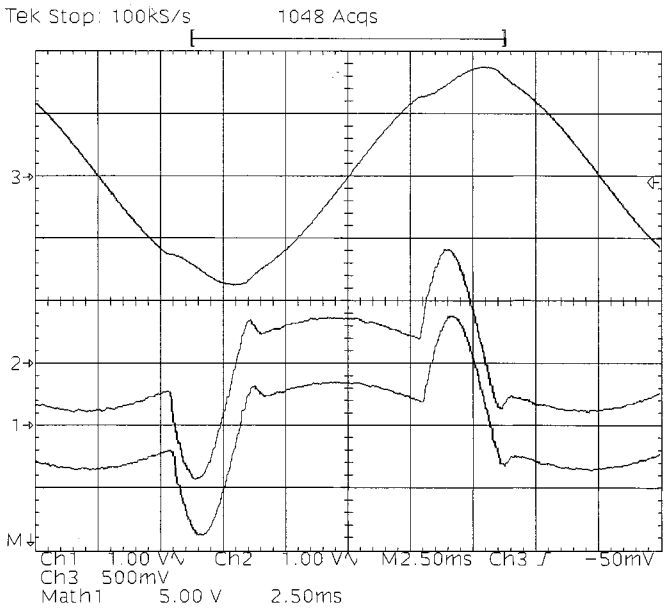

Fig. 11. Distorting load and "detuned" voltage controller. Output voltage (channel 3) 100 V/div, current reference (channel 2) 10 A/div, and actual current (channel 1) 10 A/div; horizontal 2.5 ms/div.

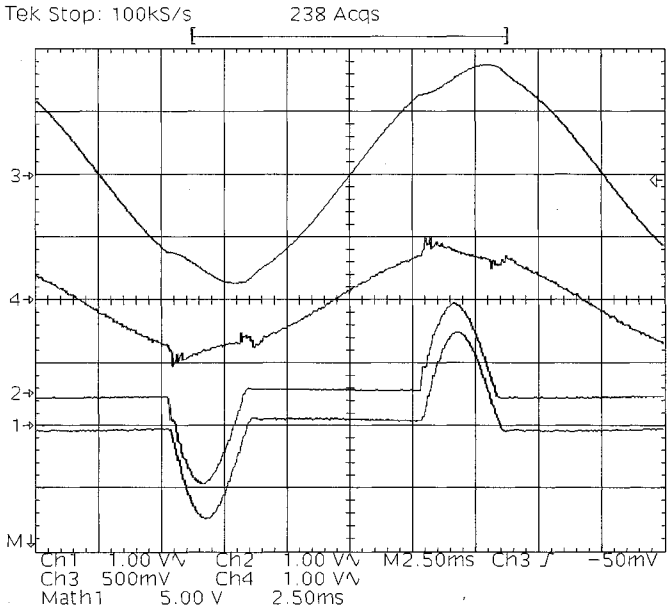

Fig. 12. Distorting load and "detuned" voltage controller. Output voltage (channel 3) 100 V/div, inverter output voltage reference (channel 4) 200 V/div, actual load current (channel 2) 10 A/div, and estimated load current (channel 1) 10 A/div; horizontal 2.5 ms/div.

theoretical analysis. The measured THD of the output voltage is 3.4%. Finally, it is worth adding that the implemented controller comprises all of the refinements discussed in Section II, such as the interpolation of the current reference, the compensation of deadtimes, and of the dc-link voltage variations.

Figs. 11 and 12 describe the effect of the detuning of the voltage controller, according to what has been discussed in Section III-B, in the case of the same distorting load considered in Fig. 9. The second real pole of the voltage controller, besides the one in the origin due to the deadbeat action, has been set to 4500 rad/s. As can be seen, the speed of response of the controller is reduced. It is clearly visible that the current and voltage waveforms are smoother (Fig. 11). The output impedance of the converter being somewhat higher with respect to the previous case, the voltage distortion induced by the distorting current is higher. This reduces the slope of the distorting current itself, whose peak is now lower and wider. As a result, the THD of the output voltage is now 3.8%. It is worth underlining that the advantage of the detuning is a better tolerance of noise and disturbances on the feedback signals, which may be required if the controller is used in a noisy environment.

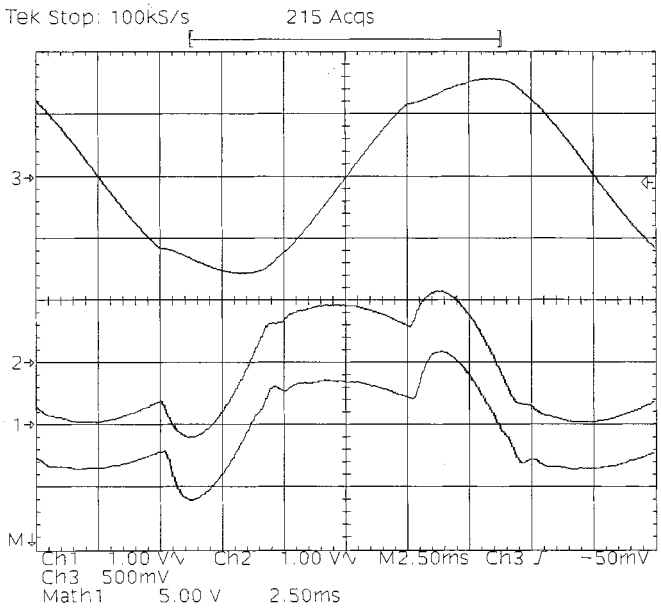

Fig. 13. Distorting load with PI control. Output voltage (channel 3) 100 V/div, current reference (channel 2) 10 A/div, and actual current (channel 1) 10 A/div; horizontal 2.5 ms/div.

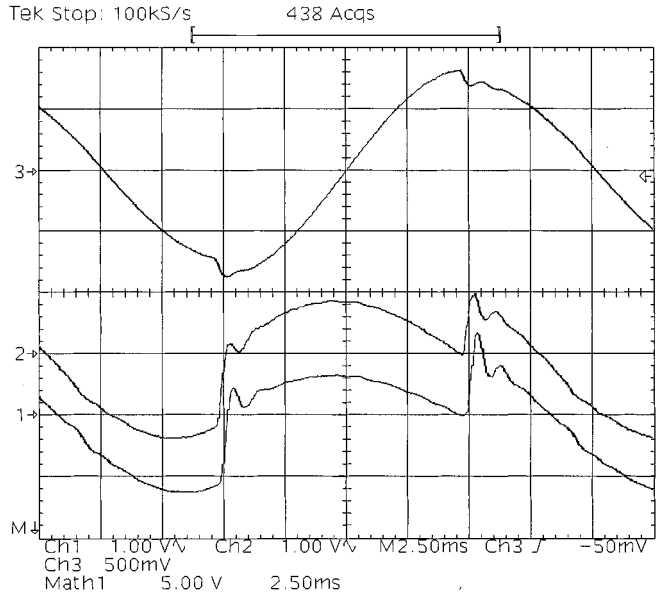

Fig. 14. Load step variations with PI control. Output voltage (channel 3) 100 V/div, current reference (channel 2) 10 A/div, and actual current (channel 1) 10 A/div; horizontal 2.5 ms/div.

Finally, in order to compare the performance of the proposed solution, we have implemented a conventional multiloop scheme where both the current and the voltage controllers are based on PI regulators. The bandwidth of the current loop was set to 7700 rad/s, with a 45° phase margin, while the bandwidth of the voltage loop was set to 3500 rad/s, with a 62° phase margin. Fig. 13 shows the results obtained with the same distorting load used for Fig. 9. As a result, the THD of the output voltage is now 6.0%. The superiority of our solution is also evident in Fig. 14, which reports the results obtained with load step variations and conventional multiloop PI control. Note that the transient response is now much slower, compared to that obtained in Figs. 7 and 8.

V. Conclusions

A digital control technique for voltage-source inverters with an L–C output filter has been presented, which is based on predictive current and voltage controllers. Based on approximated and, as a consequence, particularly simple control laws, the technique guarantees satisfactory small- and large-signal dynamic performance. In addition, it seems to be particularly easy to implement and tune, requiring only the knowledge of the output filter parameters. Various details concerning the controller structure have been considered and analyzed. Finally, the system's performance has been verified by simulation and experimental tests on a laboratory UPS prototype, basically confirming the theoretical analysis.

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