Effects of RFI and Underground Condition on PWM Current-Mode Integrated Circuits for SMPS

M. Citron ***massimiliano.citron@unipd.it***
M. Corradin michele.corradin@unipd.it
S. Buso simone@dei.unipd.it
G. Spiazzi giorgio.spiazzi@dei.unipd.it

Department of Electronics and Informatics – University of Padova
Via Gradenigo 6/a, 35131 Padova – ITALY
Phone: +39-049-827.7573

Topical area : Power Electronics

Subject area: EMC

Keywords:

- **emi**
- **rfi**
- **underground condition**
- **susceptibility**
- **integrated circuits**

Effects of RFI and Underground Condition on PWM Current-Mode Integrated Circuits for SMPS

M. Citron, M. Corradin, S. Buso, G. Spiazzi

Department of Electronics and Informatics – University of Padova
Via Gradenigo 6/a, 35131 Padova – ITALY
Phone: +39-049-827.7573
Email: massimiliano.citron@unipd.it

Abstract. The effects of a radio frequency conducted disturbing signal are evaluated on several pin-to-pin compatible control integrated circuits (IC) for PWM current-mode switching power supplies. The tested ICs were selected between some common models available on the market. The variations of the primary functional parameters (inner voltage reference, switching frequency, etc.) are investigated in conditions of different frequency and amplitude for the interfering signal. A dedicated PCB for the measurements was developed paying particular attention to HF layout. Also, the impact of underground condition (voltage at one pin below ground reference) on ICs' behaviour is analysed. The paper gives a comparative view of the results, focusing on the key macroscopic effects.

Effects of RFI and Underground Condition on PWM Current-Mode Integrated Circuits for SMPS

M. Citron, M. Corradin, S. Buso, G. Spiazzi

Department of Electronics and Informatics – University of Padova
Via Gradenigo 6/a, 35131 Padova – ITALY
Phone: +39-049-827.7573
Email: massimiliano.citron@unipd.it

***Abstract*. The effects of a radio frequency conducted disturbing signal are evaluated on several pin-to-pin compatible control integrated circuits (IC) for PWM current-mode switching power supplies. The tested ICs were selected between some common models available on the market. The variations of the primary functional parameters (inner voltage reference, switching frequency, etc.) are investigated in conditions of different frequency and amplitude for the interfering signal. A dedicated PCB for the measurements was developed paying particular attention to HF layout. Also, the impact of underground condition (voltage at one pin below ground reference) on ICs' behaviour is analysed. The paper gives a comparative view of the results, focusing on the key macroscopic effects.**

I. INTRODUCTION

It is well known that integrate circuit (IC) immunity to radio frequency interference (RFI) is a problem to be considered, due to rectification phenomena [1], parasitic effects, dc and ac crowding in the emitter region of a bipolar transistor [2]. The RFI coupled through the tracks of PCB to the IC pins can lead to bad operation of the IC, till the total degradation of the performance. For example, as shown in [3], operational amplifiers can exhibit a significant output voltage dc offset in the presence of RFI at the input. We have chosen six pin-to-pin compatible PWM current-mode ICs (of 3845 family), in order to do a comparative measure of the variations of the primary functional parameters in conditions of different frequency and amplitude interfering signals. In the analysis of the RFI effects on an IC, the first problem is to choose a coupling method between the pins and the source of RFI while maintaining a separation with the DC component [4]. Otherwise the RFI could run over the whole circuit, causing unacceptable and unpredictable effects in our case. An appropriate PCB test circuit, with bypass capacitors and blocking inductors, was developed, also guaranteeing a proper and stable point of operation for the switching IC. In fact, our goal is to disturb the IC while running in normal operating conditions. It is worth noting that the experimental set-up does not refer to any particular standard and thus only allows to compare the behaviour of the considered ICs in the same conditions. The tests are performed with RFI in a frequency range of 100÷800 MHz and amplitude of 115 dBμV.

A different experimental set-up is required for studying the underground condition. This phenomenon takes place at the output pin of a driver IC, normally connected to a MOSFET power switch. A fast falling voltage transient occurring at the drain can couple capacitively a current into the gate circuit. If the IC's output is in the low state (the power switch is not conducting), the forced gate-to-drain current can turn on the normally reverse biased isolation pn-junctions formed by the substrate of the IC and the different circuit wells (that's why it is recommended to connect Schottky clamping diodes very near the IC output). This pn-junction can also lead to problems of different nature [5]. In the experimental set-up the main problem is to generate a controlled underground condition, synchronous with the IC operation.

II. EXPERIMENTAL SET-UP

RFI susceptibility of very popular PWM current-mode controllers (3845 family) is considered in practical tests. Fig.1 shows the simplified block diagram of the IC.

The test circuit board is designed to set the IC in a stable operating point, similar to the real operating condition. Any deviation from this condition is supposed to be due to the RFI. Two points of injection for the RFI were considered, namely the supply voltage pin and the inverting input pin of the error amplifier. These are considered to be the noise inputs in any practical application, since they are normally connected to the switching converter power stage. Fig. 2 shows the test circuit for the V_{CC} pin noise injection. To obtain a current-mode operation, the voltage at pin I_{sense}

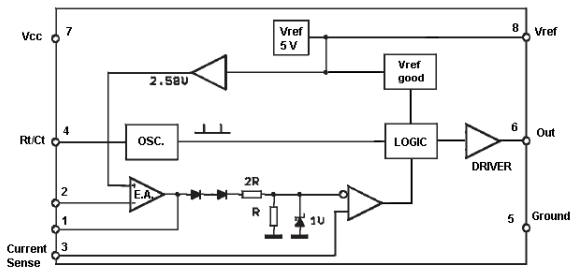

Fig. 1 - Simplified block diagram of the 3845 family ICs.

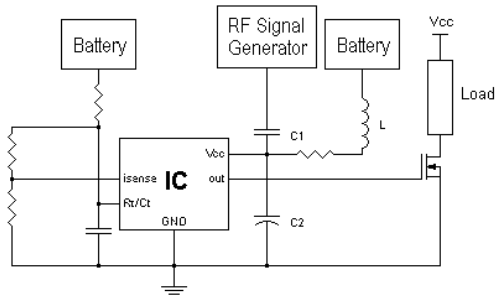

Fig. 2 – Schematic experimental set-up for RFI injection.

must be a triangular waveform, synchronised with the IC internal clock. This signal is derived from the IC ramp. Changing the value of the resistor divider can vary the output duty-cycle. C_1 and L are responsible for the AC-DC separation. To ensure enough blocking capability in a broad frequency range (i.e. 100÷800 MHz), L is formed by a series of six inductances with decreasing value (three with ferrite's core, three with ferrite's ring), so that a minimum impedance of 300 Ω is ensured in the whole frequency range. Supply voltage for the IC is obtained with a series of batteries, to avoid undesired RFI couplings that can occur with an external power supply. C_2 is a quite high value electrolytic capacitor, necessary to filter the impulsive currents drawn by the IC at switching frequency. We verified that, because of its equivalent series inductance, it behaves as a high impedance circuit at frequencies in the range of interest. Thanks to this behavior the RF interference voltage present at the supply pin was verified for all the devices to be only some dBµV (≤8 dBµV) below the nominal injected levels. The output of the IC is connected to a power MOSFET loaded by a clamped inductance to simulate real life conditions. By shorting pin 1 and pin 2, the error amplifier is set in a unity-gain buffer configuration.

Fig. 3 shows schematically the layout used for underground generation, in which the IC is still working on a stable operating point (the components for this purpose are the same as the previous case). Since it is common practice to connect a Schottky diode in parallel with the output to prevent underground, we also included it. There's no point in observing underground-effects without a diode that every expert designer will add. In this circuit we use the switching action of the power MOSFET to store energy in a magnetic core. During the off state of the MOSFET

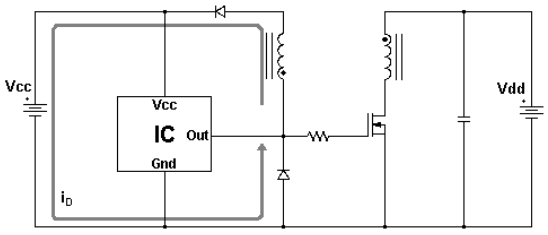

Fig. 3 – Schematic of the experimental set-up for underground generation.

this energy (like in a flyback converter) is sent to the secondary side of the transformer, where a current (i_D in Fig. 3) begins to circulate and turns on the Schottky diode and the IC isolating pn-junctions. Adjusting the value of V_{dd} it is possible to control i_D and modulate the underground amplitude and duration.

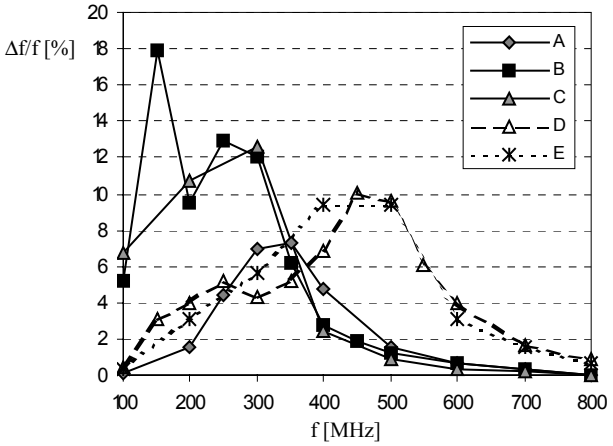

Fig. 4 – Frequency shift induced by RFI. Signal level=115dBµV. Nominal duty-cycle=30%.

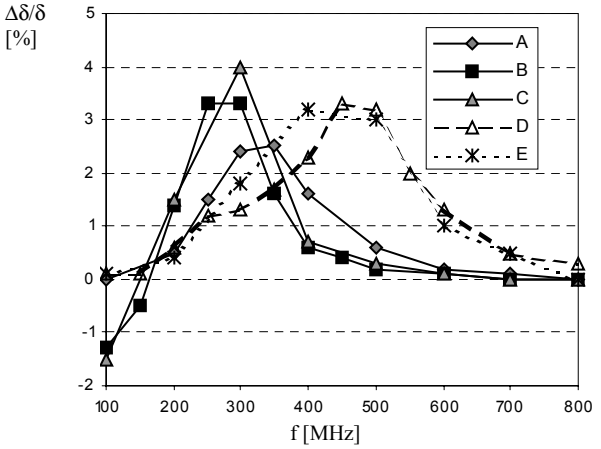

Fig. 5 – Duty-cycle shift induced by RFI. Signal level=115dBµV. Nominal duty-cycle=30%.

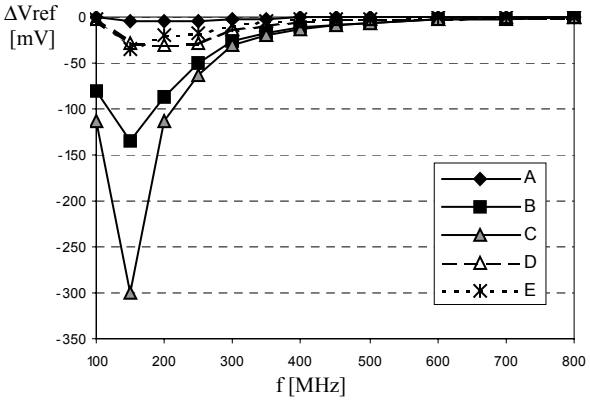

Fig. 6 – DC shift induced by RFI. Signal level=115dBµV. Nominal duty-cycle=30%. Nominal voltage=5.1V.

III. Experimental Results

We tested six different ICs. Thanks to their pin to pin compatibility, the test board was always the same. This permits to evidence the peculiar differences between their responses when submitted to the same operating and disturbed conditions. As explained before, two different injection points, the inverting input of the error amplifier and the voltage supply pin, were chosen. The main macroscopic effect in the former case, was a moderate frequency shift in the IC ramp. Possibly, the input capacitance of the IC shunted almost all the RF signal.

For injection in the supply pin, more interesting results were obtained. Fig. 4 presents the frequency deviation (nominal 32 kHz) for five models named from A to E. This fictitious names will correspond to the same component throughout the figures. Fig. 4 reveals that for this level of interference, an average deviation of +10% with respect to the nominal frequency can be obtained. For a specimen (B), almost +20% is reached. Measurements were performed at lower level (not reported here) from which an almost perfect proportionality can be inferred between RF level and IC response. Fig.5 shows absolute measured duty-cycle deviation, again for 115dBµV. From a nominal 30%, almost all ICs reach 4% of shift, i.e. the induced duty-cycle becomes 34%. In Fig. 6 the DC-shift of the inner voltage reference can be appreciated. Here component C shows a maximum decrease of 300mV with respect to a nominal value of 5.1V. It is interesting to note

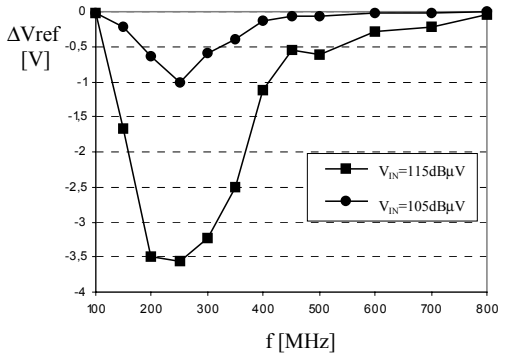

Fig. 7 – DC shift induced by RFI for component F.
Nominal duty-cycle=30%.
Nominal voltage=5.1V.

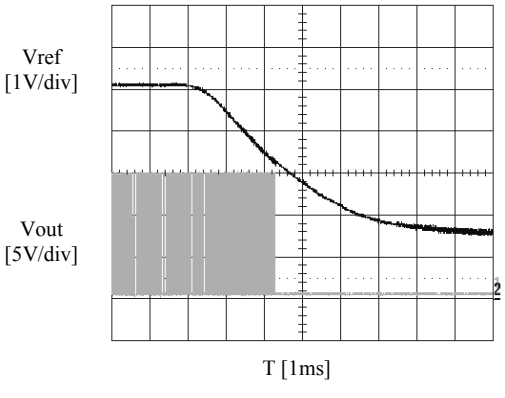

Fig. 8 – RFI effects on component F: decay of the voltage reference and stop of switching action.

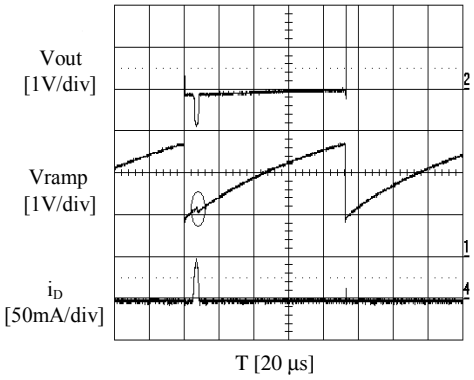

Fig. 9 – Vramp begins to show a discontinuity. From top to bottom: output pin voltage, ramp voltage, secondary side current pulse

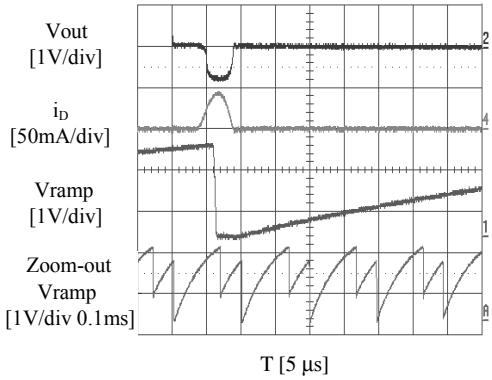

Fig. 10 – Vramp resets to zero due to underground effect (B and C type). 1) detail of voltage collapse, A) zoom-out track of the ramp voltage (a toggle flip flop sets the switching frequency to half the ramp frequency)

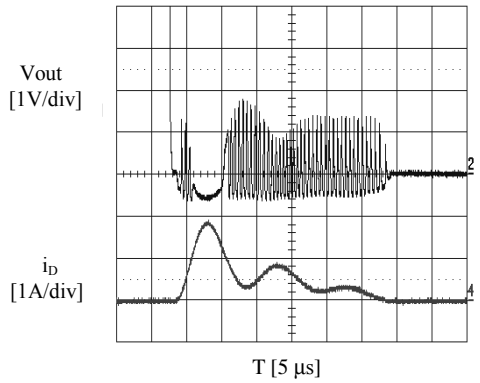

Fig. 11 – The A-type output for an i_D current-peak of nearly 2A

that the peak for the response remains the same only in the last case.

The results for component F were deliberately separated in two other figures. Fig. 7 isolates the DC shift for component F, which grows as high as –3.5V. Fig.8 explains the reason why component F does not appear in the previous graphics. For 115dBµV of injected signal the voltage reference collapses, falling to the point (nearly the internal 2.5V reference) at which the switching action stops. This is due to the intervention of block "Vref good" shown in Fig. 1.

As to underground effects, the results obtained with the circuit in Fig.3 indicate that the first effect in the operating point shows in the ramp generation block. This happens for all the ICs, except the F and A. It is decided to take i_D as a quality-reference since it determines the power delivered to the Schottky diode and the parasitic pn-junction of the IC. In Fig. 9 it can be seen that, for a certain level of the current i_D, the ramp signal begins to show negative spikes during the rising edge period. If the i_D current is made higher (Fig. 10), the ramp voltage collapses to zero and then starts to rise again. This effect makes the ramp-period increase and consequently the switching frequency and the duty-cycle change. The other pins do not show any change in their behaviour. The ICs differ for the threshold current-peak i_D at which the malfunction starts to appear: B and C have a threshold current-peak of 50mA, D and E of 500mA. The A-type presents deviations from its operating point only for a current-peak i_D of 2A. Anyway, at this high current level, a chaotic behaviour appears at its output (Fig. 11). It seems that the IC is trying to switch on the MOSFET, supplying the i_D current and pushing the output voltage toward the high-state.

The F-type shows again a particular behaviour (Fig. 12). For a peak-current i_D of 900 mA, the output of the error amplifier collapses forcing the output pin into the low state where it remains for more than 2 ms. It then starts to rise very slowly. The output starts to drive the MOSFET again, until a critical duty-cycle is reached and another reset occurs. The output of the error amplifier is directly connected to the inverting input, so apparently there is not any justification for such a long time-constant. For other considered ICs (3843 family, sixteen pins), not discussed here, a low value of the current-peak i_D, which triggers the malfunction, was found (~10 mA). Such a low current is normally able to occur in standard operating circuits.

IV. Conclusions

It is shown that interference superimposed on the power supply voltage induces a dc shift offset in the Vref, which can lead to black-out an IC (F case), and a significant deviation of frequency and duty-cycle with respect to the nominal values.

In the underground condition test there are differences among ICs for the threshold-value of the secondary side current i_D. The investigation has shown that the IC block more sensitive for this type of disturb is the ramp generation.

Future studies will be devoted to experimental research of the magnitude and frequency of interference that can couple with ICs in normal operating condition. This in order to understand how much the type of malfunction shown in this paper can occur in real-life operation.

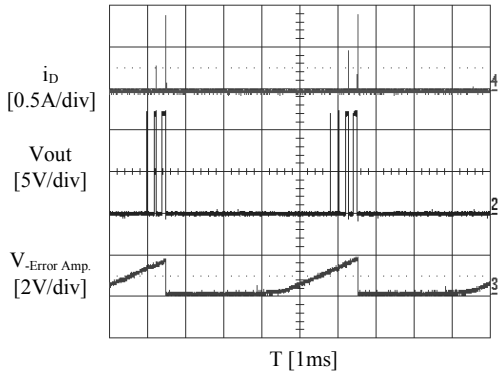

Fig. 12 – The F-type presents a blackout in the error-amplifier block that disables the circuit for a long time.

References

[1] Robert E. Richardson, Vincent G. Puglielli, Robert A: Amadori, "Microwave Interference Effect in Bipolar Transistor", IEEE Trans. On Electromagnetic Compatibility, Vol. 17, No. 4, November, 1975, pp. 261-219

[2] Robert E. Richardson, "Quiescent Operating Point Shift in Bipolar Transistors with AC Excitation", IEEE Journal of Solid-State Circuits, Vol. 14, No. 6, December, 1979.

[3] G. Masetti, G. Setti, N. Speciale, "On the key role of parasitic capacitances in the determination of the susceptibility to EMI of integrated opearational amplifiers", IEEE International Symposium on EMC, Zurich, 1999, pp. 625-630.

[4] D. Florean, M. Pinelli, P. Tommasin, " Analysis of RFI Effects in Voltage Regulator IC's: Mesurament Techniques Picking Capability Prediction and Protection Methods" IEEE International Symposium on EMC, 2000, Washington DC, Vol. 1, pp 391-395.

[5] F. Fiori, "Prediction of RF interference effects in smart power integrated circuits**",**. IEEE International Symposium on EMC, 2000, Vol. 1, pp. 345 -347.