Cost effective PFC with VIPower smart ICs for lamp ballast applications

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ABSTRACT - The paper introduces a very simple and cost effective active PFC circuit mainly for lighting applications. However, it is suitable for any other application with constant output power. The converter is based on a DCM Boost topology using VKXX devices, a new family of smart power IC from STMicroelectronics. The smart device uses proprietary VIPower technology to integrate a monolithic emitter switching power device, the driver and some protections.
Thanks to the features of such devices, the component count of the PFC is low requiring only an external capacitor.
Finally, design guidelines and performance evaluation are given, confirming the suitability of STMicroelectronics VKXX for low cost active PFC in lighting applications.

1. Introduction

Since January 2001 the European standard EN61000-3-2 on harmonics has to be applied to all electronic equipment drawing less than 16A per phase in order to get the CE mark [1]. The purpose of the standard is to limit the harmonic pollution so as to improve the efficiency of the distribution system. Harmonic pollution means poor Power Factor and high THD. A typical polluting circuit in power electronics is the input diode rectifier with capacitive filter. Several techniques can be used to reduce low frequency pollution either passive or active, but a special effort has to be done to find out a compliant solution with minimum cost and size.

In this paper a very simple and cost effective active solution is introduced in lighting applications using VK05, a smart power IC from STMicroelectronics. It has been specifically developed for half bridge lamp ballast circuit and is based on proprietary VIPower technology that integrates a monolithic power BJT and MOSFET in the emitter switching (cascode) configuration. The internal structure of such a device is shown in Fig. 1. It features five external connections and is housed in SO-8 package, performing well in terms of size and thermal management. Three control pins are given: "*diac*" for the start-up of the electronic ballast, "*sec*" for synchronous switching of the self driven half bridge and "*osc*" for frequency setting. The power stage consists in a high voltage power BJT with BV_{ces}=600V and I_C=400mA, and a low voltage Power MOSFET with Vds=60V. The advantages of such a configuration is well known [1].

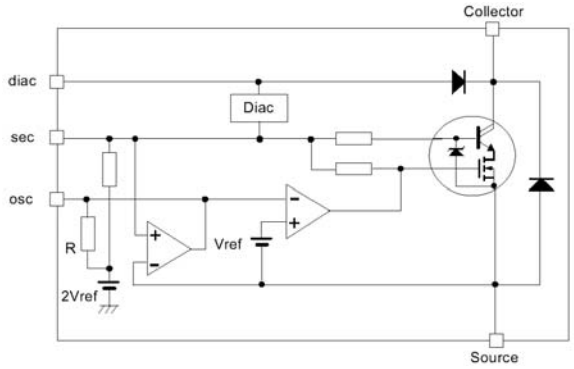

Fig. 1 – VK05 internal structure.

The application description and design rules are given in Section 2 and 3 respectively. Finally in Section 4 extensive simulation and experimental results are presented.

2. Application description

Typical electronic lamp ballast is shown in Fig. 2. The half bridge is connected to the main through a bridge rectifier and a capacitive filter. The current drawn from the mains features a distorted

waveform since it flows only when the rectified voltage is higher than the DC bus voltage across the capacitor.
The current waveform can be shaped using an input passive filter but it would result bulky since it has to filter low frequency components (50-60Hz) with PF close to unity. Although the fully active solution performs better it would require complex control logic and feedback. Intermediate solutions are able to give compliant behavior keeping low the cost of the power factor corrector circuit.
VKXX family by STMicroelectronics represents a viable solution for PFCs in lighting applications, due to the peculiar features of such an application field, i.e. constant output power and switching frequency. The PFC circuit is based on Boost topology, as shown in Fig. 3, working in Discontinuous Conduction Mode (DCM). The half bridge circuit that drives the electronic lamp sets the switching frequency by means of a synchronizing signal to "Sec" pin. The duty cycle, D, is set by a capacitor connected to "Osc" pin, with a 50% maximum value.
The harmonic performance of the circuit can be improved adding a feed-forward term of the input voltage by means of a resistor, R_D. Doing so, the duty cycle D is reduced as the input AC voltage increases.

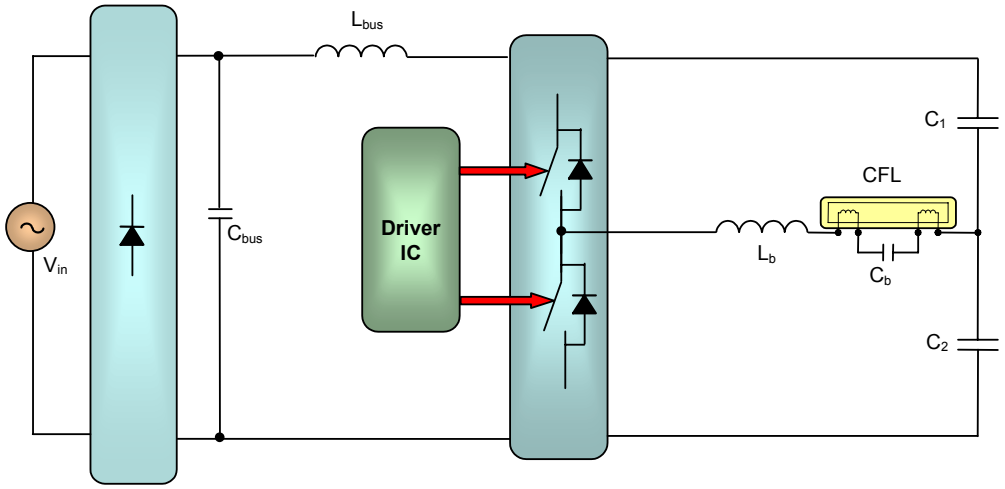

Fig. 2 – Typical electronic ballast circuit for CFL.

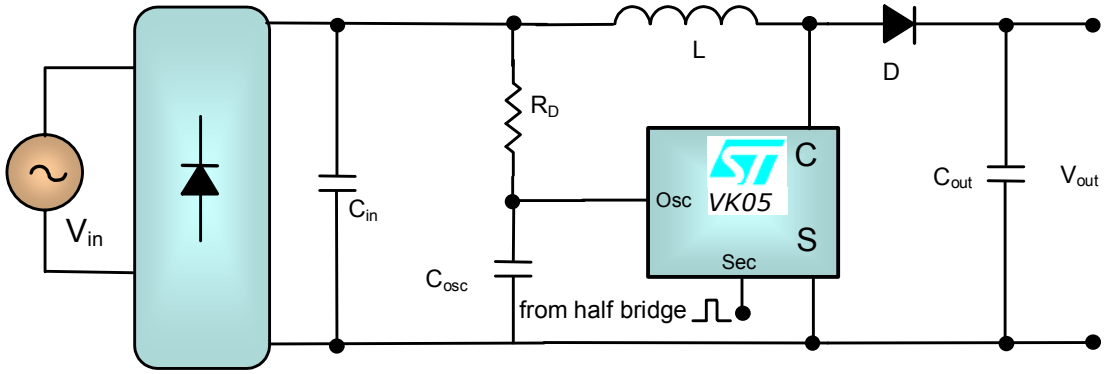

Fig. 3 – PFC circuit using STMicroelectronics VK05.

Although some draw-backs can be listed such as the voltage follower configuration, that could be a critical factor in wide range applications, and the high stress of the power device inherent of DCM topology, the proposed circuit shows high performance in terms of PF since it

boost it from 0.7 to 0.97 with THD lower than 20%.

Differently from the CCM operation, where the boost converter can be controlled in order to achieve an almost sinusoidal current absorption, when the converter operates in DCM, the input average current is not proportional to the input voltage, so that the power factor results lower than unity [3]. However, it is still possible to meet low frequency harmonic standard like EN61000-3-2 Class C. Basic converter analysis shows that the normalized input average current is given by (1).

$$\bar{i}_{LN} = D^2 \frac{V_{inN}}{1 - V_{inN}} \tag{1}$$

where the normalization factors are defined as $V_N = V_{out}$, $R_N = 2Lf_S$, $I_N = \frac{V_N}{R_N}$ and V_{in} is the input voltage. Relation (1) holds as long as the converter operates in DCM, which imposes the following constraint:

$$V_{inN} < 1 - D \tag{2}$$

According to (1), at constant duty-cycle, the average input current is not proportional to the input voltage because of the term $1\text{-}V_{inN}$ at the denominator of (1). By reducing the duty-cycle at increasing instantaneous input voltage values, a lower input current distortion can be achieved. This is the effect of the feed-forward action implemented by resistor R_D in Fig. 3. The duration of the switch on interval can be determined observing that the emitter switching device begins to turn off when the C_{osc} capacitor voltage becomes equal to the internal reference voltage V_{REF}. The duration of the C_{osc} capacitor charging phase is given by:

$$t_{on1} = \tau \, ln\left(\frac{1}{1 - \frac{V_{REF}}{V_{eq}}}\right) \tag{3}$$

where $V_{eq} = 2V_{REF}\frac{R_D}{R + R_D} + V_{in}\frac{R}{R + R_D}$,

$\tau = RC_{osc}$, and R is the internal charge resistor. The actual duration of the switch on-time is given by the sum of the capacitor charging phase t_{on1} and the switch storage time t_{STO} as in (4).

$$t_{on} = t_{on1} + t_{STO} \tag{4}$$

Accordingly, the average input current can be determined by substituting (4) into (1) which gives:

$$\bar{i}_{LN} = \frac{V_{inN}}{1 - V_{inN}}\left(\frac{t_{STO}}{T_S} - \frac{\tau}{T_S} ln\left(1 - \frac{1}{2\alpha + \frac{V_{inN}}{V_{REFN}}(1 - \alpha)}\right)\right)^2 \tag{5}$$

where $\alpha = \frac{R_D}{R + R_D}$ and T_s is the switching period. Based on (3) and (4), capacitor C_{osc} can be suitably selected, by imposing the maximum duty-cycle D_{max} (0.5) when the input voltage is zero. This gives the relation (6).

$$\tau = \frac{D_{max} - \frac{t_{STO}}{T_S}}{f_S \, ln\left(\frac{2\alpha}{2\alpha - 1}\right)} \tag{6}$$

where f_s is the switching frequency. Once capacitor C_{osc} has been selected resistor R_D must be chosen imposing the DCM condition (2) all along the line half period. Since the t_{on} time depends on the input voltage V_{in}, the verification of condition (2) must be done numerically.

As an example, a typical input average current is shown in Fig. 3, and its spectrum compared with EN61000-3-2 Class C limits in Fig. 4 (note that the fundamental component is out of scale). The current was calculated according to (1) using the following parameters: V_{in}=230V_{RMS}, V_{out}=400V, L=1mH, f_S=50kHz, P_{in}=27W, D_{max}=0.35. As shown it complies with the standard featuring THD = 15.3% and PF= 0.988.

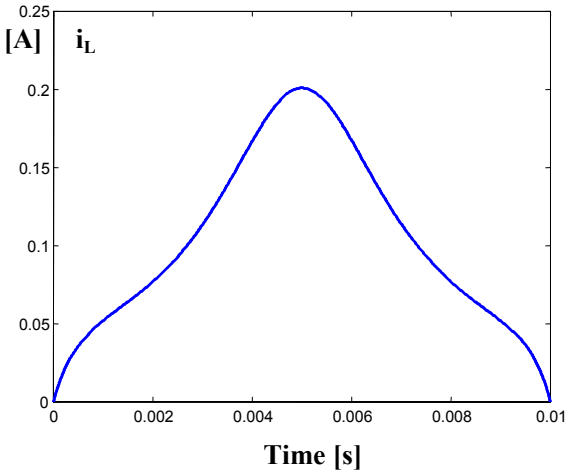

Fig. 4 – Simulated input average current.

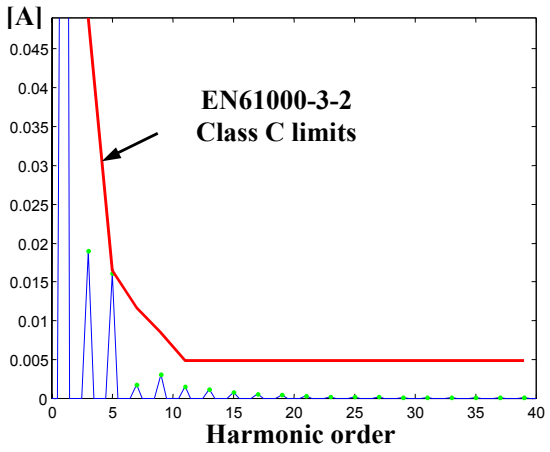

Fig. 5 – Input average current spectrum compared with EN61000-3-2 Class C limits.

In Fig. 6 and Fig. 7 the peak current I_{cmax} and the average current in the switch are shown respectively.

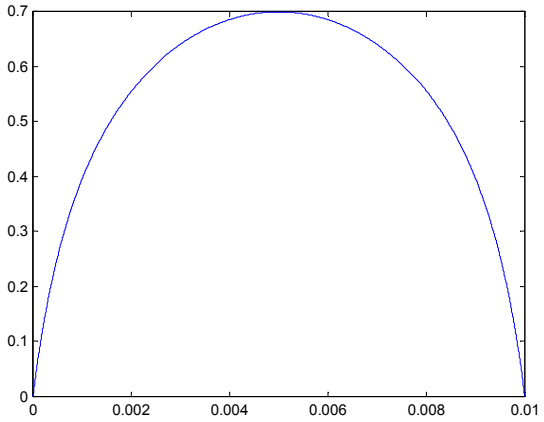

Fig. 6 – Peak switch current I_{Cmax} in a half period (y: [A], x: [s]).

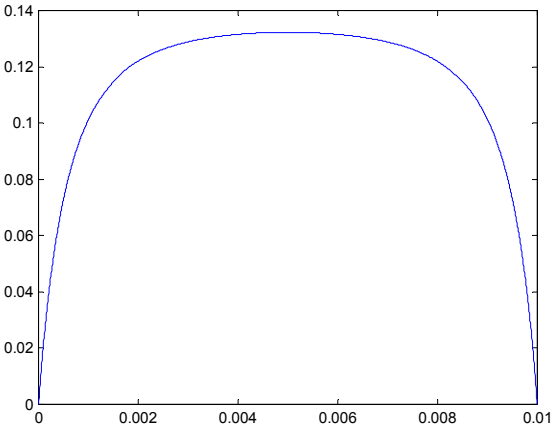

Fig. 7 – RMS switch current I_{Crms} in a half period (y: [A], x: [s])

3. Experimental results

Taking into account the aforementioned performance a prototype has been built to experimentally verify the key features of the circuit, such as the cost and the complexity.

In Fig. 8 input voltage and current of a standard bridge rectifier with capacitive filter are shown, while in Fig. 9 the same waveforms are shown in the modified circuit using VK05 device, confirming the suitability of the smart device for such an application. Only a negligible current distortion is shown close to zero crossing of the input voltage.

In Fig. 10 and Fig. 11 the collector current I_c is shown as well as the input and output voltages, V_{in} and V_{out}. Such results have been predicted by the simulation results previously shown.

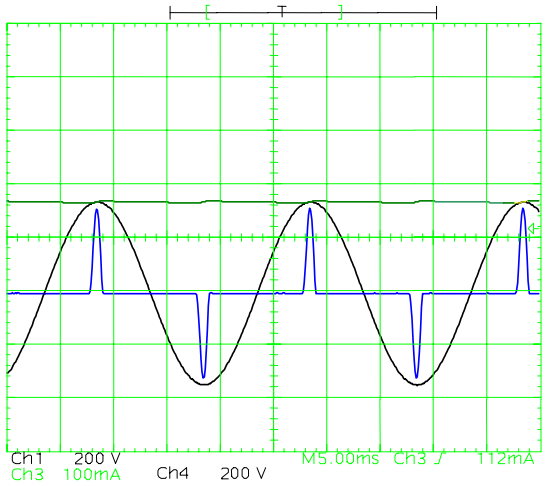

Fig. 8 – Experimental waveforms: input voltage and current, output voltage @ V_{in}=190V_{ac}.

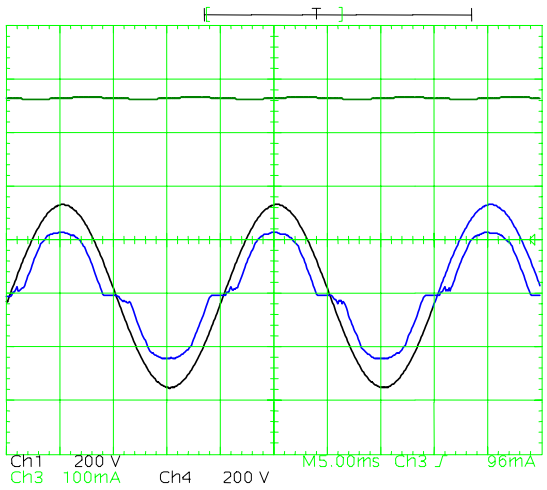

Fig. 9 – Experimental waveforms: input voltage and current, output voltage @ V_{in}=190V_{ac} using the proposed circuit.

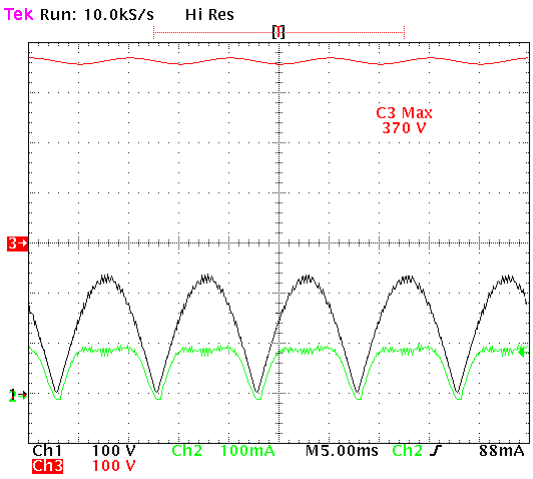

Fig. 10 – Experimental waveforms: input voltage and collector current I_C, and output voltage @ V_{in}=190V_{ac} using the proposed circuit.

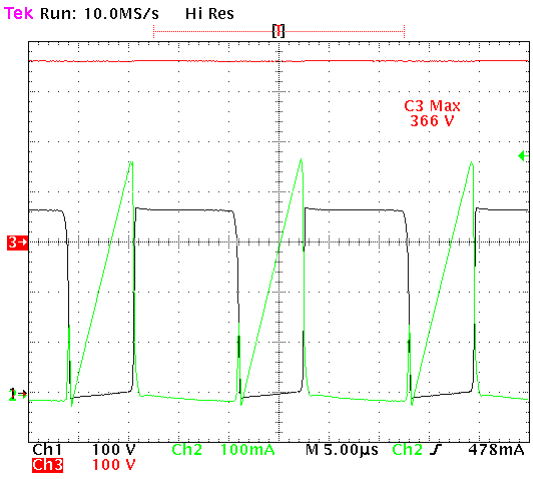

Fig. 11 – Experimental waveforms: collector current I_C, output voltage @ V_{in}=190V_{ac} using the proposed circuit.

3. Conclusions

STMicroelectronics VKXX smart power IC represents a suitable solution for low cost active PFC in lighting applications. The converter shows low complexity and very low cost thanks to VK05 features, since it requires only an external capacitor and a resistor to make the smart power working in a Boost based power factor corrector circuit.

References

[1] N. Aiello, G. Di Stefano, “A New Self-oscillating Power Converter Topology to Drive Compact Fluorescent Lamp”, PCIM 2001 Nuremberg.

[2] IEC 1000-3-2, First Edition 1995-03, Commission Electrotechnique Internationale, 3, rue de Varembé, Genève, Switzerland.

[3] K. H. Liu, Y. L. Lin, "Current Waveform Distortion in Power Factor Correction Circuits Employing Discontinuous-Mode Boost Converters," IEEE PESC 1989, pp. 825-829.