A New Soft-Switching Forward DC-DC Converter Operating in Discontinuous Conduction Mode

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***Abstract* - The paper presents a simple soft-switching forward DC-DC converter suitable for low power applications. A lossless passive turn-off snubber is employed to provide zero voltage turn off of the switch as well as transformer reset. Moreover, the choice to operate the converter in discontinuous conduction mode (DCM), while providing zero current turn on of the switch, also allows to simplify the topology by eliminating the inductive output filter.**

A detailed converter analysis, aimed to highlight advantages and drawbacks of the presented topology, is reported, together with a suitable design procedure. Experimental results are also included to verify the theoretical expectations.

I. Introduction

To be competitive, isolated DC-DC converters for low power applications must have reduced size and cost. The former constrain calls for high switching frequency, in order to reduce the reactive component size, while the latter requires to use the minimum number of active switches and magnetic components. However, the increased switching losses, associated to the high switching frequency, ultimately limit the achievable power density, not mentioning the problem of the high EMI level related to high dv/dt in the circuit. The use of active snubbers [1] can solve these problems at the expense of an extra switch with associated control, as reported in [2-4].

Cheaper solutions, with less degrees of freedom of course, employ lossless passive snubbers [5], which provide zero voltage turn off, as well as controlled dv/dt during the turn off phase. On the other hand, for low power applications, zero current turn on can be easily achieved by discontinuous operation of the converter. In this case, for example, a forward topology can be simplified by removing the inductive output filter, as shown in the proposed converter of Fig. 1: in this case the transformer leakage inductance L_d is exploited as the energy transfer element from input to output and only discontinuous operation (DCM) is allowed (in order to ensure a proper core reset).

The following sections include: description of the converter and its operation, derivation of the voltage conversion ratio, derivation of soft-switching boundaries, proposed design procedure, and experimental prototype measurements.

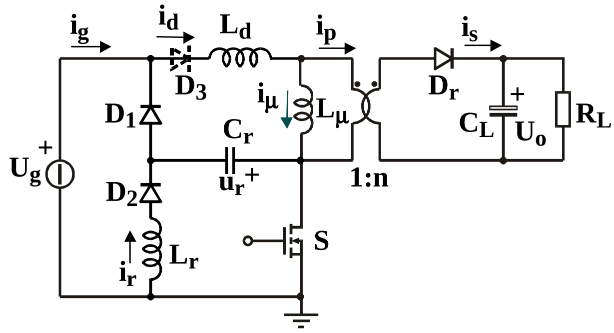

Fig. 1 – Scheme of the proposed soft-switched forward DC-DC converter. (Note that diode D_3 can be removed)

II. Converter Description

The proposed soft-switching forward DC-DC converter operating in DCM shown in Fig. 1, employs a lossless passive snubber which is made up of snubber capacitor C_r, inductance L_r, and diodes D_1, D_2 and D_3 [5]. In particular, diode D_3 is initially considered to simplify the converter analysis. However, as it will be explained in the following, it can be removed with a proper snubber design, improving the converter efficiency. According to step-down operation, the output voltage U_{op} reflected to the transformer primary side must be lower than the input voltage U_g. The lossless passive snubber provides both zero voltage switch turn off, with a controlled dv/dt, and transformer reset, while the DCM operation implies zero current switch turn on as well as soft rectifier diode turn off. The converter main waveforms in a switching period are shown in Fig. 2. As we can see, each switching period can be subdivided into five intervals described in the following. In order to simplify the notation, the time origin was implicitly selected at the beginning of each sub-interval.

Interval $T_{01} = T_1 - T_0$ [see Fig. 3a]. At instant T_0 the switch is turned on under zero current condition causing the turn on of rectifier diode D_r, if the following condition is satisfied:

$$U_g \frac{L_\mu}{L_d + L_\mu} > \frac{U_o}{n} = U_{op} \tag{1}$$

where $n = N_2/N_1$ is the transformer turns ratio

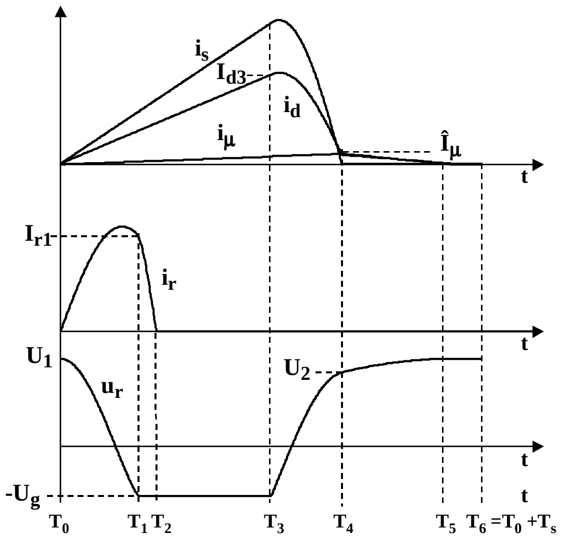

Fig. 2 - Converter main waveforms in a switching period

Both input current i_d and magnetizing current i_μ start to increase linearly, as described by the following relations:

$$i_d(t)=\frac{U_g-U_{op}}{L_d}t \tag{2}$$

$$i_\mu(t)=\frac{U_{op}}{L_\mu}t \tag{3}$$

At the same time, the snubber capacitor C_r resonates with inductor L_r through the loop formed by diode D_2 and switch S. Calling U_1 the initial capacitor voltage, voltage u_r and current i_r waveforms are given by:

$$u_r(t)=U_1\cos(\omega_r t) \tag{4}$$

$$i_r(t)=\frac{U_1}{Z_r}\sin(\omega_r t) \tag{5}$$

where $\omega_r=\frac{1}{\sqrt{L_rC_r}}$ and $Z_r=\sqrt{\frac{L_r}{C_r}}$ are the resonance angular frequency and characteristic impedance, respectively. If U_1 is higher than the input voltage U_g, capacitor voltage u_r reverses becoming equal to $-U_g$ at instant T_1. This causes the turn on of diode D_1 ending this phase, whose duration is:

$$T_{01}=\frac{1}{\omega_r}a\cos\left(-\frac{U_g}{U_1}\right) \tag{6}$$

The value of current i_r at the end of this interval is:

$$I_{r1}=i_r(T_{01})=\frac{U_1}{Z_r}\sin(\omega_r T_{01})=\frac{U_1}{Z_r}\sqrt{1-\left(\frac{U_g}{U_1}\right)^2} \tag{7}$$

Interval $T_{12}=T_2-T_1$ [see Fig. 3b]. When D_1 turns on, the capacitor voltage u_r remains clamped to $-U_g$ while current i_r decreases linearly to zero at instant T_2, thus turning off diodes D_1 and D_2 with a controlled di/dt. Current i_r behavior is described by:

$$i_r(t)=I_{r1}-\frac{U_g}{L_r}t \tag{8}$$

while the interval duration is:

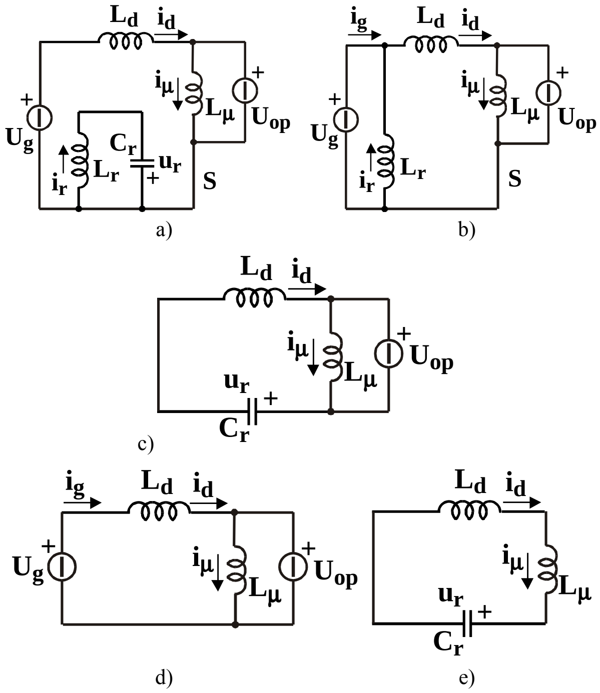

Fig. 3 - Subcircuits corresponding to different intervals during a switching period. a) interval T_{01}; b) interval T_{12}; c) interval T_{23}; d) interval T_{34}; e) interval T_{45}

$$T_{12}=\frac{L_rI_{r1}}{U_g} \tag{9}$$

Interval $T_{23}=T_3-T_2$ [see Fig. 3c]. This interval ends the switch on time while the snubber remains deactivated. During this phase as well as the previous one, the input inductor and magnetizing currents continue to increase linearly, following (2) and (3).

$$T_{23}=T_{ON}-T_{01}-T_{12} \tag{10}$$

Interval $T_{34}=T_4-T_3$ [see Fig. 3d]. The switch turns off at instant T_4 under zero voltage condition and its voltage rises following the same behavior of snubber capacitor voltage u_r, which resonates with the leakage inductance L_d. Their voltage and current waveforms are given by:

Initial conditions:

$$\begin{cases} u_r(0)=-U_g \\ i_d(0)=I_{d3}=i_d(T_{03})=\dfrac{U_g-U_{op}}{L_d}T_{ON} \end{cases} \tag{11}$$

$$u_r(t)=-U_{op}-(U_g-U_{op})\cos(\omega_1 t)+Z_1I_{d3}\sin(\omega_1 t) \tag{12.a}$$

$$i_d(t)=I_{d3}\cos(\omega_1 t)+\left(\frac{U_g-U_{op}}{Z_1}\right)\sin(\omega_1 t) \tag{12.b}$$

where $\omega_1=\frac{1}{\sqrt{L_dC_r}}$ and $Z_1=\sqrt{\frac{L_d}{C_r}}$ are the resonance angular frequency and characteristic impedance, respectively. During this phase, the rectifier diode D_r remains on, continuing the energy transfer from the source to the load. At the same time, the magnetizing current continues to increase under the action of the output voltage reflected to the primary side. This interval lasts until the transformer secondary current $i_s = (i_d - i_\mu)/n$ zeroes, causing the turn off of diode D_r, again with a controlled di/dt. Its duration can be calculated from the following equation:

$$i_d(T_{34}) = I_{d3}\cos(\omega_1 T_{34}) + \left(\frac{U_g - U_{op}}{Z_1}\right)\sin(\omega_1 T_{34}) = i_\mu(T_{ON} + T_{34}) = \hat{I}_\mu \tag{13}$$

The exact value for T_{34} can be computed only numerically. However, an approximated expression can be derived neglecting the magnetizing current in (13). The result is as follows:

$$T_{34} \approx \frac{1}{\omega_1}\left[\pi - a\tan\left(-\frac{Z_1 I_{d3}}{U_g - U_{op}}\right)\right] = \frac{1}{\omega_1}\left[\pi - a\tan(\omega_1 T_{ON})\right] \tag{14}$$

where the definition of I_{d3} from (11) was used to derive the last expression. Note that $\frac{\pi}{2} < \omega_1 T_{34} < \pi$.

The voltage U_2 across the resonant capacitor at instant T_4 is calculated from (12.a) and is given by:

$$\begin{aligned} U_2 &= u_r(T_{34}) \\ &= -U_{op} - (U_g - U_{op})\cos(\omega_1 T_{34}) + Z_1 I_{d3}\sin(\omega_1 T_{34}) \end{aligned} \tag{15}$$

Interval $T_{45} = T_5$-T_4 [see Fig. 3e]. During this interval the snubber capacitor resonates with the whole transformer inductance L_d+L_μ bringing the magnetizing current to zero, thus resetting the transformer core. The initial conditions to be used are:

$$\begin{cases} u_r(0) = U_2 \\ i_d(0) = i_\mu(0) = \dfrac{U_{op}}{L_\mu}(T_{ON} + T_{34}) = \hat{I}_\mu \end{cases} \tag{16}$$

while voltage and current are given by:

$$u_r(t) = U_2\cos(\omega_2 t) + Z_2 \hat{I}_\mu \sin(\omega_2 t) \tag{17.a}$$

$$i_d(t) = i_\mu(t) = \hat{I}_\mu\cos(\omega_2 t) - \frac{U_2}{Z_2}\sin(\omega_2 t) \tag{17.b}$$

where $\omega_2 = \frac{1}{\sqrt{(L_d + L_\mu)C_r}} = \omega_1\sqrt{\frac{\alpha}{1+\alpha}}$ and $Z_2 = \sqrt{\frac{L_d + L_\mu}{C_r}} = Z_1\sqrt{\frac{1+\alpha}{\alpha}}$ are the resonance angular frequency and characteristic impedance, respectively and $\alpha = \frac{L_d}{L_\mu}$. Interval T_{45} can be computed by letting $i_d(T_{34}) = 0$.

$$T_{45} = \frac{1}{\omega_2} a\tan\left(\frac{Z_2 \hat{I}_\mu}{U_2}\right) \tag{18}$$

The voltage across C_r at the end of this phase is equal to the initial voltage U_1 considered at the beginning of the switching period, i.e.:

$$u_r(T_{45}) = U_2\cos(\omega_2 T_{45}) + Z_2\hat{I}_\mu\sin(\omega_2 T_{45}) = U_1 \tag{19}$$

Interval $T_{56} = T_6$-T_5. This phase, in which the load is fed only by the output capacitor, completes the switching period.

$$T_{56} = T_S - T_{ON} - T_{34} - T_{45} \tag{20}$$

III. VOLTAGE CONVERSION RATIO

The approximated voltage conversion ratio M can be derived from the equations describing the converter behavior and corresponding to the waveforms of Fig. 2. In particular, the average (in a switching period) secondary current $\bar{i}_s = \frac{\bar{i}_d - \bar{i}_\mu}{n}$ is calculated and equated to the load current. In order to derive a closed form for M, the approximated formula (14) for T_{34} was used under the assumption of a negligible magnetizing current as compared to the input inductor current i_d. The result is the following relation:

$$M = \frac{U_{op}}{U_g} \approx \frac{1}{1 + \dfrac{2 + R_{LpN}\ \alpha\ \omega_1 \beta^2}{R_{LpN}\left(2 + \theta_{on}^2 + 2\sqrt{1+\theta_{on}^2}\right)}} \tag{21}$$

where $\theta_{on} = \omega_1 d T_s$, $\beta = \theta_{on} + \pi - a\tan(\theta_{on})$, and $R_{LpN} = \frac{R_{Lp}C_r}{T_s} = \frac{R_L C_r}{n^2 T_s}$ is the normalized load resistance reflected to the primary side. An example of control characteristics, i.e the voltage conversion ratio as a function of the duty-cycle for different values of normalized load resistance R_{LpN}, is shown in Fig. 4 for the set of converter parameters listed in Table I: as we can see, just like any forward converter, there is a limited maximum duty-cycle due to the need of resetting the transformer (interval T_{45} in Fig. 2), together with a limited minimum duty-cycle in order to ensure a proper operation of the snubber circuit (interval T_{01} in Fig. 2). Last, but not least, the zero voltage condition poses further limitations on the converter operating point. All these aspects are covered in the following section.

Table I - Converter parameters used in Fig. 4

$L_d = 8\mu H$	$L_r = 6.5\mu H$		
$L_\mu = 300\mu H$	$C_r = 3 \times 4.7 nF$	$n = 0.5$	$T_S = 5\mu s$

IV. ZERO VOLTAGE CONDITION

In this converter, the zero voltage turn off condition requires voltage U_1 to be higher than the input voltage U_g. This condition depends mainly on the inductive energy stored in input inductor L_d at the end of the switch on time: as a consequence, the ZVS condition is lost at light load. Moreover, a minimum switch on time equal to interval T_{01} is required to reverse the voltage u_r up to $-U_g$. In order to derive this lower boundary, the same approximation used in deriving the voltage conversion ratio, i.e. utilization of (14), is used. First, let's express voltage U_1 as a function of M and

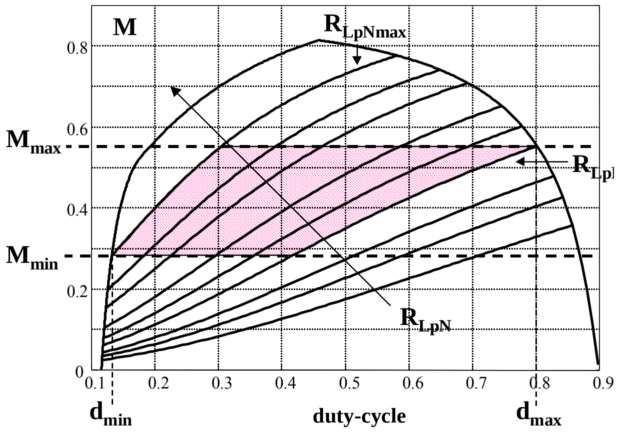

Fig. 4 - Voltage conversion ratio M as a function of duty-cycle for different values of normalized load resistance R_{LpN}

other converter parameters. Substituting (11) into (15) allows to derive U_2 as follows:

$$U_2 = U_g\left(-M + (1-M)\sqrt{1+\theta_{on}^2}\right) \qquad (22)$$

Then, using (14), (16), (18) and (22) into (19) we find:

$$U_1 = -\frac{U_g}{k} \qquad (23)$$

where

$$k = -\frac{1}{\sqrt{\left(-M + (1-M)\sqrt{1+\theta_{on}^2}\right)^2 + \alpha(1+\alpha)(M\beta)^2}} \qquad (24)$$

If $k > -1$ then $U_1 > U_g$ the soft switching condition can be satisfied, and the minimum switch on time can be derived from (6) as:

$$T_{ONmin} = \frac{1}{\omega_r}\cos^{-1}k \qquad (25)$$

The latter can be solved in numerical form for different values of the normalized load resistance R_{LpN}.

The limitation on the maximum switch on time, necessary to ensure DCM operation as well as proper transformer reset, can be found by letting interval $T_{56} = 0$ into (20). Then, we have:

$$T_{ON\,max} = T_S - T_{34} - T_{45} \qquad (26)$$

Using (16), (18) and (22) into (26) we obtain:

$$\theta_{ONmax} = \omega_1 T_S - [\pi - \operatorname{atan}(\theta_{ONmax})] + \\ -\sqrt{\frac{1+\alpha}{\alpha}}\operatorname{atan}\left[\frac{\beta\sqrt{\alpha(1+\alpha)}}{-1+\left(\frac{1}{M}-1\right)\sqrt{1+\theta_{ONmax}^2}}\right] \qquad (27)$$

An example of duty-cycle limitation given by (25) and (27) is shown in Fig. 5 in terms of boundary curves for the control characteristics. The same figure, knowing the minimum and maximum voltage conversion ratio, allows to identify the minimum and maximum normalized load resistances which still guarantee a soft commutation.

If diode D_3 is removed to avoid its conduction losses, the converter behavior changes because now, during interval T_{56}, the capacitor C_r starts to discharge to the input in the resonant manner through L_μ, L_d, L_r and D_2. This reduces voltage U_1 and adversely affects the soft switching condition, especially at high input voltage when the duty-cycle is minimum.

V. Component Stresses

In order to outline a reasonable design procedure, it is important to analyze the main component current and voltage stresses, highlighting their dependence on the different converter parameters.

Switch voltage stress. The maximum voltage across the switch occurs at the end of interval T_{45} when the voltage across the resonant capacitor reaches its maximum value, i.e.:

$$\hat{U}_{SW} = \hat{U}_g + \hat{U}_1 = \hat{U}_g\left(1 - \frac{1}{k}\right) \qquad (28)$$

where (23) was used to derive the last term. The maximum occurs at maximum input voltage and load current.

Switch current stress. During T_{ON} interval, the switch carries the sum of the input current i_d and the resonant current i_r, i.e. from (2) and (5):

$$i_{SW}(t) = \frac{U_g - U_{op}}{L_d}t + \frac{U_1}{Z_r}\sin(\omega_r t) \qquad (29)$$

Its maximum can occur both during interval T_{01} or at the end of interval T_{ON}. In the first case the peak occurs approximately at the peak of the resonant current, i.e.:

$$\hat{I}_{SW1} \approx \frac{U_1}{Z_r} + \frac{U_g - U_{op}}{L_d}\frac{\pi}{2\omega_r} \qquad (30)$$

so that the switch current stress can be expressed as:

$$\hat{I}_{SW} = \max\left\{\hat{I}_{SW1}, \frac{\hat{U}_g - U_{op}}{L_d}T_{ON}\right\} \qquad (31)$$

Diode D_1 voltage and current stresses. The maximum voltage across D_1 occurs at the switch turn on and coincides with the switch voltage stress (28). Its maximum current can occur either at T_1, when it starts carrying the resonant current i_r, or during interval T_{34}, when the input inductor current i_d is flowing through it. From (7), and (12b) we can write:

$$\hat{I}_{D1} = \max\left\{\hat{I}_{r1}, \hat{I}_d\right\} \qquad (32a)$$

where

$$\hat{I}_d = \sqrt{\hat{I}_{d3}^2 + \left(\frac{\hat{U}_g - U_{op}}{Z_1}\right)^2} \qquad (32b)$$

Diode D_2 voltage and current stresses. The maximum voltage across D_2 occurs when D_1 is on, and is equal to the maximum input voltage, while its maximum current coincides with the peak of the resonant current i_r.

Diode D_3 voltage and current stresses. The maximum voltage across D_3 occurs at the end of interval T_{45} when the input inductor current zeroes, and is equal to the maximum voltage $\hat{U}_1$ across the resonant capacitor C_r, while its maximum current coincides with the peak of the input inductor current $\hat{I}_d$.

Diode D_r voltage and current stresses. The maximum voltage across D_r occurs at the end of interval T_{45} and is given by:

$$\hat{U}_{Dr} = n\hat{U}_1\left(\frac{L_\mu}{L_d + L_\mu}\right) + U_o$$

The D_r current stress is given by the difference between the input inductor current i_d and the magnetizing current. Neglecting the latter, the maximum current equals $\hat{I}_d$ (see (32b)).

VI. Design Considerations

From the analysis carried out in the previous sections, we have seen that the converter parameters must be chosen in order to ensure soft-switching as well as a proper transformer core reset in all the operating points of interest, i.e. in the desired input voltage and output current ranges. This has to be done taking into account also voltage and current stresses in the main devices. The curves reported in Fig. 5, showing the effect of different parameters on the soft-switching area in the control characteristics, help to made a first choice. From these curves we can made the following considerations:

- the magnetizing inductance can be chosen so as to meet the core needs without affecting too much the soft switching behavior;
- the input inductor L_d strongly influences both minimum and maximum power achievable under soft commutations, and, consequently, it affects all the device current stresses;
- the resonant inductor L_r value poses a limitation only on the minimum duty-cycle (i.e. minimum power at maximum input voltage) and has effect on switch and diodes D_1 and D_2 current stresses;
- the resonant capacitor C_r is another key parameter strongly affecting the soft switching area and voltage U_1 value, which determines the voltage stress of many devices.

If the transformer parameters are known (magnetizing inductance L_μ and leakage inductance L_d), then a possibile design procedure could be to select a C_r value based on the maximum output power constraint, and the L_r value to maintain the soft switching condition up to the desired minimum power.

VII. Experimental Results

A converter prototype, rated at $U_g = 36 \div 48$V, $U_o = 12$V and $P_{oN} = 50$W with the basic component values given by Table I, was developed. The transformer, built on a ETD34 core size, had a gap on one lateral leg plus few turns in series with the primary winding (located, with the secondary

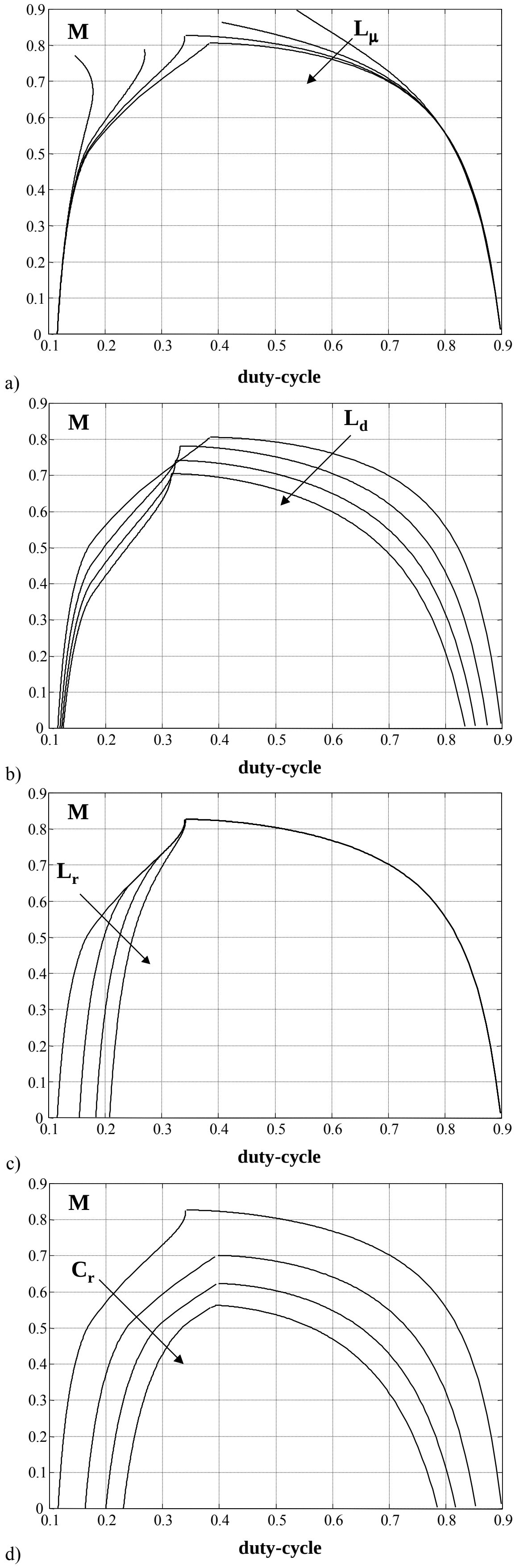

Fig. 5 – Boundary curves at different converter parameter values; a) $L_\mu = 100 \div 400\mu$H; b) $L_d = 8 \div 20\mu$H; c) $L_3 = 6.5 \div 24\mu$H; d) $C_r = 12 \div 48$nF;

winding, on the ungapped central leg) in order to produce the desired input inductance L_d. Unfortunately, at the time of writing, the transformer was not optimized, giving rise to excessive power loss. The prototype was used to verify several theoretical results. Fig. 6 shows the main converter waveforms, which closely resemble the ones shown in Fig. 2. Note the step on the u_{DS} waveform during the switch off time, revealing the end of interval T_{45}. The voltage conversion ratio was then measured, giving the results shown in Fig. 7. As can be seen, the experimental data closely match the theoretical curves, especially at reduced output power, where the unity efficiency assumption is better verified.

VIII. Topology Modification and Future Work

The elimination of diode D_3 from the converter topology greatly improves the overall efficiency, but also significantly modifies the converter's behavior. Therefore, the analysis outlined in Section II and III, is no longer valid. Nevertheless, the basic good properties of the converter are maintained. In particular, Fig. 8 shows how the converter waveforms modify after diode D_3 is removed. It is possible to see the discharge of the resonant capacitor during the switch off interval. Anyway, at nominal output power, soft switching is maintained. In these conditions, the measured efficiency grows from 0.75 to 0.815. A significant improvement can be achieved by optimizing the magnetic part of the converter, which is currently dissipating a significant amount of power. Just using an external pot core to build L_d and removing the auxiliary winding on the transformer lateral leg improved the efficiency up to 85%. This will be the object of future research activity.

IX. Conclusions

A simple soft-switching forward DC-DC converter suitable for low power applications is presented. The converter uses a lossless passive turn-off snubber to provide zero voltage turn-off of the switch as well as transformer reset. Moreover, the converter operates in discontinuous conduction mode (DCM), which guarantees zero current turn on of the switch and allows to eliminate the inductive output filter. A detailed converter analysis supported by the main simulated waveforms is given, which highlights advantages and drawbacks of the topology. Experimental results verify and validate the theoretical analysis.

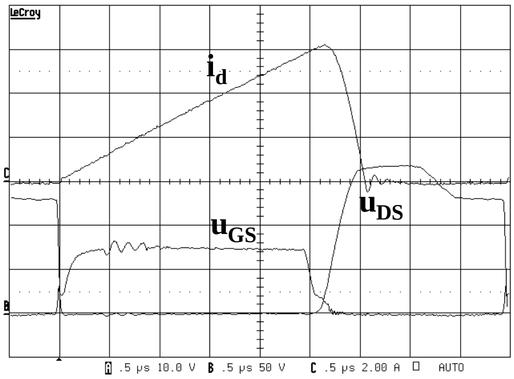

Fig. 6 - Measured main converter waveforms @U_g = 42V, U_o = 12V, P_o = 50W, with diode D_3
i_d: 2A/div, u_{DS}: 50V/div, u_{GS}: 10V/div

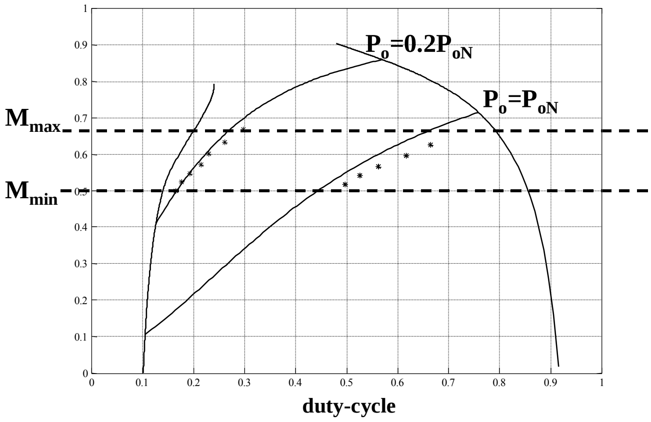

Fig. 7 - Comparison between calculated and measured voltage conversion ratio as a function of duyu-cycle for two different power levels

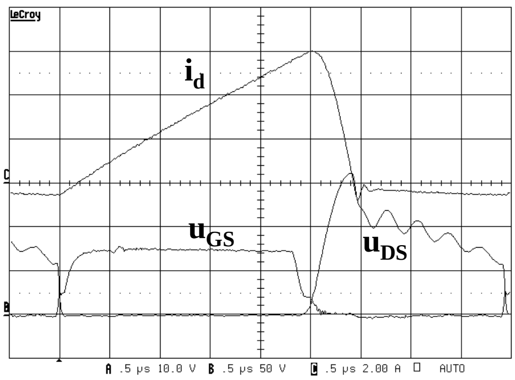

Fig. 8 - Measured main converter waveforms @U_g = 42V, U_o = 12V, P_o = 50W, without diode D_3
i_d: 2A/div, u_{DS}: 50V/div, u_{GS}: 10V/div

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