

GaN HEMT reliability research – a white paper –

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GaN reliability – a white paper concisely developing concepts required for GaN HEMT and vertical devices reliability study

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SUMMARY

This white paper provides an overview of the physical failure mechanisms and failure modes of GaN rf HEMTs, and of the related methodology for reliability study. The paper concisely describes main GaN degradation mechanisms, electrical characterization methods, deep levels analysis, device thermal characterization tools, failure analysis procedures. Comments on the role of device modeling and simulation are provided. Steps necessary for developing a research program in GaN semiconductor reliability are proposed. A preliminary analysis of the reliability of vertical devices is also reported.

1. INTRODUCTION

Reliability is a key issue for power GaN HEMT applications, from wireless and telecommunication systems, to radar, to high-efficiency energy conversion and management system. The topic of GaN HEMT reliability is receiving increasing attention from research laboratories worldwide, as testified by the number of papers published each year on this subject, see Fig. 1 and 2.

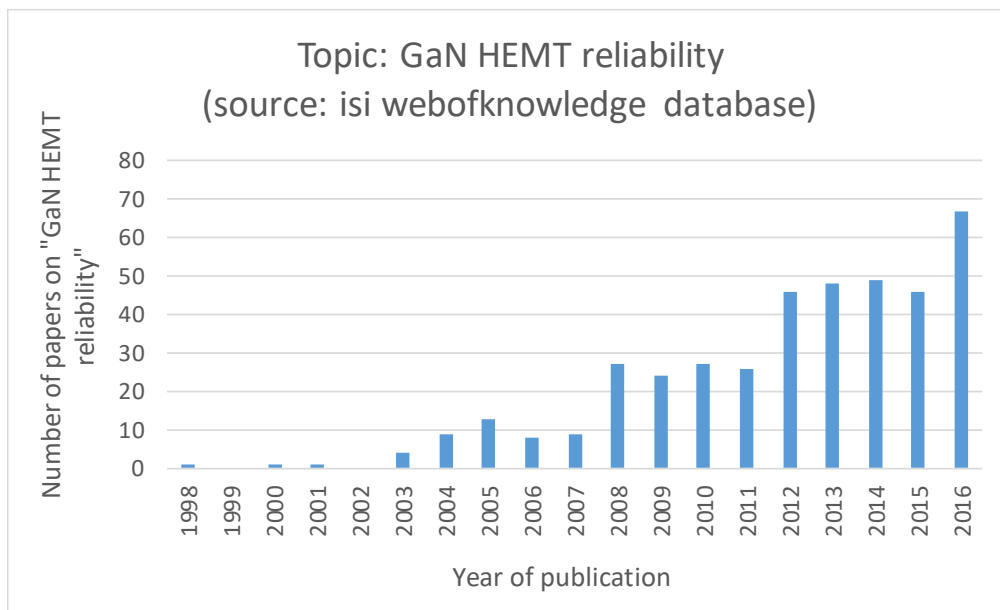


Fig. 1 : Number of papers published each year with topic "GaN HEMT reliability" according to the ISI Web of Science database.

In fact, GaN devices can be affected by failure mechanisms which are not observed in Si or other compound semiconductor devices, due to operating conditions (higher current densities, higher temperatures, higher electric fields) and to material properties (piezoelectric effects, heteroepitaxy on SiC, Si or sapphire substrates, higher density of defects and deep levels, thermal mismatch and thermal interfaces with substrate and package). This white paper summarizes main failure mechanisms of GaN devices and describes research approaches, methodologies and laboratory practice which can be adopted for the study and improvement of GaN HEMT and vertical GaN reliability.

This white paper is organized as follows:

Section 2 describes main failure mechanisms of GaN HEMTs and related characterization and testing methods.

Sub-section 2.1 describes "electrical signature" of the various failure mechanisms and their effects on device reliability

Sub-section 2.2 describes device electrical characterization procedures required for GaN HEMT reliability analysis

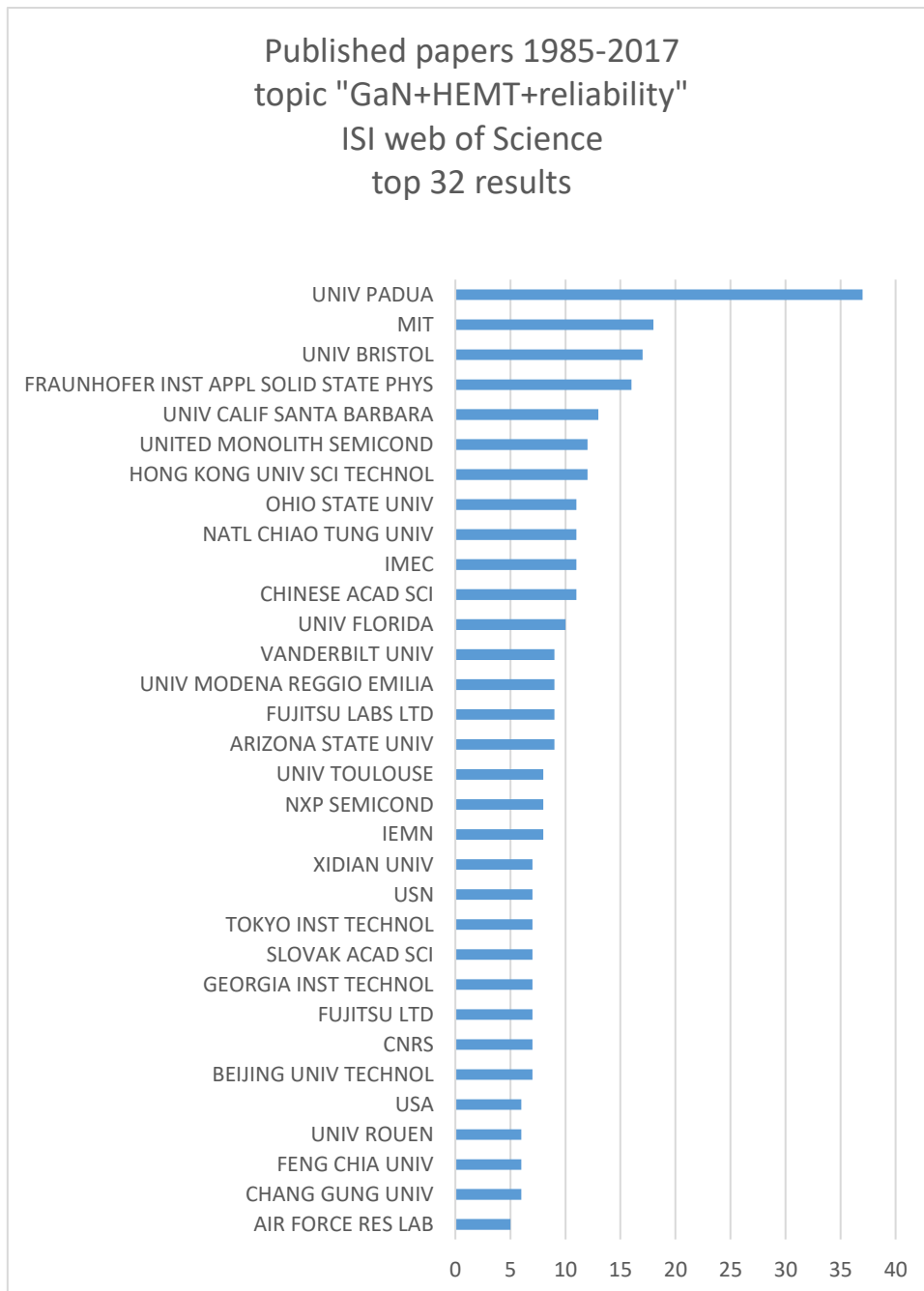


Fig. 2 : Distribution of 1999-2017 published papers with topic "GaN HEMT reliability" according to organization, source : ISI Web of Science

Sub-section 2.3 describes thermal characterization methods adopted for the evaluation of device junction temperature during accelerated tests

Sub-section 2.4 describes typical on-wafer, short-term (<100 h) tests adopted during process development to quickly select process options, or, on devices having a stabilized technology, for identifying absolute maximum ratings and electrical/environmental conditions for long-term tests

Sub-section 2.5 describes the set of long-term (>1000 h) accelerated tests generally implemented within a reliability evaluation campaign, and related methodology

Sub-section 2.6 describes failure analysis methodology and techniques, and related material analysis results which can be possibly related to device performance / reliability

Sub-section 2.7 presents some comments related to theoretical modeling and device simulation tools and their use in reliability physics study

Sub-section 2.8 lists relevant papers concerning reliability of GaN HEMT for RF applications and which conferences, tutorial and seminars to attend to upgrade knowledge in the field of reliability

Section 3 provides a discussion of the state-of-the-art development, lists some labs and Universities in USA active in this area and presents a summary of researchers involved in GaN reliability and a list of their publications

Sub-section 3.1 presents some of the labs and Universities in USA

Sub-section 3.2 presents University of Padova research results, facilities, personnel and researchers

Section 4 defines a possible research plan concerning reliability evaluation of GaN HEMT devices for rf applications, based on an incremental approach, starting with essential operation capability, and expanding it to more elaborated techniques and more ambitious objectives as time proceeds, keeping also into account availability of external services

Sub-section 4.1 sketches the research plan and recommended collaborative models between University and the industrial laboratory

Sub-section 4.2 defines skills and resources required, including manpower, computing, lab facilities, number and type of devices needed, and time frame

Section 5 presents preliminary considerations concerning characterization and reliability of GaN vertical devices. Conclusions follow in Section 6.

2. FAILURE MECHANISMS OF GaN HEMT FOR RF APPLICATIONS

Main reliability issues of GaN-based HEMTs can be categorized as follows:

(1) degradation at the gate edge: this failure mode takes place even in the off-state, results in an increase of leakage current, and is accelerated by the electric field. It appears that several physical mechanisms can cause or contribute to induce gate current degradation:

(1.1) converse piezoelectric effect can result from the mechanical stress induced by the high electric field in a piezoelectric material as GaN [1]; converse piezoelectric effect is a consequence of the application of high electric field to piezoelectric GaN: the resulting additional mechanical strain in the semiconductor can lead, in certain bias and temperature conditions, and in the presence of nucleation defects, to lattice damage and further defects formation [2]

(1.2) time dependent degradation can be induced by trap creation and formation of conductive percolative paths between gate and channel; in this case, gate leakage increase has been shown to follow a time dependence similar to MOS dielectric breakdown, with a very weak temperature dependence [3] [4];

(1.3) electrochemical dissolution of GaN can lead to progressive structural damage at the drain edge of the gate, consisting in the formation of pits and grooves, associated with the presence of oxygen or water vapor, leading to the formation of Ga and Al oxide [5]. A relatively complex chain of electrochemical reactions, which requires the presence of holes generated by band-to-band tunneling has been identified as a possible mechanism for GaN surface oxidation. Other authors [6] [7] observed the formation of an interfacial layer under the gate contact, composed by an amorphous layer of aluminum oxide which is formed from the rejection of N and the consumption of Al from an as-formed interfacial layer composed of Al, Ga, O and N.

(1.4) finally, extended erosion and cracks crossing the semiconductor epitaxial layers, as observed using FIB (Focused Ion Beam) cross-sectioning and TEM (Transmission Electron Microscopy) observations, have been found in samples submitted to on-state accelerated testing at high current density and channel temperature. Pits can be easily identified by removing completely passivation and metal layers, and observing the surface by SEM (Scanning Electron Microscopy) or AFM (Atomic Force Microscopy). According to some authors, see for instance [8], this is the true converse piezoelectric effect, which in fact requires a high junction temperature to take place.

While mechanisms (1.1)-(1.3) mostly affect the gate current, with little or no permanent degradation of the drain current, mechanism (1.4) induces a substantial, not recoverable decrease of I_D [8].

(2) permanent and recoverable trapping and detrapping effects may lead to significant device drift, with change in the threshold voltage and transconductance. These may be due to material quality (pre-existing deep levels on the surface and at interfaces, within the GaN buffer, within the semi-insulating substrate), or to process-induced instabilities, especially in connection with compensating species (Fe or C), contaminants like H, F, O, or defects [9];

(3) hot electron effects, with generation of deep levels and trapping of electrons in the dielectrics or/and at surfaces and interfaces under the gate as over the gate-drain access region may occur both during off-state tests or (more frequently) during semi-on and on-state tests [10], [11], [12], [13], [14].

The term "hot electrons" refers to non-equilibrium electrons which acquire kinetic energy values sufficient to overcome potential energy barriers, be injected into buffer, barrier or insulating layers and be trapped there, break atomic bond and create interface states or activate traps, for instance through dehydrogenation [15] [12]. According to the various experimental conditions, material properties and device weaknesses, hot electrons may give rise both to parametric, gradual, permanent or recoverable positive or negative threshold voltage shifts and/or to decrease of transconductance.

(4) Metal-metal and metal-semiconductor interdiffusion

Schottky contacts on GaN and related compounds are generally stable at high temperatures [16]. Both Schottky and ohmic contact can withstand 300°C for extended periods, even if Ni has been reported to form NiO and Ni nitrides starting at annealing temperatures as low as 200°C.

Under severe conditions, used to identify potential failure mechanism in short times, or during process development, or when technology is not yet sufficiently mature and device robustness is still marginal, one can observe the above mentioned degradation mechanisms even during short-term (< 100h) tests. In the following we describe some electrical testing methods which can provide information on the specific features or "signatures" of the various degradation mechanisms.

2.1 “Signatures” of GaN HEMT failure mechanisms

2.1.1 Electric-field induced gate leakage current (converse piezoelectric effect, time dependent gate degradation, electrochemical gate degradation)

The usual way to verify the presence of this failure mechanism is to carry out a step-stress experiment with the device biased in off-state, keeping the gate voltage below the pinch-off voltage value, and increasing the drain voltage in steps of constant duration (5-120 s), Fig. 3.

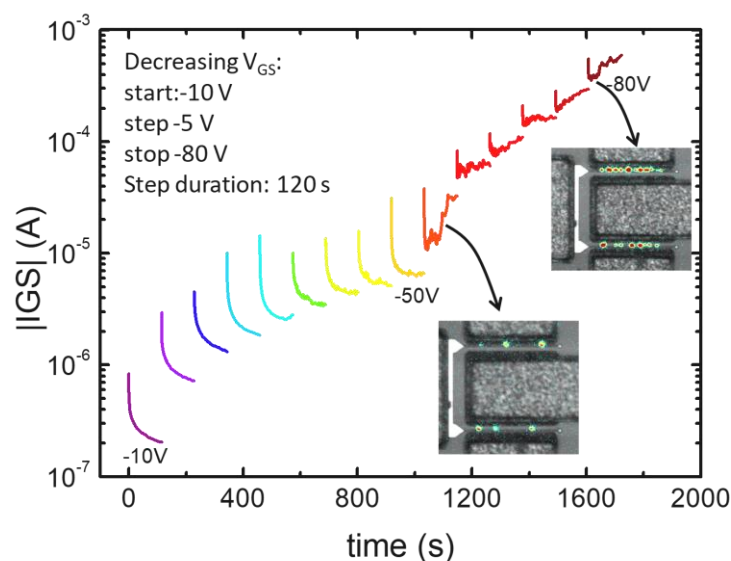


Fig. 3 : Variation of gate current during a step-stress experiment carried out as described in [17]. $V_S = V_D = 0$ V. V_G decreases from -10 to -80 V with -5 V/step, step duration 2 min. The two insets report the false color EL maps measured after two different stages of the stress experiment.

In another widely adopted configuration, source and drain are grounded, and negative bias applied to the gate is increased in absolute value. For microwave devices, where the gate-source distance is usually much shorter than the gate-drain one, testing at $V_{DS} = 0$ V makes the electric field at the source edge higher than that at the drain one, thus submitting the gate-source junction to a higher stress.

Fig. 3 shows the gate current I_G during a step-stress test; at the beginning of each step $|I_G|$ decreases as the negative electron charge trapped under the gate reduces electron injection. When the step at $V_G = -50$ V, ($V_S = V_D = 0$ V) is reached, the gate current becomes noisy and its absolute value starts to increase. During the tests, localized damage points are created, inducing sudden jumps in the leakage current, .

Each jump corresponds to the creation of a new breakdown point which can be identified using electroluminescence (EL) microscopy; see the inset of Fig. 3. The intensity of the EL signal is strongly correlated to an increase of the leakage current, see also Fig. 4. The Figure shows the variation of reverse gate current I_G after each test step on a 0.5- μ m gate Al_xGa_{1-x}N/GaN transistor. When a certain reverse voltage is reached, hereafter identified as critical voltage, the gate leakage current increases substantially, reaching sometimes 10^4 times the initial value. The critical voltage corresponds to $V_G \cong -50$ V for the device under test.

Devices belonging to the same wafer usually show a consistent behavior, with a low dispersion of the "critical voltage" for failure. Electroluminescence microscopy can be adopted as a tool to identify localized reverse current injection points and damaged areas; EL images were taken during the tests and at the end of each step using a cooled charge coupled devices camera, see Fig. 5, which refers to an AlGa_xN/GaN technology having a critical voltage of approximately 30 V.

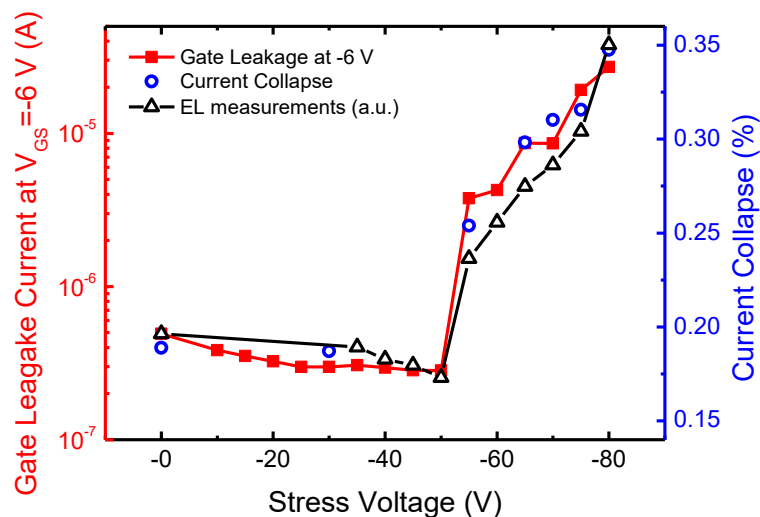


Fig. 4 : Red squares: variation of gate leakage current after each of the stages of a step-stress experiment, carried out with $V_{DS} = 0$ V. Blue circles: variation of the current collapse during the same step-stress experiment. Black triangles: variation of EL signal measured at 10 V after each stage of the step-stress experiment. Step duration 120 s.

Fig. 5 shows the false-colors EL micrographs of an AlGa_xN/GaN HEMT dual-gate test structure, taken at $V_G = -10$ V (with source and drain grounded) after the steps indicated in the figure. Before the steps at the critical voltage $V_G = -50$ V, no EL spot is observed, and $|I_G/W|$ is lower than 0.6 mA/mm. Starting with the step at -60 V, I_G is increased of more than 100x and localized emission spot points in the EL images start being observed. As the test reverse voltage is further increased we observe a higher density of defect points, rather than a widening of the damaged area around each point. Since EL images are taken from the front side of the devices, only the drain and source access regions can be observed, the area under the gate being shadowed by the gate metal. It is possible, however, to use this technique in the backside mode, by detecting the IR and visible EL emitted through the SiC substrate (optically polished and without back metallization).

Not all technologies are affected by this gate degradation mechanism: reverse-bias or off-state step-stress experiments represent an effective way to check whether one particular process is at risk. The critical voltage value, however, does not represent a "safe limit": in fact, as demonstrated by constant voltage stress tests, Fig. 6, the voltage value which induces the gate failure depends on pulse duration or, conversely, the time to breakdown depends on the applied voltage (or the electric field).



Fig. 5: EL microscopy images of a representative HEMT sample. Images were taken at $V_G = 10$ V (with $V_S = V_D = 0$ V) after each step-stress.

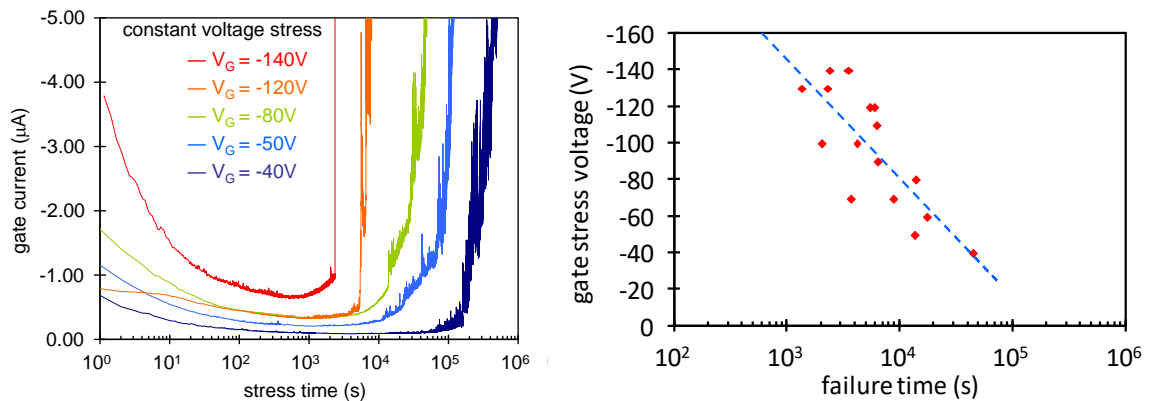


Fig. 6: Top: I_G versus t time to breakdown experiments demonstrating the dependence of the time to gate leakage breakdown on the applied reverse voltage for AlGaIn/GaN HEMTs. Bottom: power-law relating failure time to gate stress voltage.

A model similar to that developed for oxide breakdown in MOS transistors has been developed, involving the formation of defects within the AlGaIn layer and at interfaces. When the concentration of these defects is sufficiently high, conductive percolative paths are formed between gate and 2DEG, leading to an increase in gate leakage current. These paths are dynamically activated and deactivated, thus originating a noisy gate current. The creation of vertical conductive paths between the gate and the 2DEG also have another consequence: recent measurements [4] demonstrate that the increase of current collapse depicted in Fig. 4 is not due to an increase of trap density, but is related to the increased modulation of already existing traps located in the buffer. The increased dispersion indeed takes place only when the gate leakage current increases, Fig. 5, and no new trap is generated, as demonstrated by multiexponential pulsed measurements of drain current

transients, **Fig. 7**, which show that time constants spectra remain basically unchanged after the stress. For a review concerning multiexponential current transient spectroscopy, see [9]. In general, if electrochemical reactions or high temperature is not involved, no extended defect is visible in TEM micrographs of device cross-sections, thus making this mechanism different from converse piezoelectric effect (at RT or high T, identified as mechanisms 1.1 and 1.4 respectively in Section **Errore. L'origine riferimento non è stata trovata.**) or electrochemical induced surface pitting (mechanism 1.3).

In summary, signatures of gate degradation induced by reverse bias consists of: increase of gate current (all mechanisms with the exception of 1.4); random telegraph noise feature in the gate current (1.2); appearance of electroluminescence spots (all mechanisms). Permanent decrease of drain current is observed only for mechanism 1.4, while recoverable I_D degradation can be observed during step-stress test due to trapping of energetic electrons in the gate-drain access region (in the buffer, on the surface, within passivation). Mechanisms (1.1-1.3) are only slightly accelerated by temperature.

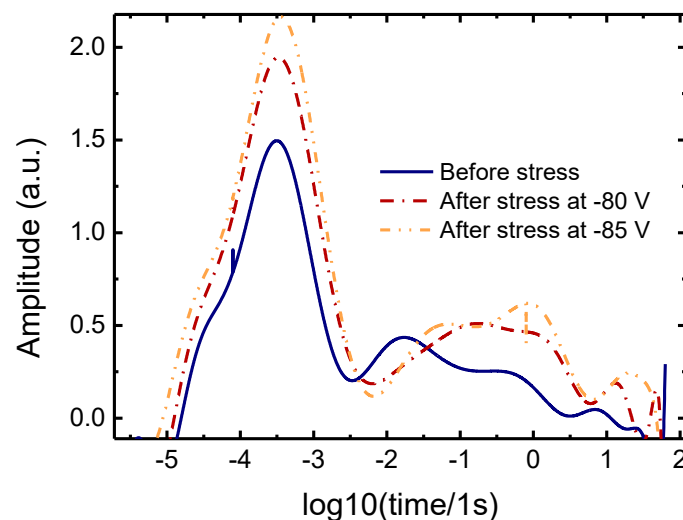


Fig. 7: Time constant spectra of trap states measured at different stages of a step stress experiment, in reverse-bias. Detrapping transients have been measured after a 100 s trapping time, with $V_G = -6$ V, and $V_D = 20$ V.

2.1.2 Trapping and detrapping effects inducing changes in the threshold voltage and transconductance

Permanent or recoverable shifts in threshold voltage and decrease of transconductance, as well as increase of dispersion effects can be consequent to electron or hole trapping and/or generation of new deep levels consequent to various mechanisms, including instabilities due to fluorine, release of hydrogen bound to Ga or N vacancies, hot-electron effects including trapping within the passivation above the gate-drain access region [18].

Fluorine may be introduced by plasma treatments adopted to clean the surface or to remove unwanted SiN in the gate area. In this situation the application of reverse bias may be sufficient to induce a shift of threshold voltage towards negative values. It is believed that part of fluorine is initially interstitial, with a dominant electronegative behaviour which reduces the absolute value of threshold voltage. As the Fluorine moves to the Nitrogen substitutional position F_N^{2+} , the net polarization charge below the gate region increases, pulling the V_{TH} towards more negative values [19].

The effect can be detected by constant reverse voltage stress, as depicted in **Fig. 8**. The time constant for the threshold shift is quite slow, possibly inducing device instabilities and "history" effects: in order to clearly identify the effects on device characteristics, a specific protocol has been devised, i.e. reverse-bias step-stress and constant-stress tests have been performed: during step-stress test, V_G has been stepped from 0V to -30V with 100 s-long 1 V-wide steps, while V_{DS} has been kept to 0V. On the other hand, constant-stress test has been performed applying constant negative V_G , still at $V_{DS}=0V$. Between each step, the characterization suite has been performed as follow: (i) 300s-long de-trapping phase in ON-state bias ($V_G=0V$; $V_{DS}=1V$) in order to de-trap the captured charge during the stress phase, avoiding artifacts during the subsequent threshold voltage measurement; (ii) I_D - V_G characterization (at $V_{DS}=1V$), during which the V_{TH} is calculated as the gate voltage for which I_{DS} equals 1mA/mm; and (iii) reverse-bias gate-source diode characterization to extrapolate gate leakage current (at $V_{GS}=-5V$). The whole step- and constant-stress tests have been performed under halogen light and with a base-plate temperature of 40°C.

The instability is dependent on the applied electric field and mostly consists of a negative threshold voltage shift. Fluorine was suspected as the possible source of instability as these devices adopt a SiN-first process which requires gate window opening by means of SF_6 ICP dry etching. Annealing at 400 °C for 20 s greatly reduces this time-dependent shift, see **Fig. 9**. The role of F was confirmed by testing devices using a gate-first structure without SF_6 treatment, which were not affected by any threshold shift up to -30 V, **Fig. 9**.

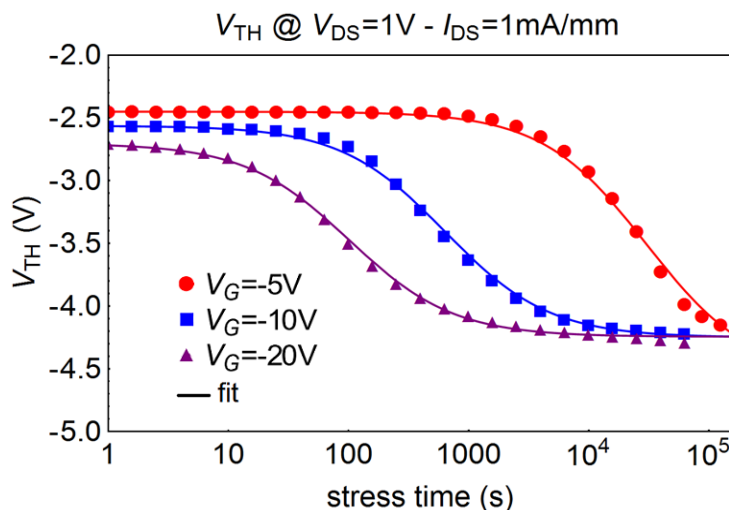


Fig. 8 : Shift of threshold voltage consequent to reverse bias tests at $V_{DS} = 0V$ as a function of time for different values of gate voltage, respectively of -5V, -10V and -20V. Exponential fitting functions are also shown. Devices under test were characterized by a SiN-first gate process (SiN deposition followed by gate window opening by means of SF_6 ICP dry etching).

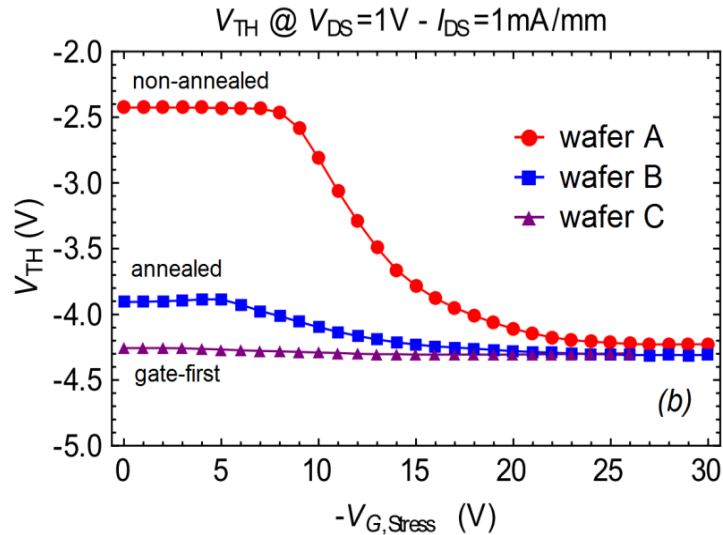


Fig. 9 : Threshold voltage behavior during reverse bias step-stress. Devices without the postannealing (wafer A), those with post-annealing (wafer B) and those without dry etching fluorine treatment (wafer C) experience respectively -1.8 V, -0.4 V and 0 V permanent shift, revealing the likely correlation between the presence of fluorine ions below the gate surface and the permanent threshold voltage shift.

As it will be discussed more in detail in the next paragraph, also energetic electrons may activate or generate new traps in the AlGaIn/GaN epitaxial structure, thus inducing threshold voltage shifts, and/or enhancing current collapse. According to Puzyrev and coauthors [12] hot-electrons induce the release of hydrogen which passivates point defects leading to transconductance degradation and increase in yellow luminescence. A Density Functional Theory (DFT) model has been developed, which explains hot electron degradation in terms of dehydrogenation of the $V_{Ga}-H_3$ defect. According to their model, dehydrogenation of the nitrogen antisite (often present in MOCVD and MBE ammonia-rich growth) would lead to a decrease of the acceptor concentration and to negative shift of the pinch-off voltage. Dehydrogenation of Ga vacancies, on the contrary, would induce positive pinch-off shifts. Such shifts, however, were not observed in all experiments.

Signature of threshold voltage instabilities due to fluorine contamination therefore include: (a) permanent negative threshold voltage shift; (b) long (> 100 s) time constants; (c) dependence on reverse bias electric field in off-state.

2.1.3 Hot-electron effects

Hot electron effects, with generation of deep levels and trapping of electrons in the dielectrics or/and at surfaces and interfaces over the gate-drain access region may occur both during off-state tests or (more frequently) during semi-on and on-state tests.

The term "hot electrons" refers to non-equilibrium electrons which acquire kinetic energy values sufficient to overcome potential energy barriers, be injected into buffer, barrier or insulating layers and be trapped there, break atomic bond and create interface states or activate traps, for instance through dehydrogenation. According to the various experimental conditions, material properties and device weaknesses, hot electrons may give rise both to parametric, gradual, permanent or recoverable positive or negative threshold voltage shifts and/or to decrease of transconductance.

2.1.3.1 Tunneling hot electrons

When traps are present within the AlGa_N layer, and the gate-drain junction is submitted to a high electric field, electrons may be injected from the gate into the channel due to trap- and field-assisted tunneling from the gate. Once injected over the barrier, electrons reach the GaN with a substantial kinetic energy, Fig. 10.

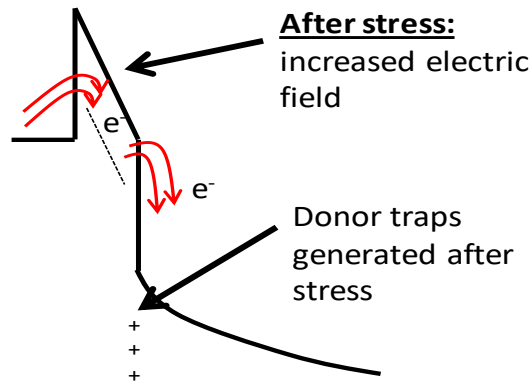


Fig. 10: Schematic band diagram showing generation of donor traps at the AlGa_N/GaN interface consequent to the injection of hot electrons due to trap- and field-assisted tunneling from the gate.

This is a permanent degradation mechanism, enhancing the electric field within the barrier layer, thus resulting in increased gate leakage current. By using suitable test structures, the presence of the donor traps can be detected by C(V) measurements, see Fig. 11 [20].

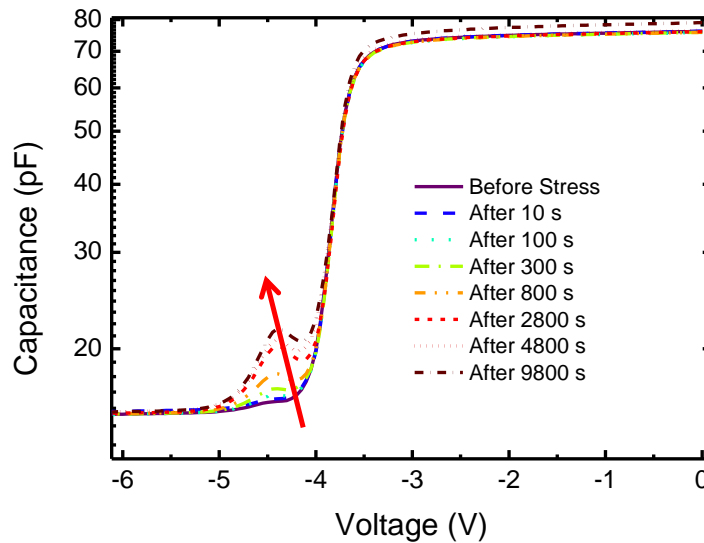


Fig. 11: Evolution of capacitance-voltage characteristics during a reverse bias test at -15 V of an AlGa_N/GaN vertical Schottky diode.

The accumulation of positive charge at the AlGa_N/GaN interface has a series of potential detrimental effects: it increases the electric field within the AlGa_N, shifts the threshold voltage towards negative values, enhances short-channel and punch-through effects, and induces a positive feedback mechanism which may lead to breakdown. A part from the generation of donor traps, other mechanisms may induce the formation of positive charge during reverse bias testing: for instance, recoverable negative shifts of threshold voltage have been observed during reverse bias tests and attributed to the accumulation (trapping) of holes at the AlGa_N/GaN interface, see Fig. 12

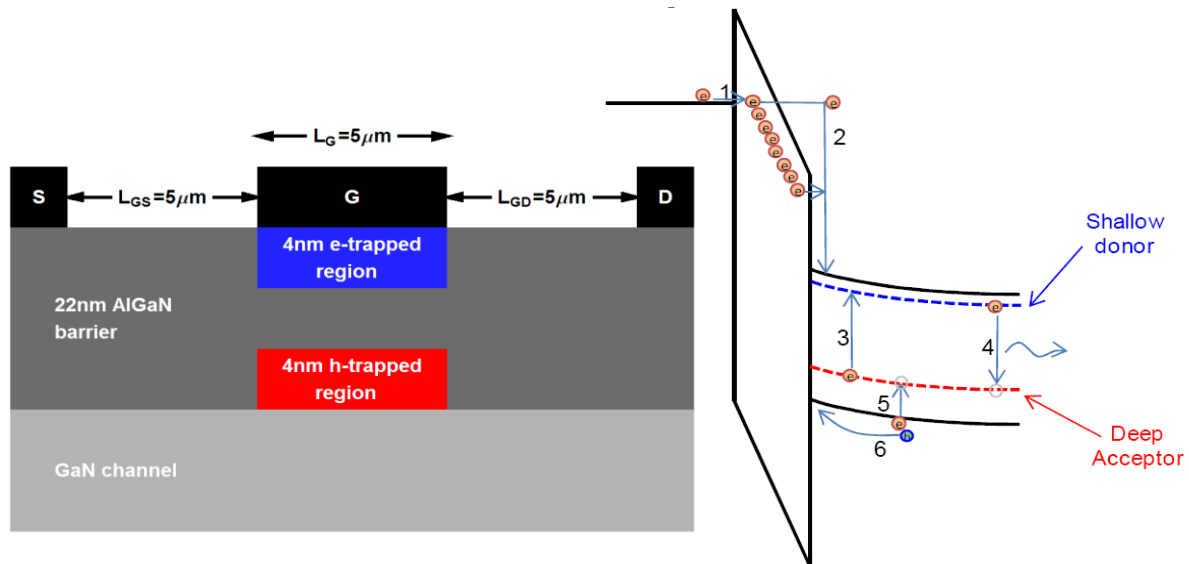


Fig. 12 : Mechanism of creation of a charge dipole within the AlGaN layer in a GaN HEMT structure. (1) Electrons injected by trap- and field-assisted tunneling become partially trapped within the AlGaN. (2) Electrons injected into the GaN become "hot" carriers. (3) Highly energetic carriers can impact ionize deep levels. (4) Transitions between deep levels emit yellow luminescence, experimentally observed, or (5) ionized deep acceptor provide free holes which may be trapped at the AlGaN/GaN interface.

Following this model, electrons injected into the AlGaN due to trap-assisted tunneling would partly be trapped within the AlGaN itself, partly injected as hot electrons in the GaN, see Fig. 12. Within GaN, they would either ionize deep levels or impact-ionize GaN. The resulting holes are trapped at the AlGaN/GaN interface. A charge dipole would consequently result from the trapping of electrons on the surface or within the AlGaN and of holes at the AlGaN/GaN interface, thus explaining the simultaneous decrease of gate current and negative threshold voltage shift observed during reverse bias tests, see Fig. 13.

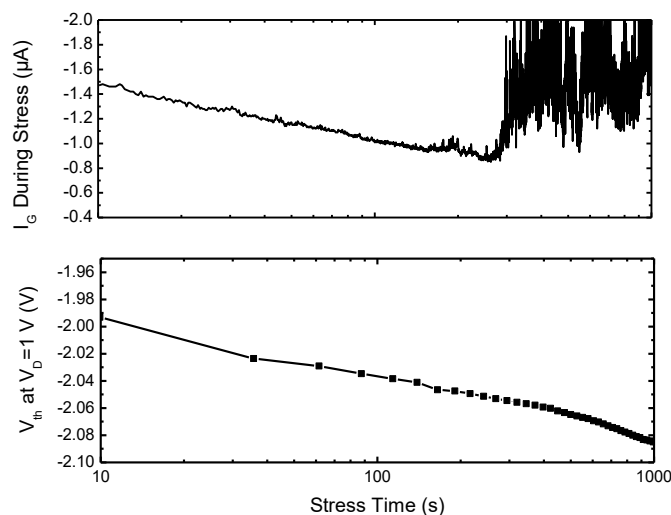


Fig. 13, top: decrease of absolute value of gate current and, bottom: negative shift of threshold voltage observed during a reverse bias test ($V_G = -30$ V, $V_{DS} = 0$ V) of an AlGaN/GaN transistor. Before the occurrence of a catastrophic increase of gate current at $t \approx 200$ s, changes are fully recoverable.

2.1.3.2 Channel Hot Electrons

In a GaN HEMT device where extremely high electric field may be present, channel electrons can reach extremely high energy values, much higher than the lattice thermal equilibrium ones. These “hot electrons” do not remain confined within the channel, Fig. 14: they can be trapped in the AlGaN layer under the gate, or in the gate-drain region where the electric field is maximum, either at the surface or within the silicon nitride passivation layer (2) or in buffer traps (3). At increasing the drain voltage, short-channel effects may take place, gate may lose control of drain current, and a significant gate subthreshold current may flow from source to drain (4).

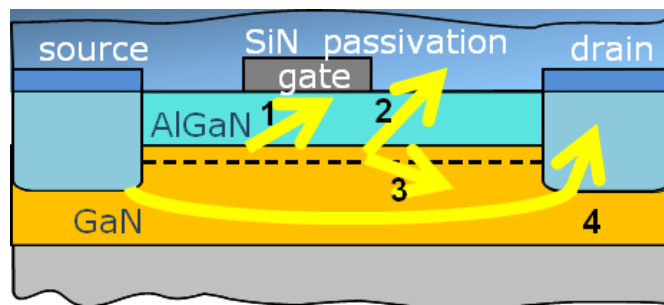


Fig. 14: Schematic HEMT cross-section showing possible mechanisms of hot-electron-induced degradation: defects generation under the gate (1) or in the gate-drain access area (2); electron trapping in the SiN passivation (2); buffer trapping (3); substrate conduction (4).

Hot electron effects can be evaluated by means of electroluminescence microscopy and spectroscopy. During ON-state operation, GaN-HEMTs can emit a weak luminescence signal: light emission is due to the deceleration (Bremsstrahlung) of electrons accelerated by the gate–drain electric field. As a consequence, the EL signal emitted by the devices has a Maxwellian spectrum, reflecting the energetic distribution of the electrons in the channel, Fig. 15. From the slope of the semi-logarithmic EL versus energy plots, it is possible to extrapolate the equivalent temperature of hot electrons. An increase in the drain voltage level determines an obvious increase in the average energy (in the equivalent temperature) of hot electrons.

The EL signal is maximum at the edge of the gate toward the drain [as indicated by the emission micrograph reported in Fig. 16c], i.e., in the region where the electric field peaks. In Fig. 16, we report the dependence of the intensity of the EL signal on the gate voltage for different drain voltage levels. As can be noticed, the EL-VG curve, Fig. 16 (a), has a bell-shaped behavior, which can be explained by considering that EL intensity depends both on the amount of electrons in the channel and on the intensity of the accelerating field. With increasing the gate voltage beyond the pinch-off, the intensity of the luminescence signal increases since the concentration of electrons in the channel (and the drain current) increases. On the other hand, as the gate voltage is increased (beyond 0.8–1 V for the samples under analysis), the gate-to-drain electric field decreases: electrons therefore become less energetic, and the intensity of the luminescence signal decreases accordingly, Fig. 16 (a).

The intensity of the EL signal (Fig. 15) and the equivalent electron temperature provide information on the amount and energetic distribution of hot electrons in the channel: these two parameters can be used to compare different device structures, processing options and bias conditions.

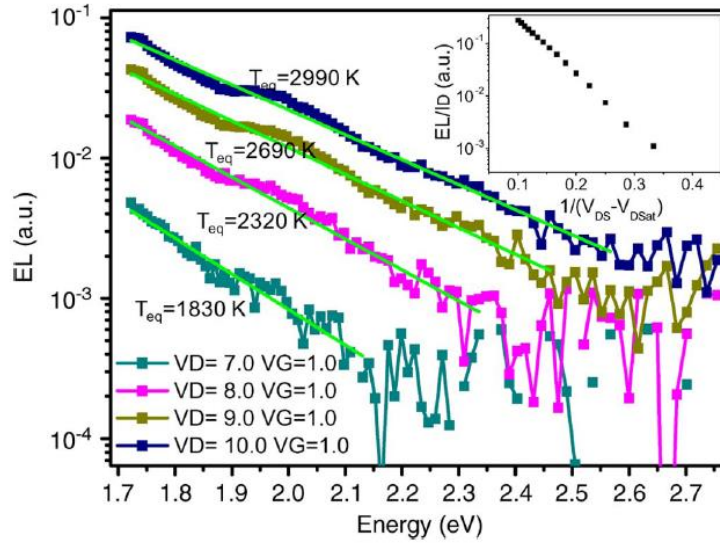


Fig. 15: EL spectra of an AlGaIn/GaN HEMT measured for different drain voltage levels. Equivalent electron temperature values are indicated for the different curves reported in the diagram. (Inset) Dependence of the EL/ID ratio on the reciprocal of the electric field, evaluated by $1/(V_{DS} - V_{DSat})$.

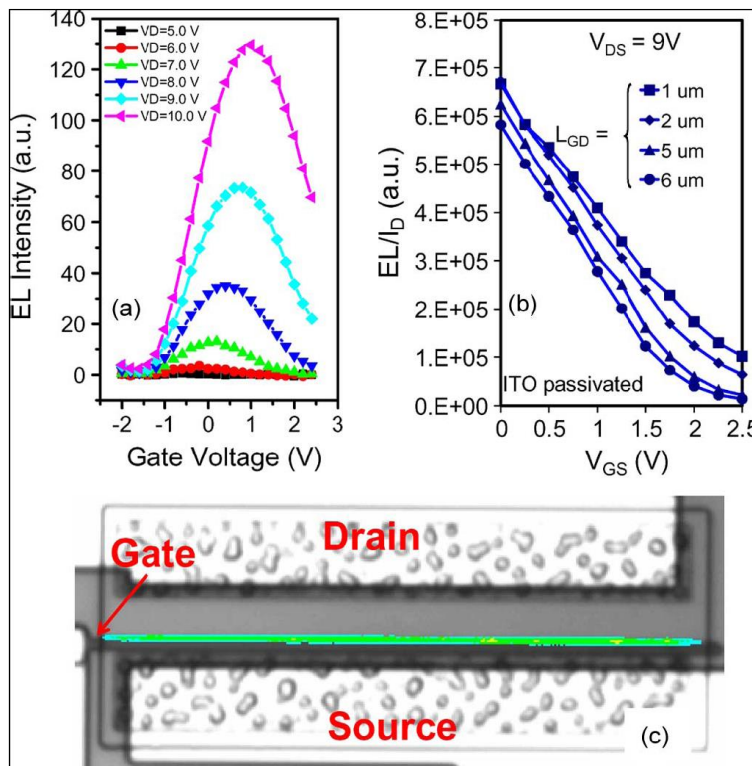


Fig. 16 : Intensity of the EL signal as a function of gate and drain voltage level. (b) EL/ID intensity as a function of the gate voltage level for samples with different gate–drain spacings. (c) False color image reporting the distribution of EL along the gate of one of the analyzed HEMTs. The devices have a transparent ITO gate and are passivated using SiN.

Hot-electron degradation follows the same bell-shaped dependence on V_{GS} shown by EL, see **Errore. L'origine riferimento non è stata trovata.**, which refers to a series of GaN HEMT devices stressed at $V_{DS} = 30$ V at several gate voltage levels. For higher V_{GS} levels, ΔI_D (i.e. the decrease in I_D induced by stress) reaches a maximum and then decreases

(despite the highest dissipated power for $V_{GS} > 0V$), similarly to what is shown by the EL signal, this confirming the role of hot electrons in determining the degradation.

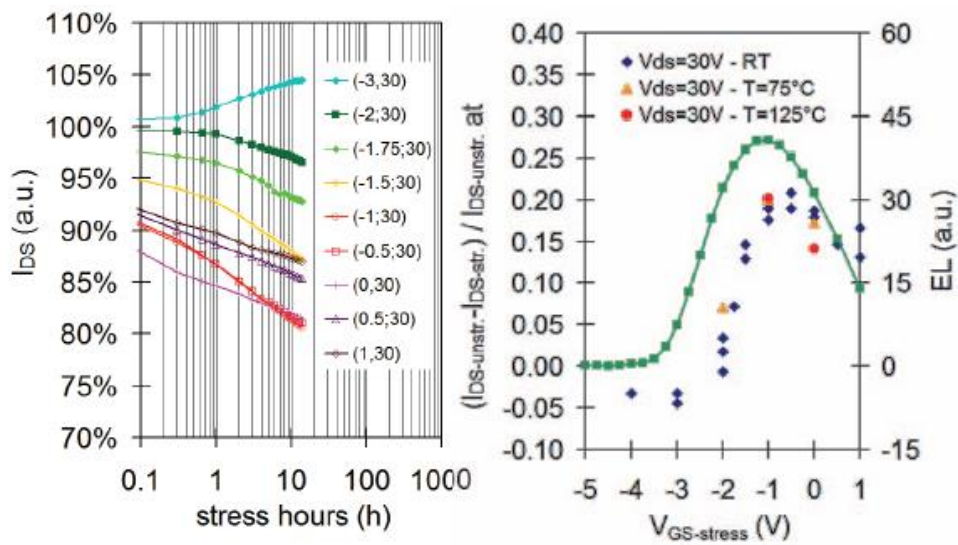


Fig. 17: (left) degradation of drain current measured on identical devices submitted to stress at several gate voltage levels, with a drain voltage of 30 V. (right) Dependence of the EL signal and of the degradation on the gate voltage level used for the stress tests.

The proportionality between the amount of device degradation and the electroluminescence (which is at its turn proportional to the hot electron current component) is maintained at different power dissipation levels, Fig. 18, demonstrating that the observed degradation is not due to thermal effects.

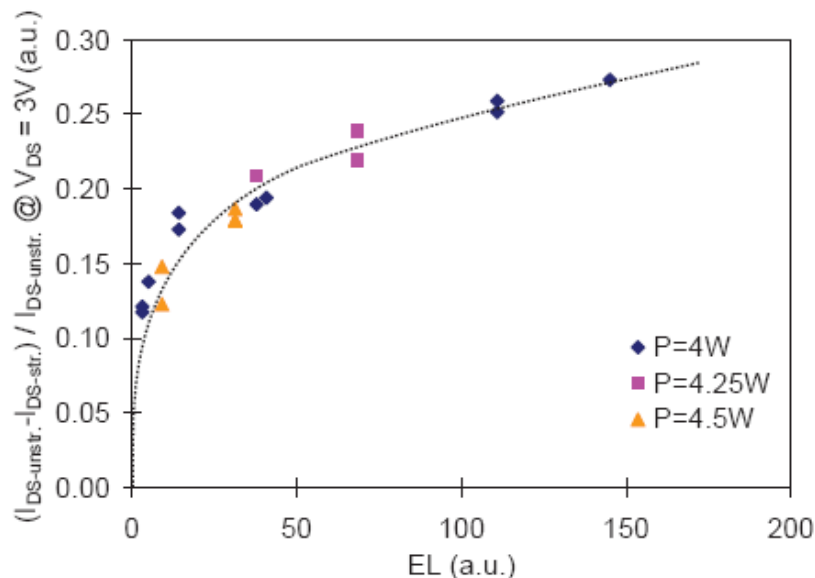


Fig. 18: Correlation between drain current degradation and EL intensity for devices stressed at different levels of dc dissipated power.

Most commonly, hot-electron-induced degradation affects the gate-drain channel region, where the electric field is maximum: in that region, highly-energetic electrons can generate or reactivate defects and/or be trapped by deep levels or in the SiN passivation. If the result

is the growth of a fixed negative charge, DC characterization demonstrates three main effects:

- (i) it depletes the channel, thus increasing drain parasitic resistance
- (ii) it acts as a parasitic gate or field-plate, thus decreasing the electric field in the gate-drain region, Fig. 19 top
- (iii) due to the reduced gate-drain conductance, it affects the maximum value of the transconductance, g_m , and the shape of the g_m vs V_{GS} curve, Fig. 19, bottom

In other cases, new deep levels are formed or activated, and the degradation is detected only as an increase of current collapse or dispersion effects observed by means of double pulse measurements or current Deep Level Transient Spectroscopy.

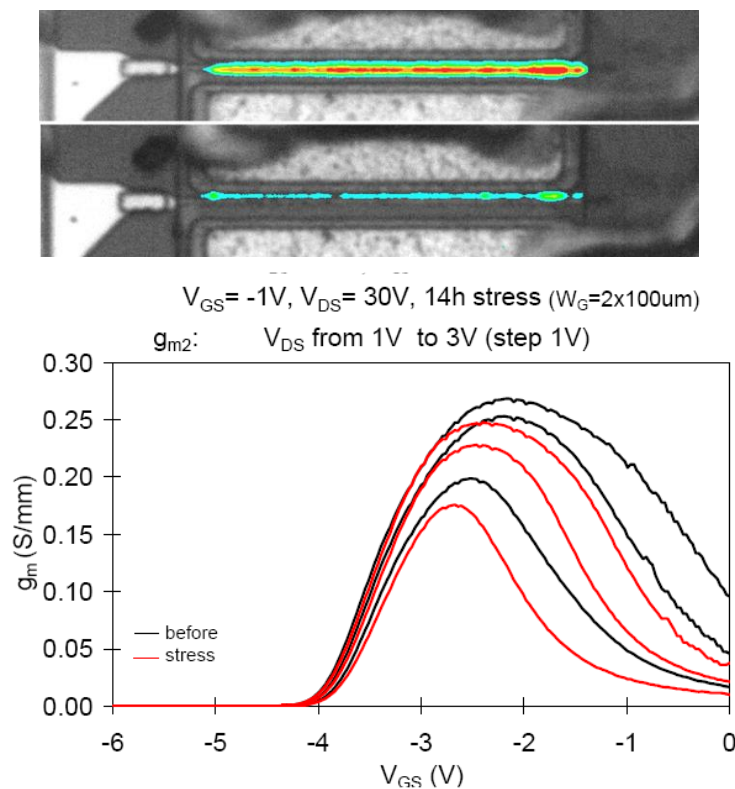


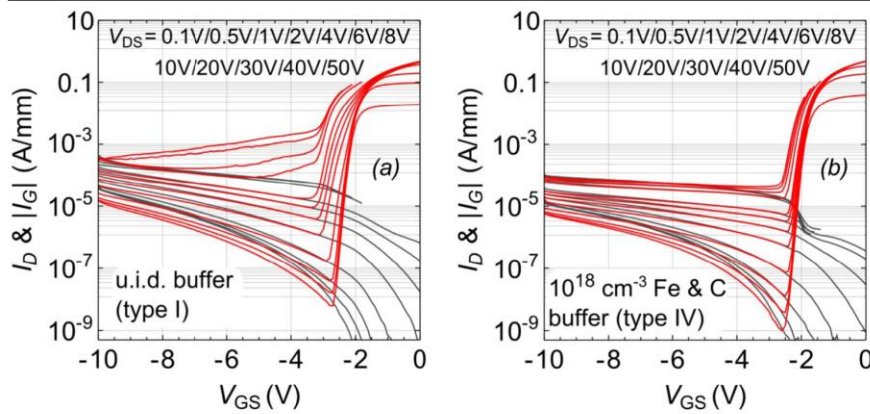
Fig. 19 : top: Electroluminescence image of a GaN HEMT before and after hot-electron test; the EL decrease is consequent to the decrease in the gate-drain electric field induced by negative charge trapping; bottom: Transconductance g_m vs V_{GS} characteristics (measured with V_{DS} in the range 1 V to 3 V, step 1 V) of a 0.25 μm gate-length HEMT. Measurements were taken before and after a 14 h on-state stress at $V_{DS} = 30$ V, $V_{GS} = -1$ V.

2.1.3.3 RF degradation

Hot-electrons degradation plays a major role when the device are actually operated using an rf signal. In fact, an enhancement of hot-electron effects takes place during RF operation when the dynamic load line reaches deep pinch-off conditions, in particular if a device is affected by short-channel effects or poor channel confinement and does not completely turn-off. Different 0.5 μm HEMTs having Ni/Au gate metallization and same processing have been compared; they adopted an AlGaIn/GaN heterostructure with nominal 25% Al concentration and 23 nm AlGaIn thickness, and different buffer compensation, including

either no doping (type I), 10^{17} cm^{-3} C-doping (type II), 10^{17} cm^{-3} Fe-doping (type III), or 10^{18} cm^{-3} Fe and 10^{18} cm^{-3} C co-doping (type IV). A PECVD silicon nitride passivation was employed during the process in order to reduce surface leakage and surface-related current collapse.

Fresh devices from each wafer were subjected to a 24 h CW RF test at 2.5 GHz with quiescent bias at ($V_{DS} = 30 \text{ V}$, $I_D = 30\% I_{DSS}$) and driven into a 6 dB compression point. Base-plate temperature was set to 40°C . Device behaved differently according to the optimization of buffer compensation; in particular, devices with no intentional doping in the buffer presented the worst subthreshold characteristics, with large leakage currents, Fig. 7, left; devices with Fe and C co-doping had optimum turn-off characteristics, Fig. 7, right.



	u.i.d. buffer (type I)	$10^{18} \text{ Fe} \ \& \ 10^{18} \text{ C}$ buffer (type IV)
SS (mV/dec)	91.2	89.2
$ I_{G,LEAK} $ (A/mm)	6.4×10^{-5}	2.4×10^{-5}
DIBL (mV/V)	69.7	22.3
$I_{D,LEAK}$ (A/mm)	1.2×10^{-3}	3.6×10^{-5}
$P_{OUT,init}$ (dBm)	29.15	29.10
PAE_{init} (%)	40.4	41.2
ΔP_{OUT} (dBm)	-1.05	-0.55

Fig. 20: I_D vs V_{GS} and I_G vs V_{GS} characteristics measured at multiple V_{DS} (from 0.1 V to 50 V) for (a) u.i.d. buffer and (b) 10^{18} cm^{-3} Fe- & C-doped buffer HEMTs. Devices with u.i.d. GaN buffer feature higher DIBL, higher I_D leakage, and higher ΔP_{OUT} .

After RF stress, no degradation of DC characteristics was found; on the other hand, pulsed measurements demonstrated an increase of current collapse, which was well correlated, with a few exceptions, with the RF power degradation, Fig. 21 and Fig. 22. A good correlation was verified between initial subthreshold source-to-drain leakage current and RF output power degradation. More in details, double-pulsed g_m vs V_{GS} characteristics (Fig. 23a and Fig. 24a) show that the increase of current dispersion after the RF testing is manifested in the drop of the dynamic transconductance (up to 60% in u.i.d. samples) accompanied by no V_{TH} degradation. As previously noted, the degradation of the dynamic transconductance could be ascribed to the generation of additional trap states localized in the access regions. Thanks to drain current transient spectroscopy (Fig. 23b and Fig. 24b), it can be noticed that the worsening of current-collapse in u.i.d. and 10^{17} cm^{-3} C-doped buffer devices is caused by an increase of the concentration of the traps with activation energy $E_A = 0.79 \text{ eV}$ and capture cross-section $\sigma_c = 6 \times 10^{-13} \text{ cm}^2$ (labelled E3) and $E_A = 0.84 \text{ eV}$, $\sigma_c = 4 \times 10^{-14} \text{ cm}^2$ (labelled E4). On the other hand, though devices with 10^{18} cm^{-3} Fe- and 10^{18} cm^{-3} C co-doping feature higher initial current dispersion (mainly caused by the trap E2, with $E_A = 0.56 \text{ eV}$ and $\sigma_c = 5$

$\times 10^{-15} \text{ cm}^2$), they experience negligible decrease of the dynamic transconductance and negligible increase of trap density after RF operations.

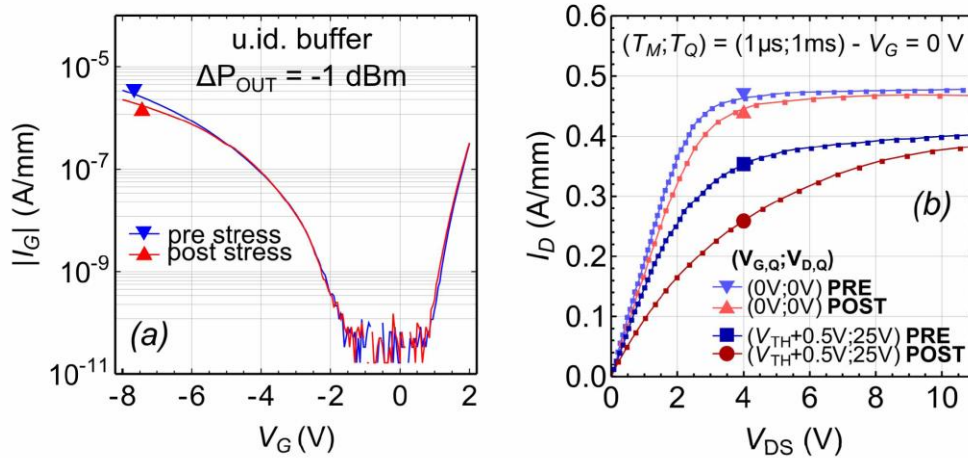


Fig. 21: I_G - V_G characteristics and (b) pulsed I_D vs V_{DS} characteristics acquired prior to and after the stress of a sample with u.i.d. buffer experiencing a ΔP_{OUT} of -1 dBm. No gate-leakage increase and no significant I_{DSS} variation are found. The worsening of the current-collapse is the main evidence of device degradation induced by RF operations.

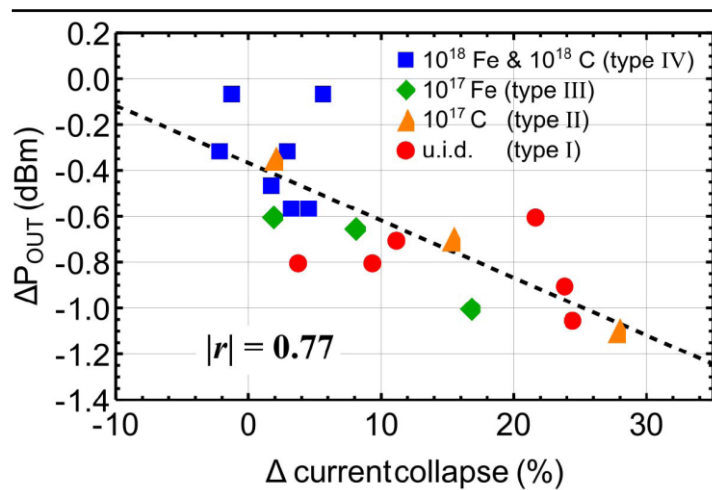


Fig. 22: Good correlation is verified between ΔP_{OUT} and the worsening of current-collapse after RF test.

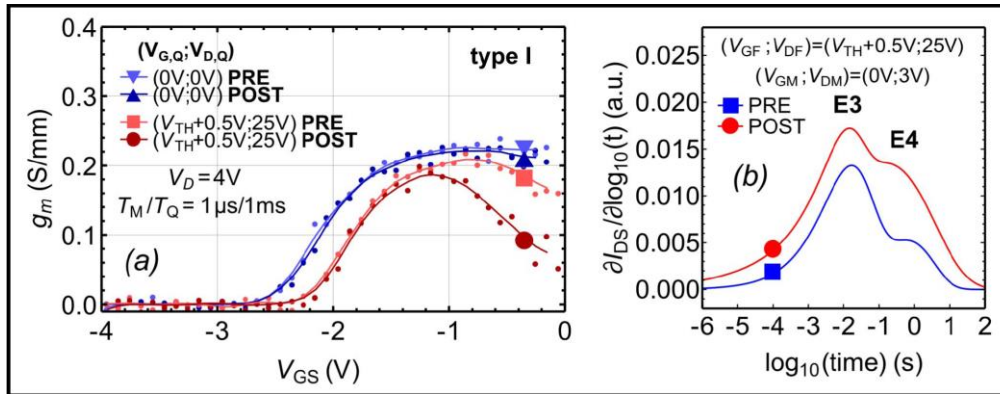


Fig. 23: (a) Pulsed g_m vs V_{GS} characteristics and (b) DCTS performed prior to and after the RF test on a sample with u.i.d. buffer (type I). Stress induces a remarkable g_m droop in the hot quiescent bias-point ($V_{TH}+0.5V; 25V$), with the concentration increase of the pre-existing deep levels E3 and E4.

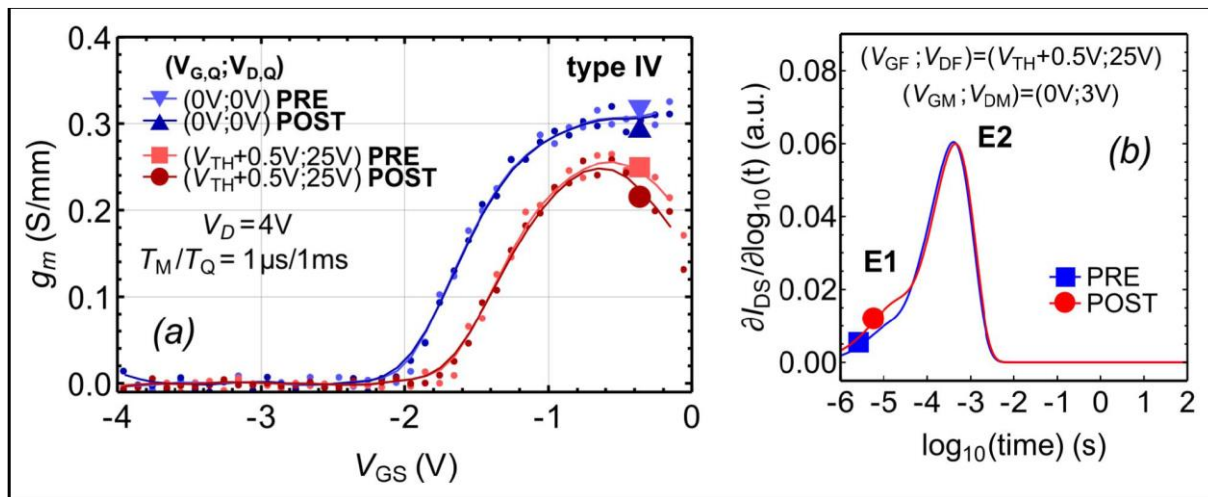


Fig. 24 : (a) Pulsed g_m vs V_{GS} characteristics and (b) DCTS performed prior to and after the RF test on a sample with 10^{18}cm^{-3} Fe- & C-doped buffer (type IV). After the RF test, only 10% g_m droop is found in the hot quiescent bias-point ($V_{TH}+0.5V; 25V$), with slight increase of pre-existing trap E1, and no relevant increase of trap E2.

In conclusion, hot electron effects can induce degradation both in off-state and in on-state. In off-state, hot electron degradation mostly affects the gate area, resulting in the generation of possibly charged deep donor states at the AlGaIn/GaN interface, within the GaN buffer, with permanent increase of gate leakage current and modification of the C(V) profile. Injection of hot electrons from the gate may also induce trapping of holes at the AlGaIn/GaN interface, with recoverable negative threshold voltage shift.

Channel hot electrons (CHE) induce on the contrary trapping of negative charge over the gate-drain access region. Signatures of CHE include permanent or recoverable increase of on-resistance and parasitic drain source resistance, decrease of I_D and g_m ; decrease of electroluminescence and increase of breakdown voltage. The degradation has a “bell-shaped” dependence on gate voltage and DC power, is correlated with electroluminescence and decreases or remains unchanged at increasing temperature. Most dangerous conditions are the “semi-on” ones.

2.2 Electrical characterization procedures

A standard characterization suite for GaN HEMT qualification includes DC measurements of basic device quantities and of most relevant I-V characteristics. Essential measurements are drain current vs drain voltage I_D vs V_{DS} characteristics at various gate-source voltages V_{GS} (output characteristics), I_D - V_{GS} trans-characteristics in linear and saturation region, transconductance g_m vs V_{GS} characteristics in linear and saturation region, sub-threshold $\log(I_D)$ vs V_{GS} characteristics from $V_{GS} = 0$ to a negative voltage corresponding to 1-2 V below pinch-off voltage, I_G vs V_{GS} forward and reverse characteristics of the gate Schottky diode. I-V curves will be measured and stored at each step of accelerated tests; moreover, typical reference point parameters that will be extracted are (data are given just as an example and refer to 0.25 – 0.5 μm technology):

$I_{DSSAT-10}$	saturated drain current at $V_{DS} = 10\text{V}$ and $V_{GS} = 0\text{V}$
$I_{DSSAT-15}$	saturated drain current at $V_{DS} = 15\text{V}$ and $V_{GS} = 0\text{V}$
$g_{mMAX-10}$	transconductance peak at $V_{DS} = 10\text{V}$
$g_{mMAX-15}$	transconductance peak at $V_{DS} = 15\text{V}$
$ I_{G_leakOFF-10} $	absolute value of gate leakage current at $V_{DS} = 10\text{V}$ and $V_{GS} = -7\text{V}$
$I_{DSOFF-10}$	drain current measured in pinch-off condition at $V_{DS} = 10\text{V}$ and $V_{GS} = -7\text{V}$
$ I_{G_leakOFF-15} $	absolute value of gate leakage current at $V_{DS} = 15\text{V}$ and $V_{GS} = -7\text{V}$
$I_{DSOFF-15}$	drain current measured in pinch-off condition at $V_{DS} = 15\text{V}$ and $V_{GS} = -7\text{V}$
V_{TH-2}	threshold voltage measured in linear region at $V_{DS} = 2\text{V}$ and $I_{DS} = 1\text{mA/mm}$
V_{TH-10}	threshold voltage measured in saturation at $V_{DS} = 10\text{V}$ and $I_{DS} = 1\text{mA/mm}$
V_{TH-15}	threshold voltage measured in saturation at $V_{DS} = 15\text{V}$ and $I_{DS} = 1\text{mA/mm}$
$ I_{GS} $	gate-source diode current at $V_G = -7\text{V}$
R_{on}	on-state resistance at $V_{GS} = 0\text{V}$ and $V_{DS} = 0.5\text{V}$

A set of at least 50-100 reference devices is typically characterized on a wafer, in order to have a sufficient number of characterized devices to be submitted to accelerated tests. On a sub-set of devices, pulsed characterization should also be carried out, in order to evaluate current collapse effects and deep levels, and to follow their evolution during tests. There are basically three methods to carry out pulsed measurements :

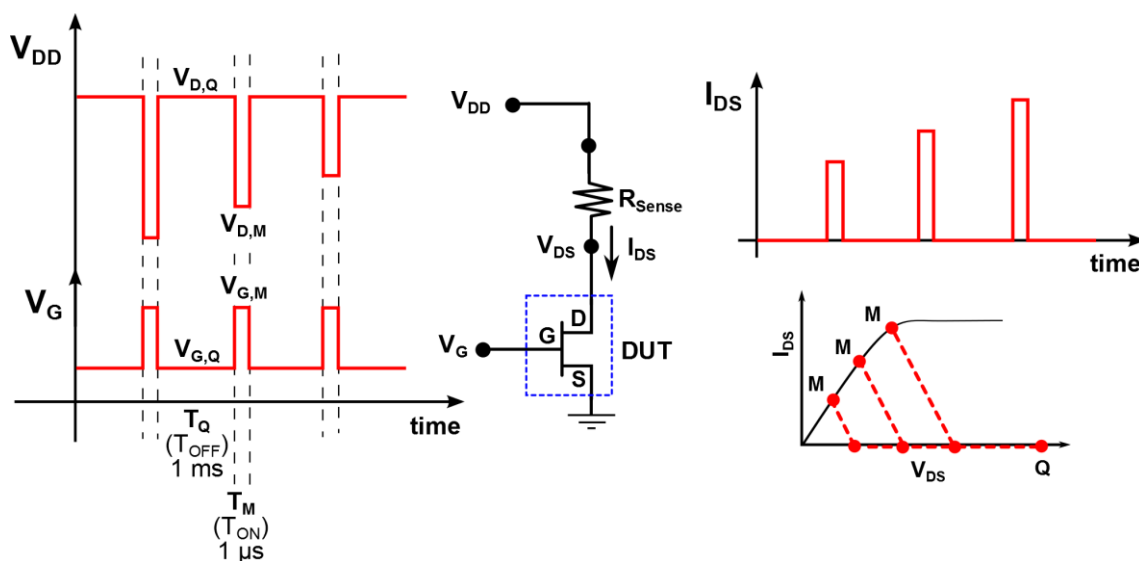


Fig. 25 During double-pulse measurements, both gate and drain voltages are pulsed from a quiescent-bias point ($V_{G,Q};V_{D,Q}$) to a measurement bias point ($V_{G,Q};V_{D,Q}$), and the drain-current (I_{DS}) is acquired as the potential drop across a sense resistor. By tailoring the quiescent and measuring bias-points, it is possible to inhibit or promote charge-trapping mechanisms, and to sweep the whole I_D - V_D and I_D - V_G , respectively.

- for the “load-line” method, a resistive load is applied to the drain of the device, a constant DC voltage is applied to the drain, the gate voltage is pulsed from the off-state (quiescent stress, trapping) conditions (t_{OFF} , $\sim 99\%$ of pulse period T) to the measurement point (t_{ON} , $\sim 1\%$ of T , resulting in an on-state duty cycle of 1%). This method is closer to real operating conditions, but does not allow to separate the effect of gate voltage stress (gate-lag) from that of drain voltage stress (drain-lag). Drain current is sampled at the beginning of the measurement pulse; current collapse is evaluated as the percentage decrease of drain current in “trapped” conditions (after application of $V_{G,Q}$, $V_{D,Q}$ during t_{OFF}) with respect to the “untrapped” ones (after application of $V_{G,Q}=0$ V, $V_{D,Q}=0$ V during t_{OFF})
- in the “double-pulse” method, Fig. 25, both gate and drain voltages are pulsed from a quiescent bias point; by tailoring the quiescent and measuring bias points it is possible to observe the entire pulsed I-V characteristics; stress induced by gate and drain voltage can be separated; the shape of pulsed I_D vs V_{GS} or g_m vs V_{GS} characteristics can provide information on lateral trap location [21]
- the “current transient spectroscopy method”, Fig. 26, the drain-current response is acquired with adequate time resolution over several time decades, so the effect of traps having all possible values of time constants is evaluated. The measurement is repeated over a wide range of temperatures and the activation energy and cross-section of deep levels is derived by plotting time constant values in a suitable Arrhenius plot [9]. By comparison with results reported in the literature, including in particular capacitance Deep Level Transient Spectroscopy data on well characterized material, it is possible to derive hypothesis on the physical origin of the observed deep levels. An extended review is presented in [9]; parasitic thermal effects can significantly affect the results and must be carefully considered [22].

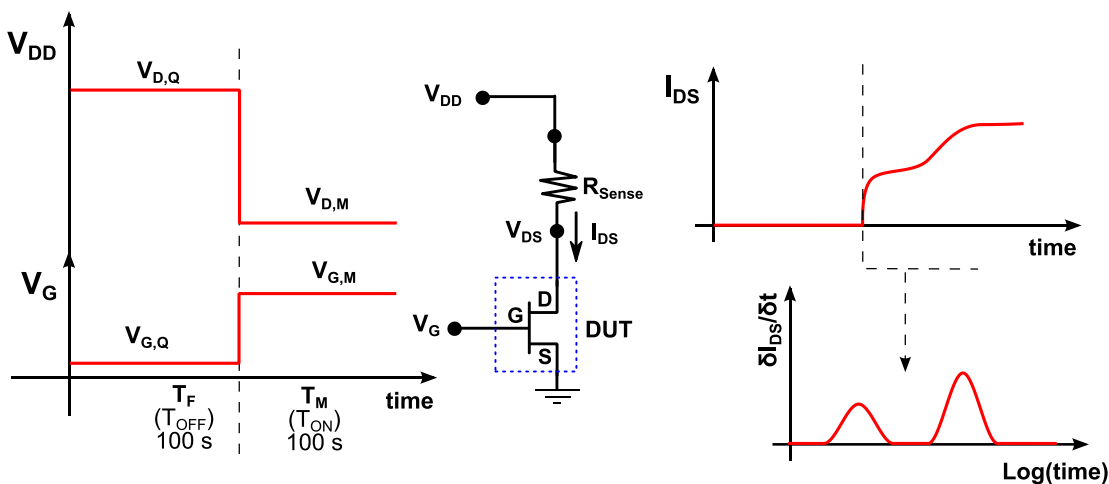


Fig. 26 : Device under test is subjected to a stress/trapping phase ($V_{G,F};V_{DF}$, typically in the off-state or semi-on-state for a period of 100 s); then, it is biased in a low-field, low-power on-state ($V_{G,M};V_{DM}$, typically in linear region, or right after the knee voltage) to permit the acquisition of the drain-current response and the analysis of the related time-constant spectrum.

2.3 Thermal characterization methods

Exact knowledge of channel temperature and its distribution on the die is key factor for correct evaluation of deep level parameters, for predicting operating temperatures and circuit performances, for the evaluation of activation energies of the different failure mechanisms and for the extrapolation of high-temperature accelerated test results to operating temperatures, in particular for what concerns the mean time to failure (MTTF). Unfortunately, at the moment an experimental technique capable of mapping surface and sub-surface device temperature with the adequate lateral and depth resolution is not available, and experimental evaluation has to be coupled with device simulation in order to obtain useful thermal data. Temperature evaluation techniques include : (i) measurement of a temperature dependent electrical parameter; (ii) infrared (IR) thermography; (iii) photoluminescence spectroscopy; (iv) scanning thermal microscopy; (v) electroreflectance thermography and, finally, microRaman spectroscopy. In the following, these techniques are shortly reviewed, together with some notes on GaN HEMT thermal characterization methodology.

2.3.1 Thermal evaluation based on measurement of temperature dependent electrical parameters

These techniques obviously do not offer spatial resolution; the results represent an average on the entire device periphery. As a consequence, the estimated junction temperature value is usually much lower than the peak temperature one. Comparison with simulation is only possible by averaging numerical data, trying to emulate the physical situation corresponding to measurements, with large uncertainties. DC [23], [24] and pulsed methods [25] are reviewed in [26] and compared with IR thermography results; the method proposed by Joh and del Alamo [25], based on pulsed measurement of the drain current and on-resistance R_{ON} provides most reliable values. One must be careful, however, as trapping effects may hinder this measurement or significantly affect the results.

2.3.2 Infrared thermography

IR thermography is based on the detection of thermal radiation emitted from the surface of the device in the 3 μm -10 μm wavelength range, depending on device temperature. This techniques requires exact calibration of the emissivity of the various material present on the devices surface (pixel-by-pixel); optical resolution is limited due to the long wavelength of the emitted radiation. As most semiconductors are transparent in this wavelength range, temperature value is averaged over the entire thickness of the semiconductor. In general, this results in a large underestimation of device temperature [26]. On the other hand, use of the technique is relatively simple; moreover, IR thermography is an imaging technique which allows direct measurements on large area devices, whereas Raman thermography is practical only when measuring small areas (see below); as a consequence, the combined use of the two techniques is not uncommon, with micro-Raman providing a tool to calibrate IR images.

2.3.3 Photoluminescence spectroscopy

In photoluminescence (PL) spectroscopy, hole-electron pairs are generated within the semiconductor by a focused laser beam with photon energy higher than the energy gap of the material [27]. When e-h pairs recombine, light is emitted; since band-edge emission energy depends on temperature, spectroscopic analysis of the photoluminescence signal provides information on local temperature with optical resolution. PL disadvantages are: since above bandgap illumination is used, absorption is significant, and only surface layers can be probed; backside measurements are not possible; the additional photo-induced current can alter device electrical behaviour; photocurrent and high power density laser illumination can add spurious device heating. Conversely, temperature dependence of the absorption band edge can be used to probe temperature in a photocurrent experiment [28], [29].

2.3.4 Scanning thermal microscopy

Scanning thermal microscopy [30] adopts a temperature sensitive tip mounted on an Atomic Force Microscope (AFM). This in principle allows one to reach nanometric resolution; however, since contact is required between the device surface and the detector, measurements can only be carried out on passivated surfaces, and only a very small area can be evaluated. Nevertheless the technique has been applied to thermal characterization of GaN HEMTs [31] and of nanometric structures [32]. Detector design, measurement reproducibility and calibration are complex; in particular the thermal contact resistance between the tip and the device surface has to be minimized and evaluated.

2.3.5 Thermoreflectance

Thermoreflectance (TR) detects a small change in the sample surface reflectivity due to a change in temperature. Change in reflectivity is small and these measurements are usually carried out on the gate metallization, either from the top or, backside, at the metal/AlGaIn interface. It has higher resolution than micro-Raman, can be employed for quasi-static and pulsed measurements, and can produce images with submicron spatial resolution [33]. In [34], the authors use backside illumination and probe the thermoreflectance of the gate metallization at the gate metal/AlGaIn interface. By combining Raman spectroscopy and thermoreflectance measurements, they claim to have developed a calibration procedure which does not require simulation. In fact, Raman and TR are complementary: Raman requires optical access to the semiconductor (see below) so extrapolation using finite element simulations is required when the hot spot at the gate edge is covered by field-plates or air-bridges. Combination of Raman spectroscopy from the top and TR topside and backside would in principle enable complete device thermal mapping, at the expenses of a significantly complicated experimental procedure. Gate temperature can be also evaluated by measuring the changes in gate metal resistance as a function of temperature [35], [36] using a four-point probe configuration, but this requires a special test structure with one (better two) contact pad at each end of the gate finger, in a gate resistance temperature detector (G-RTD) configuration.

2.3.6 Micro-Raman spectroscopy

Micro-Raman (Raman spectroscopy coupled with a suitable laser-based microscopy system) is at the moment the most accurate technique for device temperature evaluation, and is routinely adopted by several research groups and industrial research laboratories to carry out device thermal characterization and calibrate finite element simulation tools. The technique is based on the inelastic scattering of photons consequent to the interaction with quantized lattice vibrations (phonons), see [37] and references therein. The sample is illuminated with monochromatic light; Raman scattering creates or annihilates a phonon; correspondingly, the wavelength of the Raman scattered light, which is detected and analysed by the spectrometer, is shifted with respect to the stimulating wavelength towards higher or lower values (Raman shift). Specific wavelengths can be associated with phonon modes, which depend on the material. Raman shift depends on temperature and on mechanical strain in the lattice. The contributions of temperature and strain to the measured total energy shift of the Raman modes must be evaluated separately, either by calibration (i.e. by evaluate Raman shift due to temperature only in bulk strain free material) or by analysing the thermal response of different phonon modes [37]. Micro-Raman (μ R) thermography has several advantages : (i) it provides temperature mapping with sub-micron lateral spatial resolution ($\sim 0.5 \mu\text{m}$); (ii) it enables one to independently measure thermal properties of materials needed for device thermal simulation; (iii) it can evaluate thermomechanical strain concurrently with temperature measurements; (iv) it can adopt above bandgap or below bandgap laser light, allowing both surface or backside measurements; (v) since Raman spectroscopy is material selective, when below bandgap photon energy is used, the characteristic phonons of each material can be used to simultaneously probe the temperature in each device layer; (iv) it can carry out dynamic measurement, typically with 10 ns time resolution. Still Raman is not a “perfect” technique: Raman scattering is a rare event and measurements require long integration times for each measurement point; thermal mapping requires scanning the laser over the sample and is extremely time consuming; topside observations require optical access to the semiconductor; the lateral resolution of backside observation is much worse due to aberration and diffraction effects. In conclusion, even in the case of Raman thermography, comparison with finite element (FE) thermal simulation is required to determine device channel temperature: the maximum temperature point may not be optically accessible, measured temperature could be lower than the actual one due to spatial averaging, large device thermal mapping is unpractical. For the latter reason, μ R is usually coupled with IR thermography or other techniques [34],[38], [39]. A comparison between μ R, IR and electrical measurements is presented in [40] and [41].

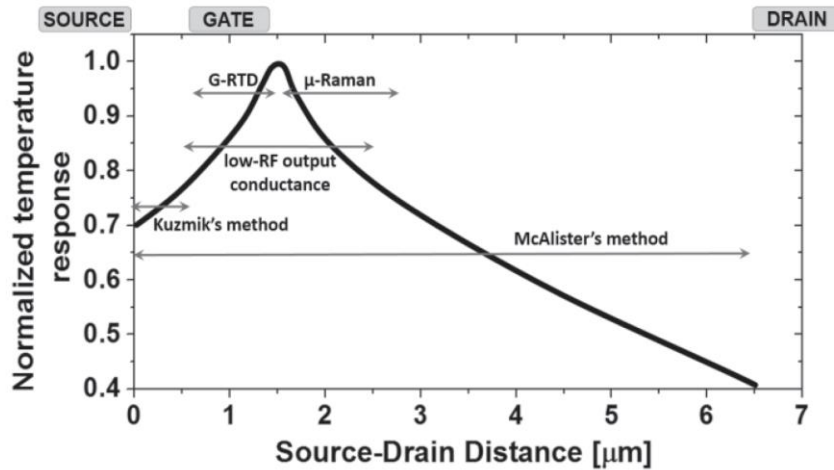


Fig. 27: Simulated source-drain temperature distribution (in the middle of a $0.8 \mu\text{m}$ AlGaIn/GaN HEMT transistor with $0.75 \mu\text{m}$ -long and $5 \mu\text{m}$ -long source-gate and gate-drain gap respectively) for a power dissipation level of 6.5 W/mm . The curve is normalized by the peak temperature. Arrows: expected temperature sensing (averaging) regions for electrical experimental methods. Taken from [41]; G-RTD is gate resistance temperature detector; McAlister and Kuzmik methods are based on DC electrical measurements and are described in [23] and [24] respectively.

2.3.7 Procedures for device thermal evaluation and modeling

As discussed in the previous paragraphs, there is no experimental technique enabling direct measurement of peak device temperature (a task that would require nanometric resolution and full 3D capability) or even mapping of surface temperature with adequate lateral resolution. The commonly adopted solution consists in developing a 2D or 3D finite element model of the device thermal environment (including the device itself, the heatsink, and the package if present) carefully taking into account all interfaces and contacts, trying to evaluate as precisely as possible all thermal conductivities, and to use realistic heat removal boundary conditions.

To build this model, all information is precious; since all techniques have strengths and weaknesses, experimental evaluation is usually carried out using both electrical measurements and all available thermography techniques (being aware of the limitations of each technique). The usual procedure consists in evaluating Joule dissipation within the device in the chosen operating conditions by using a 2D device simulator like Synopsis Sentaurus; derive a model for self-heating elements within the device; typically, a single parallelepiped heater $0.3\text{-}0.5 \mu\text{m}$ -long from the drain edge of the gate contact, $<100 \text{ nm}$ thick can be used for test structures without field plates or at low power dissipation; another block heater should be added under the field plate at higher drain voltages, when the power dissipation extends towards the drain contact. During the calibration phase of the simulation, one should also decide how extended should be the simulated volume of the semiconductor, in order to obtain meaningful results. This of course depends on layout, gate geometry, field-plates etc. in a complex manner. An example is shown in Fig. 28 [42].

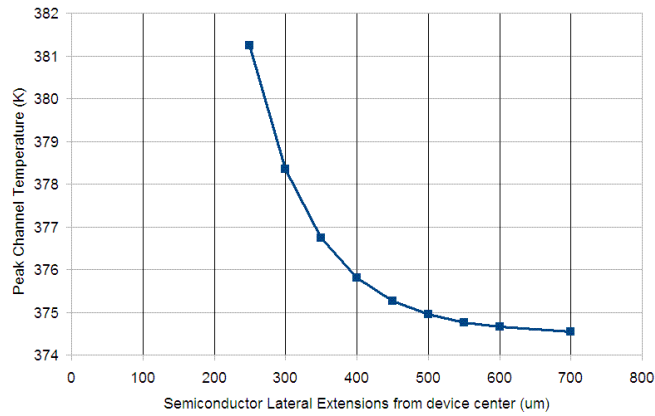


Fig. 28 : Analysis of the dependence of the peak channel temperature from the semiconductor lateral extensions used for thermal simulations. Results refers to a 4 fingers 0.5 μm -gate AlGaIn/GaN device with a 50 μm gate-pitch dissipating a power density of 5W/mm [42].

Mesh sizing is also extremely important; too large mesh values induce temperature underestimation as large as 10°C, depending on the device typical features. For 0.5 μm devices, a 50 nm mesh size was used [42]; lower mesh sizes may be needed for scaled devices. Same considerations apply to the simulated thickness of substrate, to thermal boundary conditions on the wafer backside, etc. Once the finite element simulation environment is set-up, thermal conductivity values initially selected can be adjusted in order to emulate experimental data. A certain degree of arbitrariness exists in this process, as simulation results will have to be spatially averaged in order to be compared to experimental results. The shape and extension of the average depends on the adopted technique, the electrical conditions, device layout etc. From this point of view microRaman has the advantage of offering the best lateral resolution, and the capability of directly measuring some thermal properties of the materials. Fig. 29 shows the ratio between peak gate temperature as evaluated by microRaman, and T_{peak} value obtained by finite element simulation, after spatial averaging [37]. The difference between microRaman values and simulated ones shrinks as the number of fingers increases.

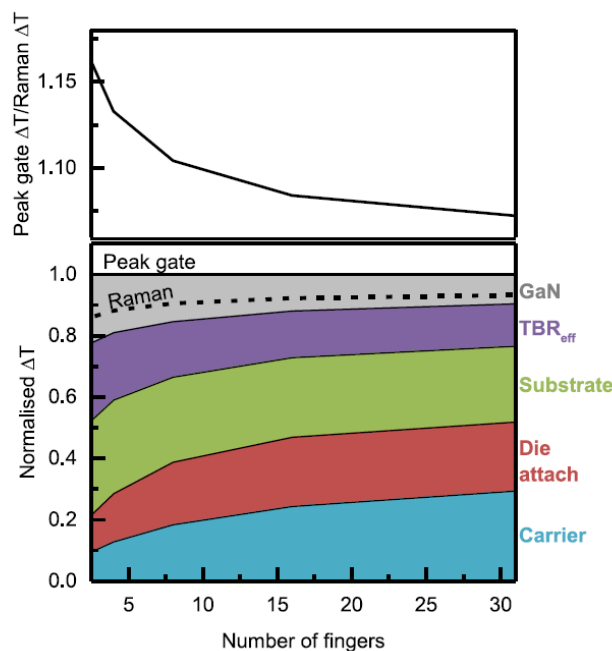


Fig. 29 Simulated temperature rise in a packaged GaN HEMT on a 100 μ m thick SiC substrate, shown as a function of number of gate fingers at a constant power dissipation density of 11W/mm. The ratio between the peak gate temperature rise and spatially averaged temperature rise, equivalent to a Raman thermography measurement, is shown. The temperature across each layer in the device stack is also shown, normalized to the peak gate temperature. A eutectic die attach and CuW carrier are included, representing the package. Taken from [37].

2.4 Short-term (<100 h) on-wafer accelerated tests

During technology development, and before starting a wide reliability evaluation campaign, on-wafer short-term tests can provide extremely useful information for the subsequent in-depth and long-term analysis:

- By carrying out step-stress tests, absolute maximum I_D , V_{DS} and DC dissipated power which could be applied during accelerated tests without inducing immediate device catastrophic failure can be identified
- By carrying out DC tests at various operating bias points, identification of failure modes in on-state, off-state and semi-on state can be carried out; preliminary identification of accelerating factors and failure mechanisms may be also possible. On-wafer tests provide fast feedback to process engineers and device designers
- On-wafer load-pull testing at various compression levels enables the identification of specific failure mechanisms which can not be detected during DC tests

2.4.1 Step-stress tests

Before starting reliability tests, failure criteria must be defined. Typical values are for instance 10%-20% drain current and/or transconductance degradation, 100X increase of gate leakage current, 20%-30% increase of current collapse. When production devices are studied, failure criteria should be tailored according to reliability goals and device applications; for research purposes, the level of degradation reached during accelerated testing is usually higher, in order to achieve good chances of identifying the failure mechanisms involved by means of subsequent analysis.

A typical DC step-stress test requires approximately 30 fully characterized devices, to be submitted to test at three bias points, in off-state, semi-on state ($V_G > V_{TH}$) and on-state. For each bias point, drain voltage is increased from 10 V to device failure in 5 V or 10 V steps, 2 minutes each. During the test, drain and gate current should be monitored; electroluminescence microscopy can be used to check whether the current is evenly distributed during the test, if there are hot spots, to identify the threshold for the onset of hot electrons and to find failure location, Fig. 30.

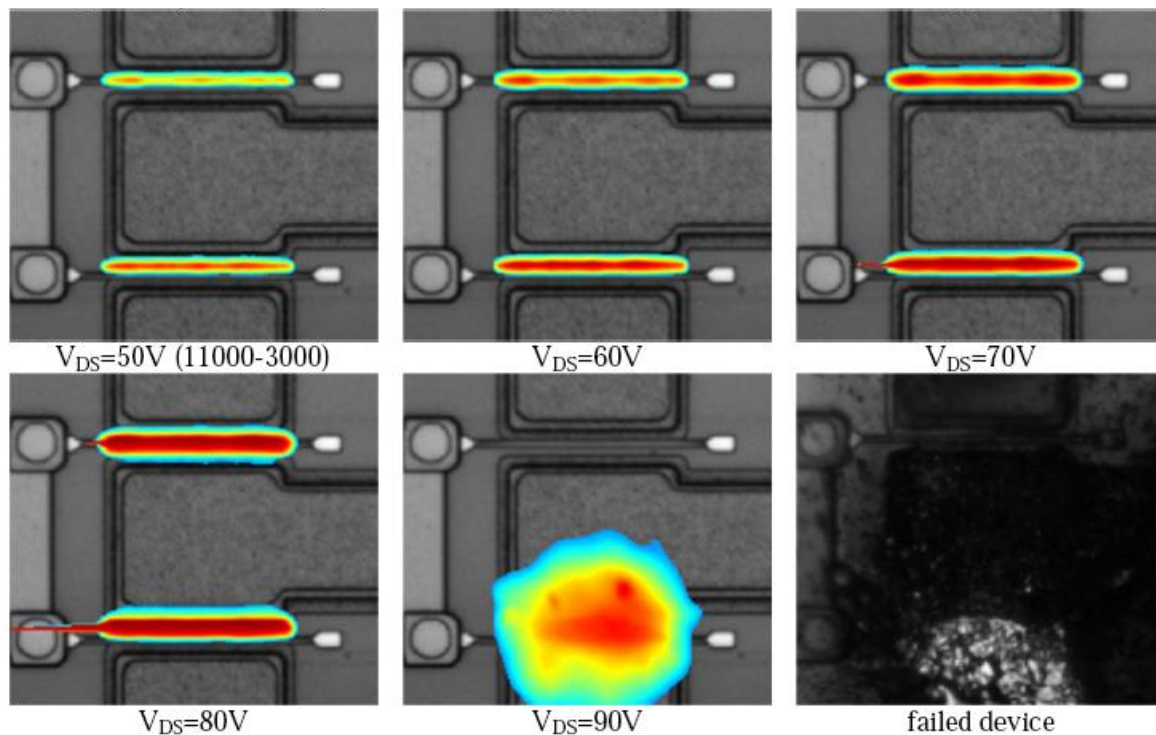


Fig. 30: Emission microscopy images of a 0.25 μm -gate AlGaIn/GaN test device during step stress tests at $V_{GS} = -2$ V, V_{DS} from 50 V to 90 V.

Step-stress tests indicate power and voltage limits that can not be surpassed during subsequent on-wafer testing. Short-term DC on-wafer test (typically 1-24 h) can be accomplished either by choosing V_{GS} and V_{DS} bias points on an iso-power line (constant power dissipation, conditions varying from “high current, low electric field and no hot electrons” to “medium-low current, high electric field and hot electrons”) or by keeping V_{DS} constant and increasing V_{GS} from pinch-off to 0 V (moving from “high electric field, no current, no power dissipation, few hot electrons” to “low electric field, high current, high power dissipation, few hot electrons”). In the latter case, if degradation is due to hot electrons, device degradation will have a non-monotonic behaviour as a function of V_{GS} , as shown in [11], as semi-on conditions correspond to maximum hot electron generation. Another test consists in evaluating 24h degradation at increasing V_{DS} with V_{GS} constant, thus enhancing at the same time power dissipation and electric field. If thermal resistance is known, power dissipation can be translated into (average) junction temperature, and device temperature limits can be found, providing a guide for subsequent long-term testing, see Fig. 31 and Fig. 32. Results shown in Fig. 32 clearly show that a thermally-activated mechanism is responsible for device degradation in the technology under development, thus ruling out hot electron effects, which are not thermally activated or have a negative activation energy. It should be noted, however, that other factors may contribute to accelerate degradation, and that extreme accelerating conditions are applied during these short-term tests, which are not present under typical device operation. Moreover, medium energy electrons may achieve higher energies at higher temperatures, thus possibly reaching threshold for defects formation, dehydrogenation or activation.

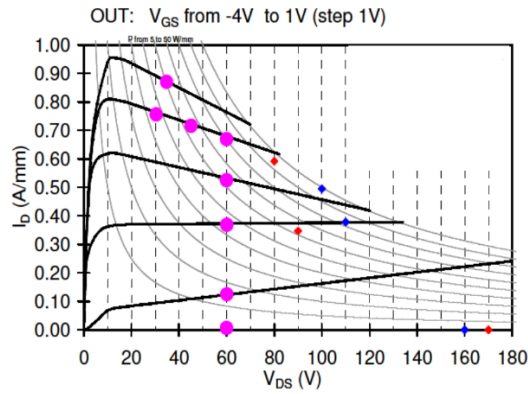


Fig. 31: DC output characteristics of a typical 0.25 μm -gate device; blue and red diamonds correspond to I_D - V_{DS} values at burnout during step-stress tests in two different device technologies. Iso-power curves are plotted in grey from 5 W/mm to 50 W/mm. Dots correspond to bias points for on-wafer 24h tests.

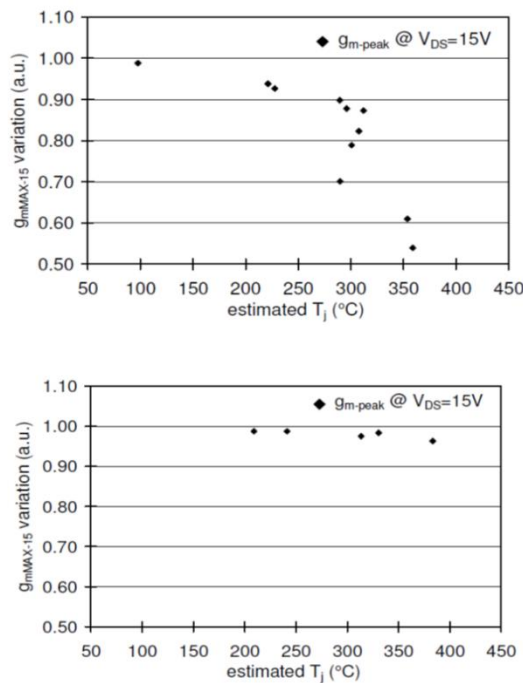


Fig. 32 : Relative transconductance degradation after 24 hours on-wafer tests on 0.25 μm -gate AlGaIn/GaN HEMTs at various bias conditions, as a function of the junction temperature. Top: first device generation; bottom: improved technology devices. Average temperature has been evaluated from power dissipation using the thermal resistance derived by calibrated finite element simulation. As it can be seen, the improved technology is sufficiently stable to be submitted to long-term tests at elevated (350°C) junction temperatures.

2.5 Long-term accelerated tests

Short-term tests are useful for identifying early failures during technology development, in order to correct material, process and device design intrinsic and extrinsic weaknesses; for stabilized processes, extremely accelerated conditions are used, in order to obtain information concerning possible failure mode and mechanisms of the technology under study in short time. Those modes and mechanisms, however, may be not representative of

operating conditions; moreover, short-term test do not provide any information on degradation kinetics, activation energies, mean time to failures and their extrapolation models. In order to get confidence on the reliability of a specific technology, long-term (>1000 h) tests are required, increasing significantly the complexity of the reliability evaluation process, requiring adequate device packaging and specialized test equipments or burn-in systems. A reliability campaign for GaN-based devices normally includes :

HTST, High Temperature Storage Tests: three-temperatures storage tests to be carried out on wafers (no package required, unless the backend reliability has to be evaluated) in air or in controlled atmosphere. GaN technology is stable at high temperature, so storage temperatures above 300°C are typically adopted. Target failure modes/mechanisms are : changes in Schottky barrier height due to metal-semiconductor interdiffusion at the Schottky gate; increase of ohmic contact resistance, delamination of passivation layers due to thermomechanical stress, contaminants indiffusion. Three temperature values are used in order to be able to derive the activation energy (or energies) of the involved degradation mechanisms

HTRB, High Temperature Reverse Bias: packaged devices are tested in off-state at elevated temperature, at drain and negative gate voltages significantly higher than the nominal value, resulting in high electric field, but low or negligible current. This accelerates gate edge and trap-induced degradation effects (converse piezoelectric effect, GaN oxidation and surface dissolution, time dependent gate breakdown induced by defects percolative path formation, threshold shifts due to trapping)

DC HTOL, High Temperature Operating Life tests: packaged devices are tested in on-state at elevated temperature, at different bias points, with the aim of identifying the effect of electron current density and of hot electrons (reaching energies much higher than the equilibrium value) by comparison with thermal storage tests results. Ideally, a set of bias points should be identified, (i) keeping the operating point constant and changing the temperature; (ii) keeping the temperature approximately constant along an iso-power line; (iii) keeping V_{DS} fixed and changing V_{GS} . Since a significant number of devices is needed for each bias points for statistics, the cost of this test may increase rapidly

RF HTOL, High temperature operating life test with rf signal applied, with the devices biased in class A or class AB, using input power at relevant frequency and corresponding to device peak added efficiency (as evaluated by load pull testing)

The reliability campaign can also include biased/unbiased tests at different relative humidity (RH) , like 85°C/85 RH in a suitable environmental chamber; unbiased HAST test in autoclave, to study corrosion phenomena, High Forward Gate Current test (HFGC) to emulate forward gate current taking place during rf overdrive in compression; DC and rf overstress effects, Electro Static Discharge testing [43]. Space and avionics qualification require study of GaN HEMT radiation hardness, which is beyond the scope of the present document. An extensive review of radiation effects on GaN devices can be found in [44].

All the above mentioned tests, except thermal storage, require device packaging; in the case of rf testing, either a 50-ohm matched dynamic evaluation circuit (DEC) consisting of a single-stage rf amplifier or the use of matching impedance networks may be needed. Packaging quality has to be evaluated, in particular for what concerns die-attach, which may substantially affect thermal resistance. X-ray micrography of package is usually adopted to

this purpose. The thermal characterization procedure previously described in Section 2.3 for devices on-wafer has to be repeated for packaged devices; time resolved thermal evaluation enables separation of the die/package and package/sink contributions to thermal resistance; finite element modelling again provides a tool for the evaluation of different layouts and package solutions.

2.6 Failure analysis methodology and techniques

Failure analysis of scaled GaN HEMTs is not an easy task: many degradation mechanisms are related to trapping effects or to the generation of point defects, which are extremely difficult to observe, even using high resolution Transmission Electron Microscopy (HR-TEM) [45], [46], [47], [48], [49]; when more extended lattice damage is created, the defective area has an extension of few nm. Delayering for sample preparation is complicated, as etchants commonly used for Si or other III-V compounds are ineffective for GaN. Starting from a very detailed analysis of electrical failure modes, a failure analysis methodology can be defined, which should be able to identify the failure mechanisms involved. A possible procedure is sketched in Fig. 33.

Increase of gate leakage (with or without correlation with drain current degradation) is either a signature of point defects formation and percolative conductive path [8] or of structural degradation consequent to high-power and high-temperature stress, and possibly related to electrochemical surface degradation, extending into the epitaxial structure due to strain [50], and can be related to diffusion processes [51]. Electroluminescence microscopy can be a suitable tool to identify leakage paths either by topside or backside observation [52], [53]; physical damage (dimples, grooves, pits, trenches and cracks) [54], [55], [56], [57], [58], [59], [60], [61] can be studied in detail by recurring to Transmission Electron Microscopy (TEM) observation. This implies cross-sectioning the device by Focused Ion Beam (FIB), (usually combined with mechanical polishing and etching in order to reduce damage). High-angle annular dark-field (ADF) scanning transmission electron microscopy (HAADF-STEM) can provide images which are easily interpreted since it avoids electron interference and multiple electron scattering. A high-performance STEM instrument provides a resolution better than 0.05 nm. A combined use with electron energy loss spectroscopy (EELS), which uses electrons transmitted through the center hole of the ADF detector, enables element analysis column by column. EELS can also provide information about the presence of additional energy levels such as defect levels [45]. Chemical analysis can be implemented using Energy Dispersive Spectroscopy (EDS) or other techniques, enabling for instance the observation of oxygen, responsible for GaN surface dissolution.

Conversely, a faster and effective way to observe physical damage without recurring to TEM observation consists in completely removing device passivation and metallization by wet etching and then observing the surface by SEM and Atomic Force Microscopy (AFM). Surface erosion then becomes detectable in degraded samples, while control (untreated) samples do not show voids or pits. Defective areas look different according to the etchant adopted for metal removal (either TFAC, ferric cyanide (FeCN)/potassium iodide (KI) [50] or Aqua Regia [54]; one should also take into account that an enlargement of the defective area is unavoidable during the etching process.

2.6.1 Materials related characterization

Other techniques may be useful for materials and devices characterization. Even if these techniques have not been used for GaN HEMT failure analysis, they proved to be useful for the correlation of material properties with deep levels and parasitic effects. The presence of yellow band and/or blue band in the cathodoluminescence spectra of the epitaxial structure of GaN HEMTs has been correlated with kink effects in device I-V characteristics [62] and with deep levels formation after reverse bias testing [63]. Secondary Ion Mass Spectroscopy (SIMS) profiling of impurities and GaN buffer compensation dopants (Fe, C) is also relevant for a possible correlation with deep level effects such as current collapse, and with degradation mechanisms induced by hot electrons [13],[14],[64],[65].

2.7 Theoretical models and device simulation tools

Physical modeling of degradation processes, and comparison with results of 2D device simulations are extremely helpful for the understanding of GaN HEMT reliability. Several TCAD framework for 2D/3D simulation of GaN devices are commercially available, but no environment can provide the capability of emulating all observed failure modes or, even more challenging, of predicting degradation. Consequently, several research groups have developed new models targeting different physical aspects of GaN devices behavior and reliability (the following are just examples, as the review of GaN material and device simulation research activities would require an entire white book :

- *ab initio* modeling of defects and impurities in GaN lattice (and related compounds), providing information on the position of deep levels energy within the bandgap, which can be compared, for instance, with Deep Level Transient Spectroscopy (DLTS), cathodoluminescence, photoluminescence and photocurrent results [66][67]
- models concerning mechanisms of formation of electrically active deep levels consequent to high temperature or hot electron stress, due for instance to dehydrogenation of defects [12], [15], [68], [69], [12]
- models analyzing the physical effects of DC and rf electrical stress, e.g. thermomechanical strain due to piezoelectric and thermal mismatch effects, [70][2][71] or hot electron energy distribution using Monte Carlo simulations, in order to check which degradation mechanisms can be activated [72] [73], [74], [75], [76].
- drift-diffusion and hydrodynamic 2D models aimed at identifying the effect of traps in terms of : trap nature, cross-section and energy level within the bandgap; lateral location of traps (under the gate, in the S-G and G-D access region), vertical location of traps (surface, AlGaIn, GaN buffer) [42], [77]–[82]

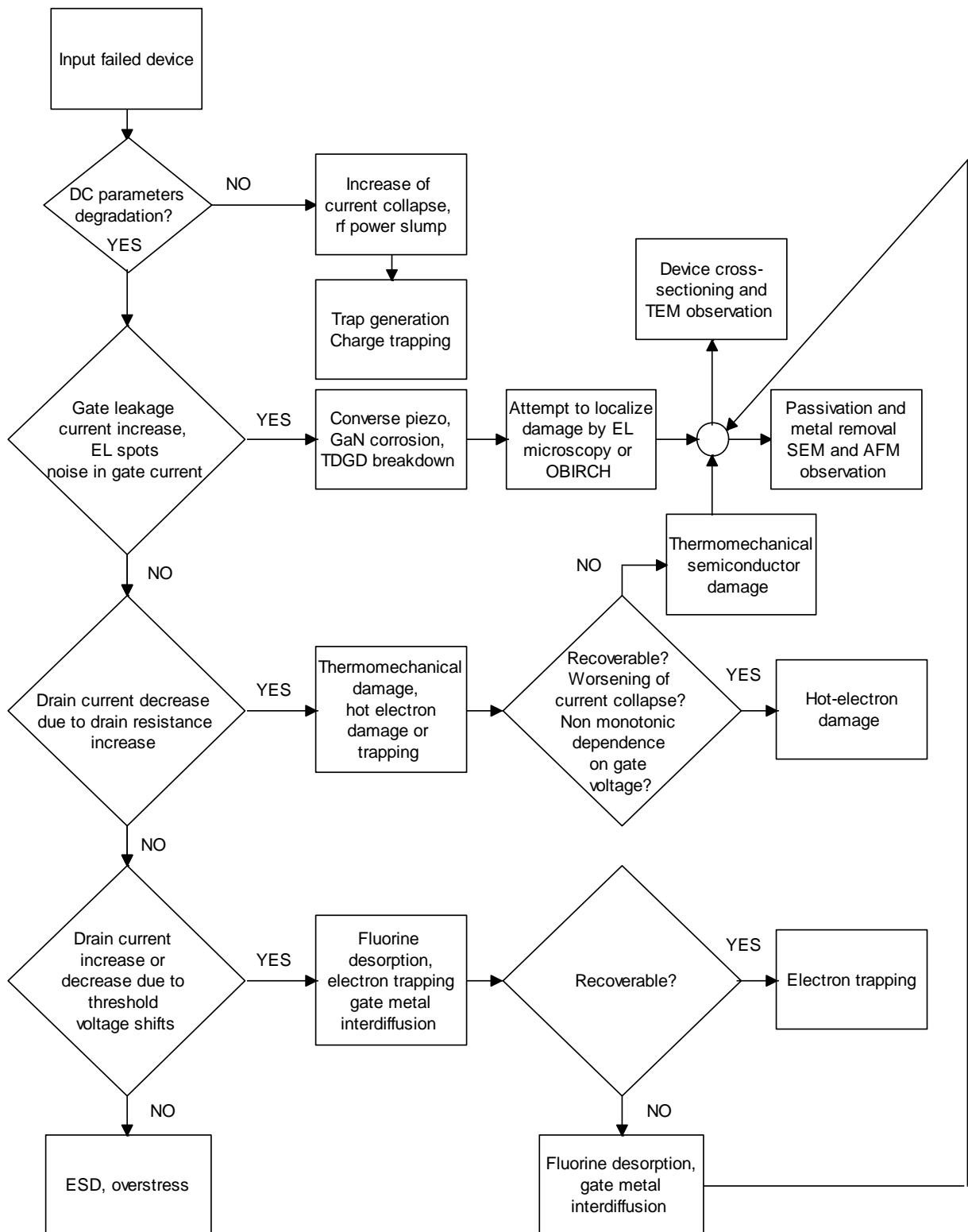


Fig. 33 : A possible flow-chart for failure analysis of GaN HEMTs. OBIRCH = Optical Beam Induced Resistance Change; TDGD = Time Dependent Gate Degradation; EL = Electroluminescence; ESD = Electro Static Discharge; TEM = Transmission Electron Microscopy; SEM = Scanning Electron Microscopy; AFM = Atomic Force Microscopy.

2D drift-diffusion simulation allows the most versatile and relatively simple approach to the emulation of current collapse effects and degradation mechanisms; in order to capture the details of failure physics however, like hot electron effects or transfer of energetic electrons into GaN buffer and trapping therein, more sophisticated models like hydrodynamic [81], [83] and Monte Carlo models are required. Monte Carlo in particular is the only method which enables a rigorous study of dynamic effects, device scaling, hot electron phenomena and, in general, all problems which require a reliable evaluation of electron energy distribution [73]–[76], [84]–[87].

2.8 Relevant papers and conferences concerning reliability of GaN hemt for rf applications

A list of essential references follows:

Gate edge degradation : [1], [4],[8],[17],[54],[55],[88],[89]

Electrochemical GaN reactions : [5]

Time dependent gate breakdown: [3],

Deep levels and defects: [9], [21],[62],[90]

Hot electrons: [11], [12]–[15], [64],[66]

Thermal measurements: [25][37]

Radiation effects [44]

Transmission Electron Microscopy [45],[61], [91]

Electroluminescence [52], [53]

Modeling and simulation [80], [85], [87]

Relevant Conferences

IEEE International Reliability Physics Symposium (IRPS)

European Symposium on Reliability, Failure Physics and analysis (ESREF)

International Conference on Compound Semiconductor Manufacturing Technology (MANTECH)

Annual Reliability of Compound Semiconductors Workshop (ROCS)

International Workshop on Nitrides (IWN) – even years

International Conference on Nitride Semiconductors (ICNS) – odd years

SPIE Photonics West

MRS Symposia

International Symposium on Testing and Failure Analysis (ISTFA)

International Symposium on the Physical and Failure Analysis of Integrated Circuits (IPFA)

3. STATE OF THE ART CONCERNING GaN HEMT FOR RF APPLICATIONS

3.1 Leading labs and university research groups involved in GaN HEMT reliability research in USA

In the following, some US University research groups with intense activity on the reliability of GaN devices are quoted. The list is by no means exhaustive; reported data are taken from scientific literature or bibliographical data base for each group; most recent results and highlights are quoted

3.1.1 MIT (Prof. Jesús A. del Alamo, Thomas Palacios)

MIT is involved in research on the reliability of GaN HEMTs since 2005 approximately. Prof. Jesús A. del Alamo (IEEE Fellow) and collaborators first identified gate current degradation mechanism and attributed it to converse piezoelectric effect; carried out rf testing of GaN HEMTs and correlated it to DC results; extensively studied trapping effects and related characterization methods. In collaboration with Triquint, Jesús A. del Alamo identified cracks and pits in GaN HEMTs submitted to accelerated testing. They developed a reliable electrical method for GaN HEMT thermal characterization, and models for strain, voltage and temperature dependence of defect formation. They identified activation energy of drain-current degradation in GaN HEMT under high-power stress and studied the reliability of InAlN/GaN HEMTs. More recently, Prof. del Alamo extended his study to GaN devices for switching applications, including dynamic on-resistance effects, positive and negative bias temperature instability effects (PBTI and NBTI). Prof. Tomas Palacios (IEEE Fellow) is involved in research on GaN devices since year 2001; he has an in-depth knowledge of GaN technology and GaN devices processing, developed during his PhD at UCSB. He contributed to develop several processes for the fabrication of high frequency AlGaIn/GaN HEMTs. He collaborated with ASU researchers in the study of the effects of threading dislocations on AlGaIn/GaN HEMTs. Tomas Palacios is involved in the study of GaN reliability since 2010. He investigated electric field distribution by means of electroluminescence, the role of oxygen in the off-state degradation of AlGaIn/GaN high electron mobility transistors, the impact of moisture and fluorocarbon passivation on the current collapse of AlGaIn/GaN HEMTs. He contributed to identify the electrochemical reactions leading to off-state degradation of AlGaIn/GaN HEMTs and to develop a model of fabrication and operation-induced mechanical stress in AlGaIn/GaN transistors. His research group also set up a system for the dynamic thermal characterization of GaN HEMTs by means of microRaman thermometry. More recently, he developed vertical GaN-on-GaN transistors based on a “fin” structure and started an analysis of trapping effects in these devices. The MIT group has outstanding capabilities in GaN device physics, processing, device fabrication, reliability evaluation and reliability physics. They have capability of prolonged device testing (an Accel RF system with 4 channels) and other equipments; the group is eminently experimental, but has device modeling experience.

Relevant publications :

Prof. del Alamo : [1], [55], [89], [92]–[95][96], [97]

Prof. Palacios : [55], [89], [98]–[101][102], [103]

3.1.2 Arizona State University (Steve Goodnick, Molly Mc Carthy, Fernando Ponce, Bob Nemanich, Marco Saraniti, David Smith)

Outstanding expertise in materials and devices microscopy, analysis and device simulation is available at Arizona State University. The Monte Carlo (MC) group (Steve Goodnick, IEEE and Alexander von Humboldt Fellow, Marco Saraniti) developed a full-band MC simulator

for GaN, which has been applied to the study of high field transport in AlGaIn/GaN HEMT, to the evaluation of scaled GaN HEMT structures, including short channel effects, and to the evaluation of N-polar structure. Reliability has been extensively studied (effects of dislocations, hot electron effects). Simulations of polarization charge has been compared to experimental results obtained by means of electron holography in a TEM, the latter implemented by Prof. David Smith and collaborators at ASU. A self-consistent harmonic balance / Monte Carlo environment has been developed for RF device performance and applied to the study of scaled high-frequency devices up to the THz range.

The microscopy group (Molly Mc Carthy, Fernando Ponce, Dave Smith) is a worldwide reference for TEM observation and analysis of GaN materials and devices. They are studying the quality of freestanding and homoepitaxial GaN for vertical devices, defects induced by proton irradiation on GaN HEMTs, effects of source field plate on off-state stressed GaN HEMTs. They developed electron holography techniques for the study of polarization charge, electric field in GaN nanostructure and devices.

Bob Nemanich is a leading expert in the field of GaN material characterization, surface analysis, band structure and alignment identification by different spectroscopy techniques, including microRaman, photoemission microscopy, XPS, photoluminescence.

This group of researcher at ASU represent an excellent asset for what concerns knowledge on GaN materials, TEM observation and failure analysis, spectroscopy techniques, detailed physics-based device simulation. Device electrical testing or accelerated testing is not carried out at ASU, which has therefore complementary expertise with respect to MIT.

Relevant publications: [73]–[75], [84], [85], [87],[16], [57], [91], [104], [105], [106].

3.1.3 Ohio State University (S.A. Ringel, A.R. Arehart)

The group at Ohio State has a long-term expertise in the analysis of deep levels in GaN and related compounds, the correlation with parasitic effects like current collapse, the influence of deep levels on device DC and rf characteristics. They collaborated with QORVO on the DLTS and DLOS (Deep Levels Optical Spectroscopy) analysis of devices submitted to reliability tests. They worked together with Vanderbilt University and UCSB (J. Speck) on the study of the degradation effects of GaN HEMT MBE grown on N-rich or Ga-rich GaN and on the study of the radiation hardness of GaN devices. They set up a series of techniques for the in-situ analysis of deep levels concurrently with short-term aging and DC, pulsed and rf characterization. Ohio State is a reference center of excellence for study of deep level effects in semiconductors and in particular in GaN.

Relevant publications: [90], [107]–[114]

3.1.4 Vanderbilt University (D.M. Fleetwood, S.T. Pantelides, R.D. Schrimpf et al.)

Vanderbilt University has a wide expertise in different field of GaN characterization, testing, reliability and radiation hardness. They conducted a wide test campaign on the effects of high energy protons on GaN devices

They studied the influence of impurities like oxygen on the reliability of AlGaIn/GaN HEMTs. They developed models based on Density Functional Theory (DFT) for the study of defects and substitutional impurities like iron and their effect on hot electron GaN HEMT degradation. They proposed the model based on dehydrogenation of defects to explain hot electron degradation of GaN HEMT. They developed methods based on 1/f noise

measurements for the characterization of deep level effects and degradation in GaN HEMTs. Vanderbilt University is a center of excellence for what concerns GaN defects and deep level characterization and modeling and radiation hardness testing of GaN-based devices.

Relevant publications : [12], [15], [64], [69], [107], [109], [115]–[119]

3.1.5 University of Florida (D.J. Cheney, E.A. Douglas, S.J. Pearton, F. Ren et al)

The University of Florida has a long experience in the study of GaN HEMT reliability, including DC and rf testing (with capabilities of long term testing), electrical characterization, study of parasitic effects, failure analysis (cathodoluminescence, TEM in collaboration with D. Smith), deep levels characterization (DLTS, DLOS) and radiation hardness (electrons, protons, heavy ions). Their work focused on gate current degradation effects, formation of pits and voids consequent off-state, on-state and RF testing, hot electron effects, passivation properties. The group is eminently experimental, with some capabilities of modeling (they developed an electromechanical model for GaN HEMT). University of Florida is a center of excellence for the study of GaN HEMT reliability.

Relevant publications : [7], [16], [120]–[127]

3.2 University of Padova research results, facilities, researchers

The microelectronics group of the Department of Information Engineering at the University of Padova started working on GaN HEMTs devices in 1998 and since that time has developed a state of the art testing laboratory for the detailed investigation of parasitic effects and reliability issues in GaN and related compounds.

In particular, we have carried out a systematic study of parasitic effects (mainly gate leakage and trapping) in GaN-based devices, and recently we defined a data base of GaN related traps enabling a fast comparison of data referring to a specific technology with all literature data and with the data we have gathered in the course of our activity. 2D TCAD device simulation is systematically adopted to understand the effects of material properties, of deep levels and of device design modifications; our tools have been calibrated for GaN through the comparison with experimental results of a number of experiments on a very wide set of different technologies. We have identified main failure mechanisms of GaN HEMTs for microwave applications and related tools and methods for reliability analysis of GaN microwave devices in the framework of several projects of the European Defense Agency (EDA) and of the European Space Agency on the validation of 0.5 μm and 0.25 μm GaN HEMT technology. We intensively studied time-dependent breakdown effects in GaN HEMTs [3],[4],[8], hot-electron damage after long-term tests [10],[11], hot-electron damage induced by rf operation [14] failures affecting gate edge in GaN HEMTs [17], reliability degradation consequent to fluorine dry etching [19], electroluminescence evaluation of hot electron effects [21], device thermal characterization techniques [26], ESD and overstress in GaN HEMTs [43], general GaN HEMT reliability [128], [65], [129],[130].

We have been working on semiconductor device reliability, failure physics and failure analysis (of Si, GaAs, SiC and GaN electronic and optoelectronic devices) for more than 30 years; on these topics we published more than 500 papers.

We coordinated/are coordinating the European effort on reliability of the EDA projects KORRIGAN, MANGA and EUGANIC.

University of Padova has a long tradition of collaboration with Japanese companies and research laboratories having worked/working with NTT Photonics Lab (InP HEMTs) and with Panasonic R&D (GaN GITs, GaN lasers) for several years, under collaboration research contracts. You may find what was possible to publish concerning these collaborations in the literature; other results have been kept confidential.

Currently we also have a bilateral research contract with Nagoya University (prof. Hiroshi Amano) concerning development of vertical GaN devices.

For what concerns study of GaN HEMT failure physics and reliability, our most recent projects which have been concluded are the following (there are many many others):

European Space Agency contract 40000106310 Validation of a 0.25 μm GaN HEMT technology

for rf applications, including development of techniques for the study of failure mechanisms, thermal characterization, radiation hardness, 2D simulations.

Duration 42 months, budget 500 kEURO

one-to-one contract with a (confidential) industrial partner on validation of GaAs pseudomorphic technology

including study of thermally activated mechanisms and DC/rf testing.

Duration 12 months, budget 110 kEURO

U.S. Office of Naval Research project

"GaN HEMT reliability physics: from failure mechanisms to testing methods, test structures and acceleration laws", Award No.: N000141410647, under the supervision of Dr. Paul Maki

Duration 12 months, budget 450 kUSD

Facilities at University of Padova

The Microelectronics Laboratory at the Department of Information Engineering at the University of Padua covers an area of approximately 500 m^2 , currently divided into four main areas: (i) DC, rf and pulsed electrical characterization lab; (ii) accelerated testing laboratory; (iii) electroluminescence and other optical characterization techniques for electron devices; (iv) optoelectronics. The electrical characterization lab is equipped with 10 DC and rf microprobe systems and 12 semiconductor parameter analyzers, enabling measurements from 1 fA, 0.2 μV to 8 mA/3000 V or 20 A/ 40 V. An Agilent E8361A 10MHz-67GHz Network Analyzer (PNA) is used for small-signal rf characterization; an external partner provides load-pull power device characterization. Parasitic effects due to traps are characterized by means of the double-pulse technique, i.e. by pulsing synchronously the gate and the drain and measuring the dynamic device I-V characteristics, or by biasing the device with a fixed VDD supply voltage and load-line, by pulsing the gate. For a detailed analysis of deep levels, current and capacitance Deep Level Transient Spectroscopy are adopted [9].

The accelerated testing laboratory includes 6 environmental chambers for thermal biased or unbiased storage tests from RT to 250°C in controlled atmosphere, 4 furnaces for test up to 1200°C, two 400-liters, RT to 280°C chambers and one Vorsch VCL 7000 85°C – 85 RH humidity test system.

Two automatic life-test systems are specifically adopted for long-term (>1000 hours) reliability tests on microwave devices: (a) an i-Test DC burn-in system with 12 positions for DC stress, each including a drain source module with 120 W power, from 120 V, 1 A to 30

V, 4 A and a gate-source power module with a maximum output +/- 20 V and 200 mA; baseplate temperature can go from 0°C to 175°C. (b) an Accel RF AARTS system with 8 DC channels + 2 rf. In the latter case the drain module has a 60 W power capability and 100 V max voltage; the gate module provides +/- 18 V, up to 150 mA. Temperature can be controlled in a 50°C to 250°C range. For rf testbeds, a two-channel RF distribution unit is available with 1.5 GHz to 10GHz bandwidth. The modules can deliver up to +30dBm RF input drive to each DUT in the 1.5 to 10 GHz frequency range.

The optical characterization laboratory has three electroluminescence microscopy and spectroscopy systems for the characterization of hot-electron and breakdown effects, and for failure analysis. Photoluminescence and photocurrent systems are also employed to study the quality of epitaxial material for both electronic and optoelectronic devices. Electrical overstress and Electro Static Discharge, as well as breakdown pulsed I-V characteristics are evaluated by means of a Transmission Line Pulse (TLP) systems providing 100 ns pulses with sub-ns rise time, and enabling dynamic I-V evaluation in a 50 ohm environment using time-domain reflectometric techniques.

Enrico Zanoni, IEEE Fellow

Enrico Zanoni, was born in Legnago (Verona) in 1956, graduated in Physics summa cum laude at the University of Modena in 1982. Since 1997 he has been full professor of Microelectronics at the Department of Information Engineering of the Univ. of Padova. Author or co-author of more than 500 papers published on international journals or presented at international conferences, coeditor of the book "Flash Memories" (P. Cappelletti, C. Golla, P. Olivo, E. Zanoni eds, Kluwer Academic Publishers) and coauthor of 7 book chapters. Coauthor of more than 80 invited papers at international conferences. The ISI Web of Science database reports 332 records by E. Zanoni in the 1986-2014 timespan, which have been cited as reference 2926 times, excluding self-citations, with an h-index of 30. He was or is committee member for the following conferences: IEDM 1995, 1996, 2008, 2009; ESSDERC 1997, 1998, 2000; ESREF 1996, 2000, 2004; SPIE Photonics West 2015; ESSDERC 2014. He has been member of the editorial board of Microelectronics Reliability. He has been principal investigator of the Human Capital and Mobility project "Study of impact-ionization in Si, Si-Ge, AlGaAs/GaAs BJTs and in lattice-matched and pseudomorphic HEMTs" (1994) and of the SMT ESPRIT III project PROPHECY "Procedures for the early phase evaluation of reliability of electronic components by means of CECC rules" (1998). From 2004 to 2008 he was the European coordinator of the subproject "Reliability" for the project "Key Organisation for Research on Integrated Circuits in GaN Technology" (KORRIGAN), finalized to the development of a European power GaN microwave HEMT technology, financed by the European Defence Agency. From 2009 to 2014 he has been European coordinator of the subproject "Reliability" for the project "Manufacturable GaN" (MANGA), financed by the European Defence Agency. He has been responsible for several research projects finance by U.S. government agencies. The research group at the University of Padova, DEI has been active in the field of characterization, modeling, reliability physics and failure analysis of electron devices since 1982, and has been involved in the study of the reliability of GaN electronic and optoelectronic devices since 1999, cooperating with major Universities and research centers and with industrial laboratories.

Gaudenzio Meneghesso IEEE Fellow

His research interests involves mainly the Electrical characterization, modeling and reliability of several semiconductors devices: a) microwave and optoelectronics devices on III-V and III-N; b) RF-MEMS switches for reconfigurable antenna arrays; c) Electrostatic discharge (ESD) protection structures for CMOS and SMART POWER integrated circuits including

ElectroMagnetic interference issues; d) organic semiconductors devices; e) photovoltaic solar cells based on various materials. Within these activities he published more than 600 technical papers and he has been invited to present his research activities in more than 80 International conferences. He is also co-author of eight papers which got the best paper award. He has been serving since 2005 for the IEEE International Reliability Physics (IRPS) Symposium, being TPC Chair of the Compound Semiconductor from 2008 to 2010, and since 2009 he has been member of the management committee. He was the General Chair of HETECH 2001, WOCSDICE 2007, HETECH 2009, ESREF 2012, WOCSEMMAD 2013, TWHM 2013, ESSDERC 2015. He has been elevated to IEEE Fellow class 2013, with the following citation: “for contributions to the reliability physics of compound semiconductors devices”.

4. GaN HEMT RELIABILITY RESEARCH PLAN

This Section contains the proposal for a research plan on the evaluation of the reliability of GaN HEMT for microwave applications.

The main objectives of this plan are the following:

- (i) Develop a methodology for the study of the reliability of scaled GaN microwave transistors, i.e. identification of deep level effects and related techniques, identification of main failure mechanisms, failure analysis and physical modeling of failure mechanisms and definition of acceleration laws. Transfer of this methodology to the industrial laboratory and/or related laboratories
- (ii) study of specific failure mechanisms, with specific interest at most dangerous effects for scaled GaN HEMTs: (a) thermally activated metal-semiconductor interaction effects; (b) hot-electron-induced effects; (c) time-dependent breakdown effects.

The plan has an incremental structure, starting from essential activities and then widening the scope of the plan and, consequently, the effort required. The plan is organized in four phases; the following short description of each phase includes an outline of the activities, the general focus, the results to be obtained. I also indicated “long-term” results which indicate the final research objective.

Phase 1 ($t_0 \rightarrow t_0+9$)

Includes: set-up of characterization methods, device selection and procurement, thermal characterization, untreated devices characterization;

Focus: experimental and theoretical study of deep level effects on device performances, including the effects of compensating species such as Fe and C, back barriers, field plates. Includes 2D physical device modeling, provided details on device structure are known on the basis of an NDA.

Results: analysis of deep levels present in the device and their effect on device DC and rf performances; comparison of deep level effects in different epi structures/suppliers; understanding the influence of device design on deep level effects.

Long-term results: understanding the physical origin of deep level effects

Phase 2 ($t_0+6 \rightarrow t_0+18$)

Includes: DC and rf on-wafer short-term reliability accelerated testing and related diagnostics, long-term pure thermal storage tests and related diagnostics; definition of failure criteria; set-up of failure analysis techniques

Focus: define and practice a methodology for studying device robustness based on short-term, on-wafer testing, by using specific testing conditions with aim of accelerating selectively (as much as possible) specific failure mechanisms: thermally activated metal-semiconductor interaction effects; hot-electron-induced effects; time-dependent breakdown effects.

Results: identification of failure “signatures” (specific electrical failure modes) for the technology under test; analysis of failure mechanisms induced in short-term under highly-accelerated conditions; fast benchmarking of different alternative options; identification of absolute maximum ratings. Definition and practice of short-term reliability evaluation.

Long-term results: understanding of thermal stability of Schottky and ohmic contacts, thermal and of electrochemical stability of device surface.

Phase 3 (t₀+18→t₀+24)

Includes: extension of DC and rf testing for a deeper understanding of identified failure mechanisms. Set-up, on the basis of the results obtained during previous phases, of specific (>1000 h) long-term accelerated testing, selection of devices to be submitted to long-term tests, selection and procurement of packaging, device packaging, die attach qualification and thermal characterization of packaged devices

Focus: devise suitable, less accelerated long-term tests capable of providing more realistic information on degradation mechanisms, towards the definition of degradation laws

Results: definition of the reliability testplan

Long-term results: methodology for long-term reliability evaluation

Phase 4 (t₀+24→t₀+36)

Includes: Long-term accelerated testing and failure analysis. Simulation of failure mechanisms by means of 2D device simulation

Focus: in-depth understanding of failure mechanisms: thermally activated metal-semiconductor interaction effects; hot-electron-induced effects; time-dependent breakdown effects.

Results: identification of failure mechanisms, acceleration laws, MTTF extrapolation, device models including simulation of degradation mechanisms

Long-term results: methodology for long-term reliability evaluation and failure analysis.

4.1 Research plan and recommended collaborative models between University and the industrial laboratory

The proposed model involves the collaborative development of a complete reliability evaluation plan of GaN HEMTs for rf application, as a way to transfer the proposed methodology for on-wafer and long-term reliability of GaN HEMT from University research lab to the industrial laboratory and/or related partners. To this aim, the University research laboratory will carry out a comprehensive study of GaN HEMT failure mechanisms on the devices submitted by the industrial laboratory and/or related partners. The plan will be jointly developed by the University research lab and the industrial laboratory and/or related partners, through this model:

- a PhD or post-doc will be hired by the University research lab to follow the project
- project evolution will be monitored by regular bi-weekly teleconferencing
- the industrial laboratory or the industrial laboratory's partner research representative will periodically visit the University research lab to directly participate to the project development for a period of up to 1 month/year for the entire duration of the project
- University research lab representatives will visit Japan twice a year to present results of the project and suggest methodology implementation.
- a progress report will be issued every six months
- a final report will be issued at the end of the project.

Phase I and Phase II include the implementation of short-term on-wafer tests including 24 hours DC and rf load-pull testing, and long-term (>1000h) thermal storage tests. This already enable the study of failure modes and mechanisms, including gate edge degradation effects, metal-gate interdiffusion phenomena, ohmic contacts degradation, hot electron effects. The study also involves and in-depth analysis of deep level effects.

The proposed methodology involves the use of DC and pulsed testing, electroluminescence microscopy and rf load pull testing, the development of failure analysis techniques and (possibly) the management of external services for more elaborated or expensive characterization and f.a. techniques. Phase III and IV require test engineering, packaging and suitable matched test structures or matching networks, implementation of long-term tests.

4.1.1 Phase 1 (from t0 to to+9 months) : Set-up of characterization methods, device selection and procurement, thermal characterization, untreated devices characterization

In this phase, DC, pulsed and rf characterization methods will be defined. As described above in Section 2.4, this procedure can be optimized if suitable test structures are available, enabling the independent analysis of the different device technology elements:

Typical elements include:

1. A gated TLM test structure
2. Large area Schottky and MIS structures
3. A leakage evaluation structure; the layout described in [131] enables separation of surface and vertical leakage components
4. Metal-Insulator-Metal Capacitor and interconnect test structure
5. A large periphery 4x10x100 μm transistor
6. A coplanar power transistor (8 x 125 μm)
7. A test structure for metal lines and air bridges
8. A test vehicle with passive elements, 2-finger transistor, a large area Schottky diode
9. A dynamic evaluation circuit including a pre-matched microstrip power transistor
10. Possibly HEMTs with different LG, LGS, LGD and different orientation



Fig. 34 : Reliability test structure adopted by MIT (J. Joh and J.A. del Alamo, tutorial notes of ESREF 2009, <http://www-mtl.mit.edu/~alamo/pdf/2009/RC%20160%20slides.pdf>, [132])

The set of measured parameters will include, among others (values are just examples)

Electrical parameter	Description	Testing conditions
$I_{DSSAT-10}$	saturated drain current	$V_{DS} = 10V$ and $V_{GS} = 0V$
$I_{DSSAT-15}$	saturated drain current	$V_{DS} = 15V$ and $V_{GS} = 0V$
$g_{mMAX-10}$	transconductance peak	$V_{DS} = 10V$
$g_{mMAX-15}$	transconductance peak	$V_{DS} = 15V$
$ I_{G_leakOFF-10} $	absolute value of gate leakage current	$V_{DS} = 10V$ and $V_{GS} = -7V$
$I_{DSOFF-10}$	drain current measured in pinch-off condition	$V_{DS} = 10V$ and $V_{GS} = -7V$
$ I_{G_leakOFF-15} $	absolute value of gate leakage current	$V_{DS} = 15V$ and $V_{GS} = -7V$
$I_{DSOFF-15}$	drain current measured in pinch-off condition	$V_{DS} = 15V$ and $V_{GS} = -7V$
V_{TH-2}	threshold voltage measured in linear region	$V_{DS} = 2V$ and $I_{DS} = 1mA/mm$
V_{TH-10}	threshold voltage measured in saturation	$V_{DS} = 10V$ and $I_{DS} = 1mA/mm$
V_{TH-15}	threshold voltage measured in saturation	$V_{DS} = 15V$ and $I_{DS} = 1mA/mm$
$ I_{GS} $	gate-source diode current	$V_G = -7V$
$T I_{GD} $	gate-drain diode current (only for DCL and gated-TLM devices)	$V_G = -7V$
R_{on}	on-state resistance	$V_{GS} = 0V$ and $V_{DS} = 0.5V$

On selected samples, double pulse characterization of deep levels should be carried out, providing information on trap nature and location, as described in [133], [21].

The characterization can be completed with the measurement of S-parameters of representative devices, at various V_{DS} and various frequencies.

As described in [14], a simple, low-frequency, load-pull system can be extremely useful for (i) correlation with pulsed current collapse measurements; (ii) short-term (24h) on-wafer accelerated testing and (iii) evaluation of rf degradation after accelerated testing.

Characterization of hot electron effects, as well as failure analysis of gate leakage current degradation and other failure modes can be accomplished by an electroluminescence microscopy system, which can be implemented by suitable modification of a microprobe system, as described in [53].

Evaluation of active device channel temperature has to be performed at least for the various power dissipation levels that are planned for accelerated life testing.

Average channel temperature and thermal resistance values can be evaluated using pulsed electrical methods and infrared techniques, coupled with device modeling. Since GaN HEMTs may, in general, be affected by trapping effects, electrical measurements based on the properties of the gate Schottky junction usually show poor reliability and reproducibility. The method suggested by Joh and del Alamo [25], based on the combined measurements of on resistance and drain saturation current can be adopted for R_{th} evaluation. All these measurements have to be compared to finite element simulations of device thermal behavior (possibly provided through consultancy) and calibrated by means of microRaman thermography (which also provides values close to maximum device temperature) or other suitable techniques, see Section 2.3.

An University partner provides 2D device simulation emulating device characteristics and current collapse effects.

4.1.2 PHASE 2 on-wafer reliability accelerated testing, short-term biased tests, long-term pure thermal storage tests and related diagnostics (from t_0+6 to t_0+18)

The main goal of this activity is to obtain, by means of short-term tests, a well defined signature for each of the failure modes/mechanisms which affect the devices (e.g. shape of degraded I_D vs V_{DS} , $I_D - g_m$ vs V_{GS} , I_G vs V_{GD} curves. These signatures will be obtained through non-destructive analysis, and used in order to allow correlation of the results obtained on different technologies and/or using different test methodologies (e.g. DC vs. RF...).

In general, the guidelines for designing the short-term tests will be the following :

- for gate junction leakage degradation consequent to reverse bias or off-state stress: identify critical voltage by means of step-stress tests (SST); carry out constant reverse voltage tests at RT and vs temperature; study the dependence of critical voltage and time to breakdown on V_{DS} , T; check possible correlation with formation of pits on the device surface or at the gate/semiconductor interface and study dependence on the test environment
- high forward gate current (HFGC): emulates forward biasing of the gate Schottky junction which takes place during rf testing at high compression levels
- hot carrier tests (HCT): using electroluminescence intensity as a guideline to evaluate hot-electron acceleration factor (see Appendix on failure mechanisms literature survey), HCT will be carried out at different bias points in order to distinguish hot electron effects from thermally activated mechanisms

- other specific tests include tests for accurate thermal characterization; pulsed tests in order to emulate dynamic and memory effects which may be encountered during rf operation
- 24 hours rf testing on a load pull bench, Fig. 35

Table 1 shows a preliminary list of short-term tests which could be carried out in the framework of this project.

	Type of test	Methodology	Goal	Conditions	Assembly
	SHORT-TERM TEST (up to 100h)				
1	Step-stress reverse bias test	Increase voltage up to catastrophic leakage increase monitor EL, IG, current collapse	Reverse bias gate degradation Critical voltage	VG from -5 to -200V, 2min step , VD=VS=0 as described in 2.3.2.1	On wafer; Devices must be optically visible ¹
2	Constant reverse voltage tests	Monitor EL, IG, current collapse	Reverse bias gate degradation acceleration law	VG<VG critical (up to 5 values), VS=VD=0 , stress time>1h, different VG chosen depending on technology	On wafer; Devices must be optically visible ¹
3	Constant reverse voltage vs T	Study time to breakdown dependence on T	Reverse bias gate degradation acceleration law	Same conditions of 2. Measurements made between RT and 200°C (max). At least 3 different temperatures	Chip carriers and DIL
4	Constant reverse voltage vs ambient	Study time to break down and degradation mode dependence on environment	Reverse bias gate degradation influence of ambient (RH, oxygen)	Same conditions of 2 changing relative humidity, or ambient	Chip carriers and DIL
5	High forward gate current	Step stress first, then constant current tests	MMIC high IG during RF testing at high compression levels	First IG stepping from 1uA/mm to 10mA/mm (step time to be decided > 2min) and then constant IG=1 mA/mm	On wafer
6	High forward gate current vs T	Constant current tests at various T	Same of 5 Vs T	Same stress of 5 with the addition of T from RT to 200°C (max). At least 3 different temperatures	Chip carriers and DIL
7	Hot electron tests vs electroluminescence vs VGS, at fixed VDS>40V (GH50) or VDS>20V (GH25)	Use EL as parameter to identify level of hot electron stress	Hot electron degradation vs VGS	VDS>40V, VG const at 6 different values, see 2.3.2.3	On wafer; devices must be optically visible ¹
8	Hot electron tests vs electroluminescence vs VDS, at fixed VGS	Use EL as parameter to identify level of hot electron stress	Hot electron degradation vs VDS	6 different VD ,VG constant chosen depending the device, see 2.3.2.3	On wafer; devices must be optically visible ¹
9	Hot electron tests along a isopower line	Separate hot electron effects from those accelerated by temperature	Hot electron degradation at constant T	4 or 5 bias points following a isopower curve, see 2.3.2.3.	On wafer; devices must be optically visible ¹
10	Hot electron tests vs T	Separate hot electron effects from those accelerated by temperature	Hot electron degradation temperature model	Some selected test described in 7. 8. and 9. repeated at different temperatures (max 4 different T) from RT to 150°C.	Some sample on-wafer and on Microwave package

Table 1: Preliminary list of short-term tests for the identification of failure mode signatures

In addition to short-term tests, thermal storage tests at three temperatures of wafer-level devices will be carried out, with the aim of studying purely thermally activated failure mechanisms and to extract their activation energy.

Diagnostics will be based on DC, pulsed and rf measurements, to be carried out periodically during the tests; failure analysis will adopt electroluminescence characterization Fig. 36, passivation and metallization removal and observation by SEM and AFM. FIB and TEM will be adopted for the identification of interdiffusion effects and localized damage on selected (and different) samples.

An external partner provides 2D device simulation emulating device characteristics and short-term device degradation modes and mechanisms.

4.1.3 PHASE 3: Set-up of long-term accelerated testing, selection of devices to be submitted to long-term tests, selection and procurement of packaging, device packaging, die attach qualification and thermal characterization of packaged devices (from t0+18 to t0+24)

Microwave packages have to be used for long-term DC and rf accelerated testing. Suitable packages, which could reach the operating frequencies selected for rf testing, have to be selected and procured. After mounting, die attach has to be controlled by X-ray micrography and thermal resistance has to be evaluated. 30 to 50 devices are typically needed for a 3 conditions DC test + 1 condition RF test.

An external partner provides 2D device electro-thermal simulation.

4.1.4 Phase 4: Long-term accelerated testing of packaged devices and failure analysis (t0+24 to t0+36)

Proposed DC and rf long-term tests include DC operating life tests in three conditions and one RF test (single condition). For DC life tests, the choice of conditions, preliminarily defined in the reliability assessment will take into consideration the combination of the main accelerating factors: hot electrons, electric field, junction temperature, as suggested by the results of short-term tests.

Table 2 summarizes long-term tests to be carried out.

Type of test	Methodology	Goal	Assembly
Thermal storage, three temperatures (carried out in Phase 1)	250°C, 300°C, 350°C	Purely thermally-activated failure mechanisms	on-wafer
DC life test	3 conditions (2 bias points, 2 temperatures)	effect of combined electric field, current, temperature	microwave package
RF life test	1 condition	Emulation of operating conditions, accelerated	microwave package

Table 2: Long-term tests to be carried out: thermal storage on PCM and microwave devices; DC and Rf life tests on microwave packaged devices

Each long-term reliability test will be stopped at the end of the defined test time (typically >2000h), or if failure criteria will be reached, as shown in Table 3.

Parameters DC tests	Failure criteria
I_{DSS}	Decrease $\geq 20\%$
g_{m_MAX}	Decrease $\geq 20\%$
Parameters rf tests	
P_{OUT}	Decrease ≥ 1 dB
Linear gain	Decrease ≥ 1 dB

Table 3: Failure criteria

Each of the events shown in the Table can be used as failure criteria, keeping the threshold voltage and the diode characteristics under control at each measurement step.

Diagnostics will be based on DC, pulsed and rf measurements, to be carried out periodically during the tests; failure analysis will adopt electroluminescence characterization, passivation and metallization removal and observation by SEM and AFM. FIB and TEM will be adopted for the identification of interdiffusion effects and localized damage on selected (and different) samples.

A University partner provides 2D device simulation emulating device characteristics and long-term device degradation modes and mechanisms.

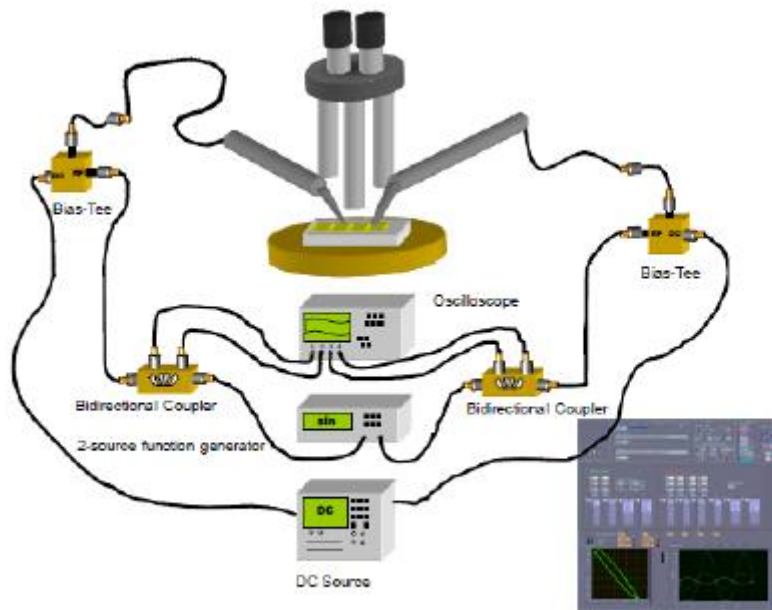


Fig. 35 : Sketch of a simple load-pull testing system

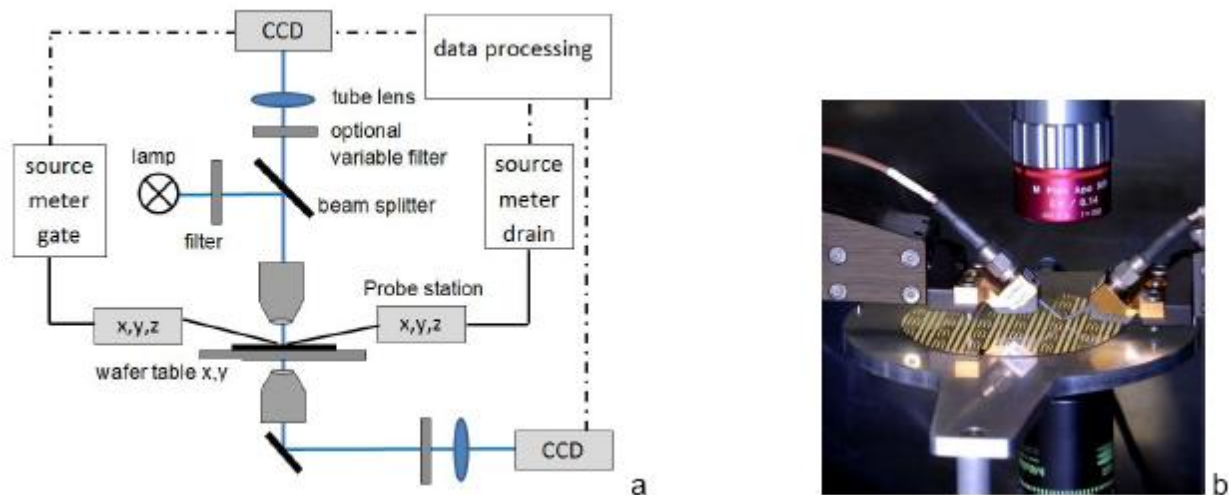


Fig. 36 : Implementation of an electroluminescence emission microscopy system using a microprobe station and two CCD cameras

4.2 Skills and resources required, including manpower, computing, lab facilities, number and type of devices needed and time frame

Phase 1 and 2 of the proposed research plan implies the development/use of the following experimental set-up :

- 1- A probe station for DC and rf measurements, equipped with semiconductor parameter analyzer, rf network analyzer, double pulse system, thermal chuck
- 2- A probe station connected to a load-pull system
- 3- An electroluminescence microscopy system, mounted on probe station 1
- 4- A small personal computer network equipped with instruments control software e.g. NI Labview and related software
- 5- Three environmental chambers for unbiased tests RT to 375°C, in air or controlled atmosphere
- 6- Device simulation environment (at least capability of finite element thermal simulation using ANSYS or similar tools)
- 7- Sample preparation capability, like a small chemical laboratory

External or University partner services: microRaman thermography, AFM, SEM and TEM microscopy, 2D device simulation

Phase 3 and 4 requires the implementation of automated testing equipment for long-term accelerated testing, like Accel-RF, plus packaging capabilities. For example, the University of Padova is equipped to carry out long-term DC and rf testing on small groups (~10) of devices at a time.

External or University partner services required: microRaman thermography, AFM, SEM and TEM microscopy, 2D device simulation

Skills and manpower:

1 reliability engineer (PhD) with knowledge on device physics, testing methods, GaN device processing and technology, failure modes and mechanisms of GaN devices, capable of interacting with external University groups providing expertise on reliability

physics, device modeling, failure analysis; capability of designing and implementing testing systems, thermal measurement systems, microscopy systems

1-2 electronics engineers with knowledge on device physics, microwave devices, device electrical characterization, DC and rf measurements, automation of measurement systems and related software

1 project supervisor EE or Physics PhD senior researcher with expertise on GaN devices, technology and reliability

5. PRELIMINARY CONSIDERATIONS CONCERNING CHARACTERIZATION AND RELIABILITY OF GaN VERTICAL DEVICES

Vertical GaN devices are extremely promising for applications requiring the handling of high voltage (>1.2 kV) and power (>10 kW) levels. vertical GaN-on-GaN diodes with blocking voltages higher than 4 kV have already been demonstrated [134], and both diodes and transistors have been fabricated (see for instance [135]–[140]). Another advantage of the vertical GaN devices is the significant reduction of chip area compared to the lateral topology [141]. Three main structures have been proposed for GaN-on-GaN vertical transistors: the first solution is the current aperture vertical transistor (CAVET, [142]), in which the source region is separated from the drain region by an insulating layer with a narrow conducting aperture. The Schottky gate is located above the aperture and allows the modulation of the current which passes through it [143]. Promising depletion and enhancement mode performance have been demonstrated, by using an Mg-ion-implanted GaN layer as current blocking layer [144]. The second approach is based on the vertical GaN-based trench gate MOSFET, grown on a GaN substrate [145]. A blocking capability of 1.6 kV has been demonstrated based on this approach [146]

Reliability study of this devices is still at an early stage. Not all technologies have reached maturity. For instance capability of repetitive, non-destructive avalanche breakdown of GaN-on-GaN pn junctions has been obtained only recently. In general the following failure mechanisms have been reported for vertical p-n diodes:

- Increase of leakage in reverse bias
- Knee voltage instabilities following forward biasing
- Time dependent breakdown in reverse bias conditions

In general, these effects depend on material defectivity, but also on surface conditions (flatness in particular), edge termination, passivation etc. In [135], the results of high temperature reverse bias (HTRB), high temperature operating life (HTOL), temperature humidity bias (THB), temperature cycling (TC), and inductive avalanche ruggedness tests conducted on vertical GaN devices packaged in standard power packages were reported.

Conclusions are that fundamental failure mechanisms are almost always traced back to the starting substrate material quality, substrate miscut angle, and surface morphology post epi growth. No observation of R_{ds} drift was made for vertical diodes fabricated on bulk GaN substrates under the stress conditions mentioned above was found if a suitable back metal and die attach process was adopted. An electroluminescence and TEM study on the effects of dislocations on leakage of GaN-on-GaN vertical p-n diodes has been recently presented

by Amano's group at ICNS, Strasbourg (unpublished). Leakage was correlated with a specific dislocation size and with GaN growth conditions.

CAVETs can be affected by current collapse effects and incomplete turn-off characteristics; at the moment no experiments have been shown on the long-term stability of those devices.

Vertical MISHEMT structures can be affected by threshold voltage bias-temperature instabilities and time dependent breakdown effects, as occurs in horizontal MISHEMTs. In a recent study [103], the results of a reliability study on the recoverable degradation of GaN-on-GaN fin-vertical transistors under positive bias stress have been reported; when subjected to moderate gate stress ($0 \text{ V} < V_{GS} < 3 \text{ V}$), these devices show a negative threshold voltage shift, which is correlated with a decrease in on-resistance. This process is ascribed to the detrapping of electrons from the Al_2O_3 insulator, induced by a low positive bias; conversely, for high stress bias ($V_{GS} \geq 5 \text{ V}$), a strong positive shift in threshold voltage is observed. This effect, which shows a slow recovery, is ascribed to the injection of electrons from the accumulation region (channel) toward the dielectric. Temperature-dependent measurements and 2-D simulations were carried out to support the hypothesis on degradation, and to evaluate the contribution of surface and bulk current in the n-GaN drift layer.

6. CONCLUSIONS

This white paper has analyzed reliability of AlGaIn/GaN HEMTs. Failure mechanisms of GaN HEMTs have been reviewed and a short reliability research plan has been presented, together with essential test equipments and capabilities. Some research centers active in this field in USA have been presented in a partial list. Expertise and equipments available at the University of Padova are also presented. Finally, some comments on the reliability of vertical GaN devices are briefly reported.

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