

# SOMMARIO

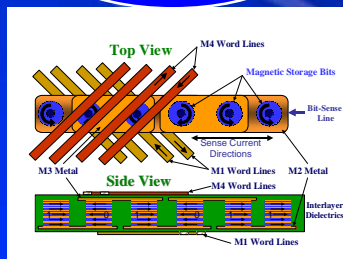
- **Introduzione alle memorie a semiconduttore**
- **Il transistor a floating gate**
- **Meccanismi di scrittura**
- **La Flash NOR**
- **Affidabilità**
- **La Flash multilivello**
- ▶ **Le memorie emergenti a stato solido**

# The Dream

- The search for the Universal Memory, combining
  - Fast read
  - Fast write
  - Non volatility
  - Unlimited endurance
  
- at a cost competitive with Flash and DRAM

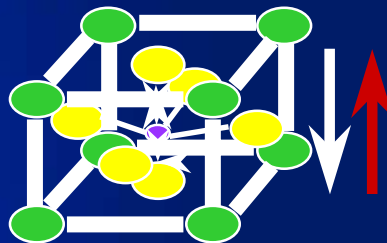
# More New Technologies Than Any Time In History

**MRAM**

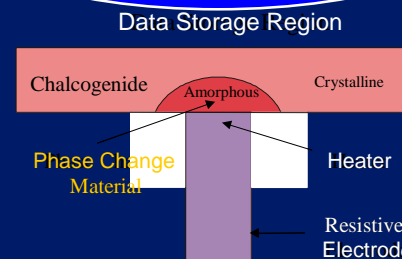


*Applied Electric Field Moves Center Atom*

**FERAM**



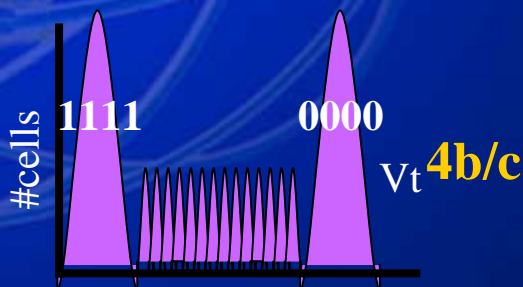
**OUM**



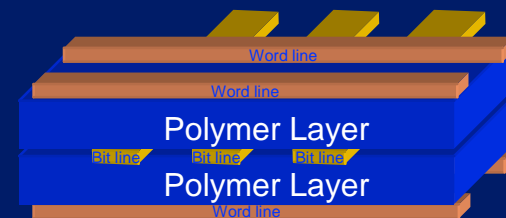
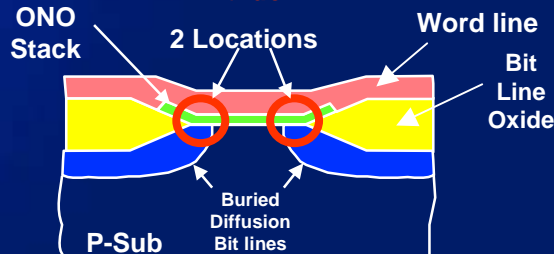
**ETOX®-4bpc**

**NROM**

**Polymer**



Charge Storage Sites in Nitride:



\* Other brands and names are the property of their respective owners

**One or two will become mainstream**

# Ferroelectric RAM (FRAM): the Concept

## ■ Storing mechanism:

- permanent polarization of a ferroelectric material

## ■ Writing mechanism:

- electric field produced in the ferroelectric layer by the voltage applied to capacitor plates

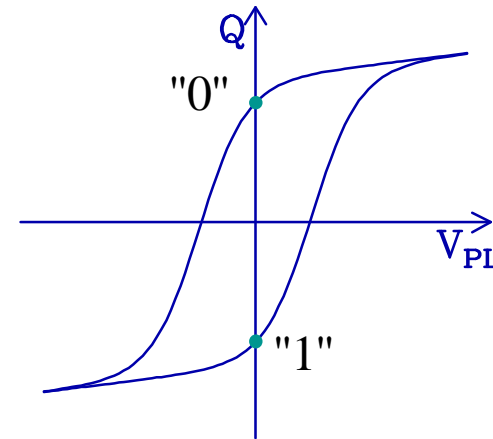
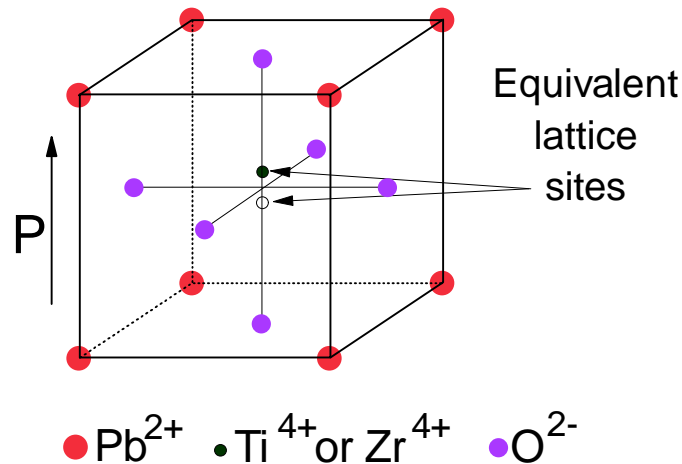
## ■ Sensing mechanism:

- displacement current associated to the polarization switch

## ■ Cell structure:

- 1 transistor, 1 capacitor (1T/1C), like DRAM

# FRAM Storing and Writing Mechanism



## ■ Two types of materials used:

- **lead zirconate titanate PZT ( $Pb_x Zr_{1-x} Ti O_3$ )** known since long time,
  - High remanent polarization (that is, high  $Q_{sw}$ ) and low process temperature
- **strontium bismuth tantalate SBT ( $Sr Bi_2 Ta_2 O_9$ )** more recent material
  - Good endurance properties, better thickness/voltage scalability

■ A ferroelectric capacitor will show an electrical polarization hysteresis loop under application of an electric field

■ The capacitor can be polarized in two steady states that can be maintained even without power supply

# Magnetoresistive RAM (MRAM): the Concept

## ■ Storing mechanism:

- permanent magnetization of a ferromagnetic material in a Magnetic Tunnel Junction (MTJ)

## ■ Writing mechanism:

- magnetic field produced by the current flowing in memory array metal-lines

## ■ Sensing mechanism:

- Resistance change of the magnetic tunnel junction

## ■ Cell structure:

- 1 transistor, 1 resistor (1T/1R)

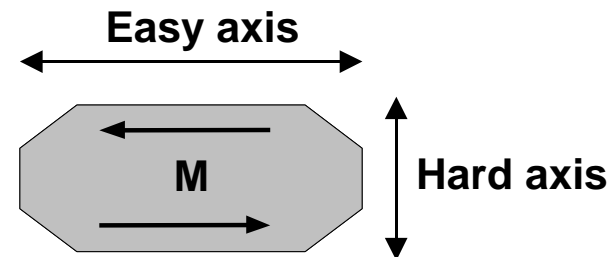
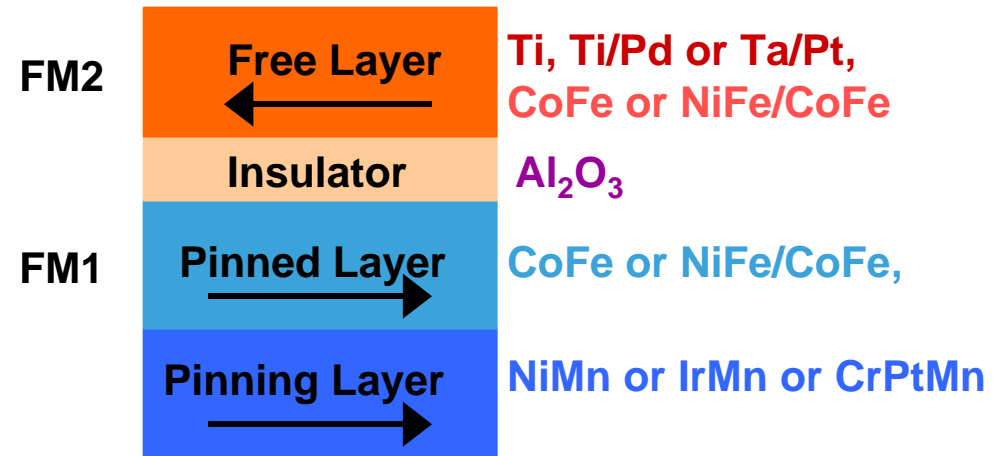
# MRAM Storing

## ■ Magnetic Tunnel Junction (MTJ):

a thin insulator between two FerroMagnetic (FM) layers, FM1 and FM2:

## ■ Spin Dependent Tunneling (SDT) effect depending on relative magnetization (M) orientation: FM1 pinned, FM2 switching

■ First FM electrode acts as spin filter, second FM layer acts as spin detector



# Phase Change Memory (PCM): the Concept

## ■ Storing mechanism:

- amorphous / poly-crystal phases of chalcogenides

## ■ Writing mechanism:

- self-heating due to current flow (Joule effect)

## ■ Sensing mechanism:

- resistance change of the chalcogenide

## ■ Cell structure:

- 1 transistor, 1 resistor (1T/1R)

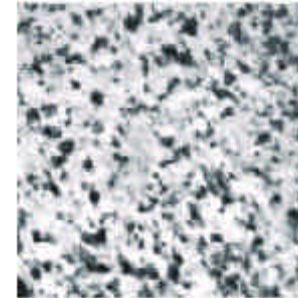
# PCM Storing Mechanism

## Amorphous



- ❑ Short-range atomic order
- ❑ Low refractive index
- ❑ High electrical resistivity

## Crystalline



- ❑ Long-range atomic order
- ❑ High refractive index
- ❑ Low electrical resistivity

Refractive Index



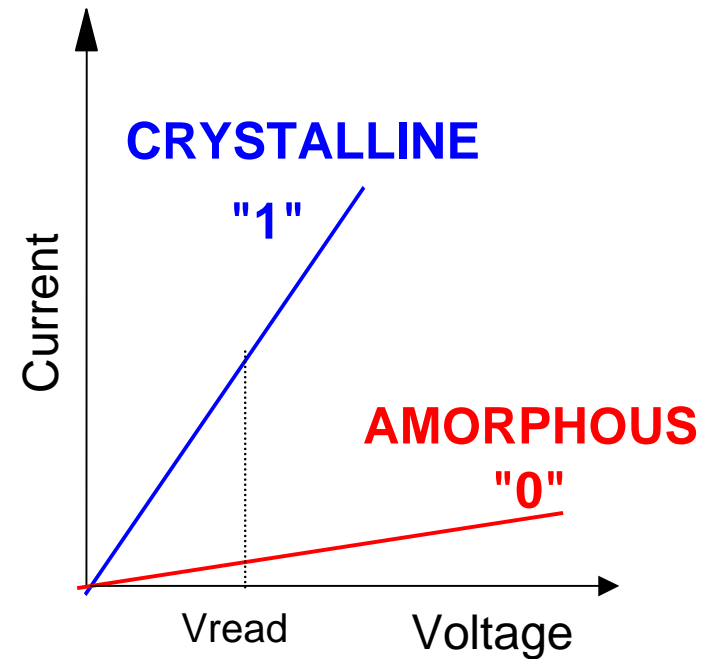
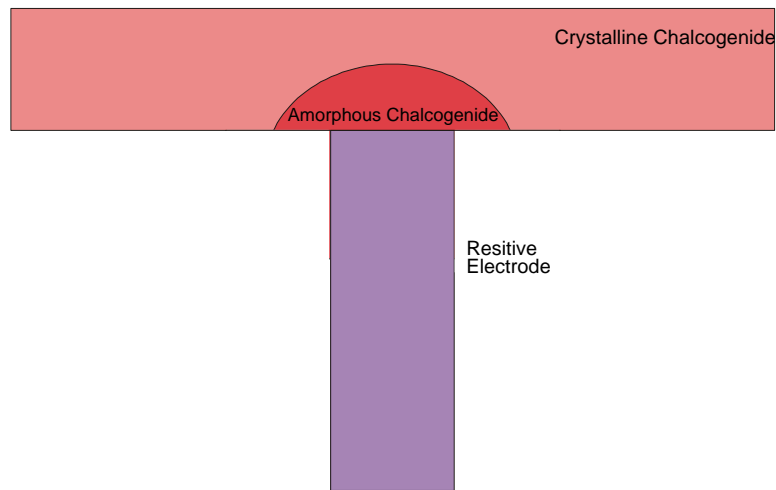
Re-writable CD and DVD

Electrical Resistivity



Non-Volatile Memories

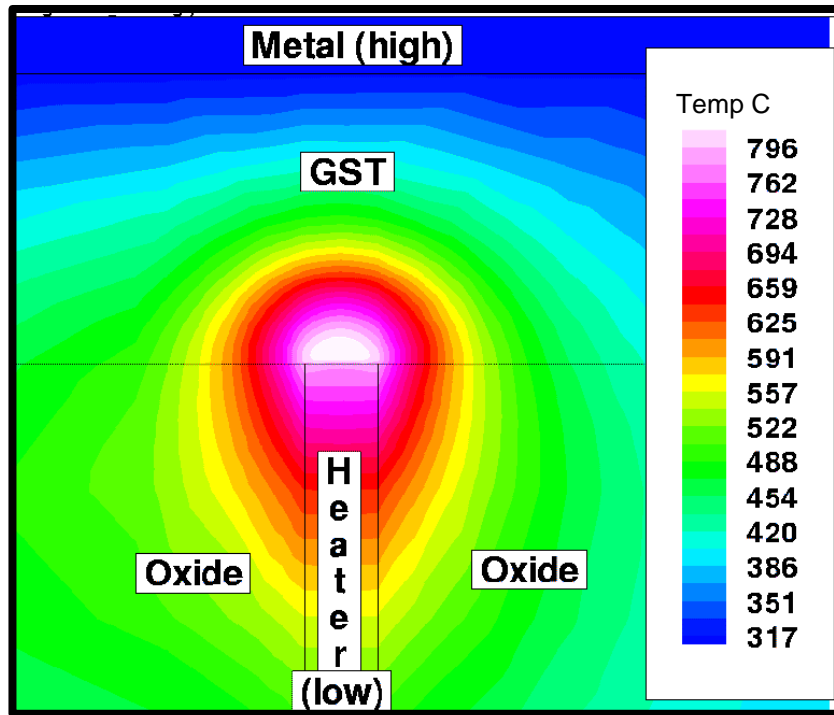
# PCM Sensing Mechanism



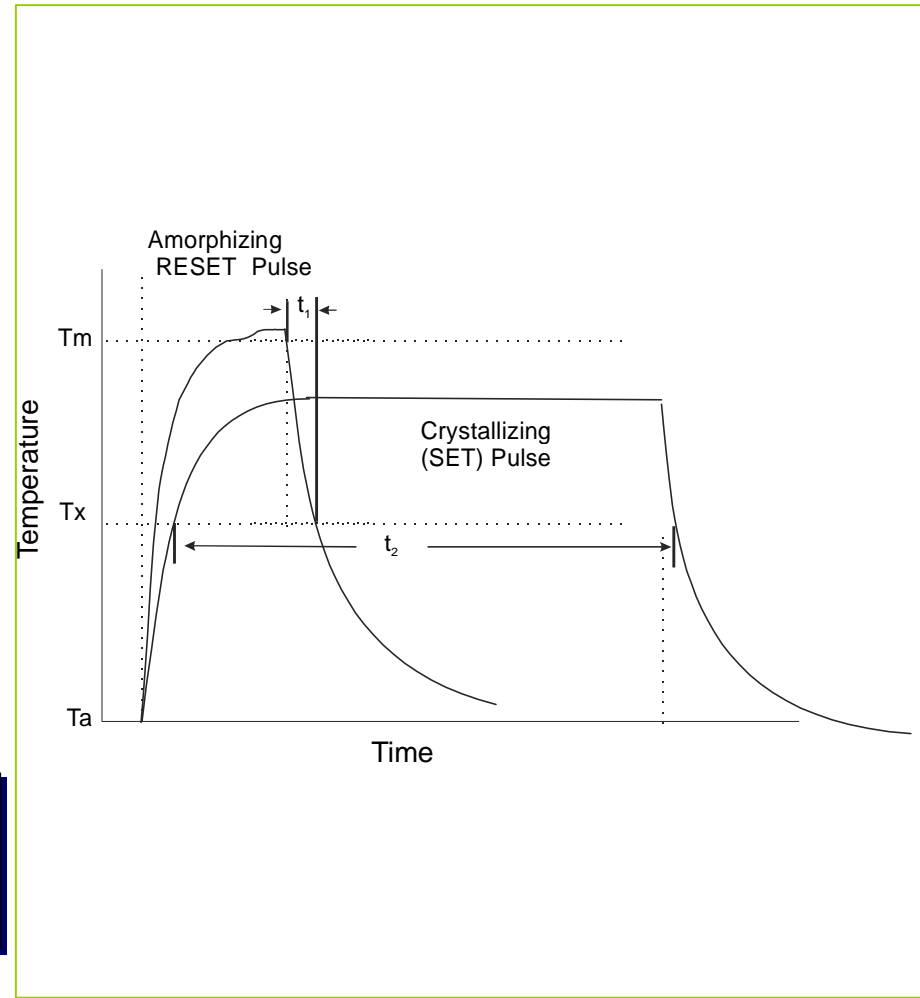
"1" => Crystalline phase => low Resistance

"0" => Amorphous phase => high Resistance

# PCM Writing Mechanism



Simplified structure of a phase change memory: simulation of temperature distribution during PCM programming



# Memory Technology Benchmark

	DRAM	Flash	FRAM (ferroelectric)	MRAM (magnetic)	PCM (phase change)
Relative bit size*	1	0.25 - 1	3 - 10	1 - 3	0.5 - 2
Relatv. mask count	1	1.1	1	1	1
Scalability	Fair	Fair	Poor	Poor	Good
Endurance	Unlimited	10 <sup>5</sup>	10 <sup>10</sup> (destructive read)	>10 <sup>14**</sup>	10 <sup>12</sup>
Data retention	10ms	> 10years	> 10years	> 10years	> 10years
Write time	< 100ns	μs/ms	< 100ns	< 100ns	< 100ns
Write power/B (VxI)	3Vx100μA	5V x 1mA	3Vx100μA	1.8Vx10mA	3Vx1mA
Maturity	Volume prod.	Volume prod.	Limited prod.	Test chips	Test chips

\* 1= DRAM cell size (~NOR flash)

\*\* MTJ oxide layer reliability still not proven.

— Central R&D

R.Bez – IMST 2002

Non Volatile Memory Process Development



# CONCLUSIONI

- ▣ Unendo i vantaggi delle EPROM e delle EEPROM, le memorie FLASH hanno assunto un ruolo dominante nel mercato delle memorie non-volatili e ne sostengono la crescita.
- ▣ Grazie alla semplice struttura della cella di memoria ed alla possibilità di memorizzare più bit per cella, le memorie FLASH si candidano a diventare le memorie a stato solido di minor costo e maggior densità.
- ▣ Le tecnologie che consentono di incorporare memorie FLASH con la logica CMOS svolgeranno un ruolo strategico nell'integrazione di sistema su singolo chip.
- ▣ Le memorie FLASH saranno ancora lo standard di mercato per almeno un decennio. Nel frattempo, alcune nuove tecnologie sono in sviluppo.