ELECTRICAL CHARACTERIZATION IN VLSI TECHNOLOGIES

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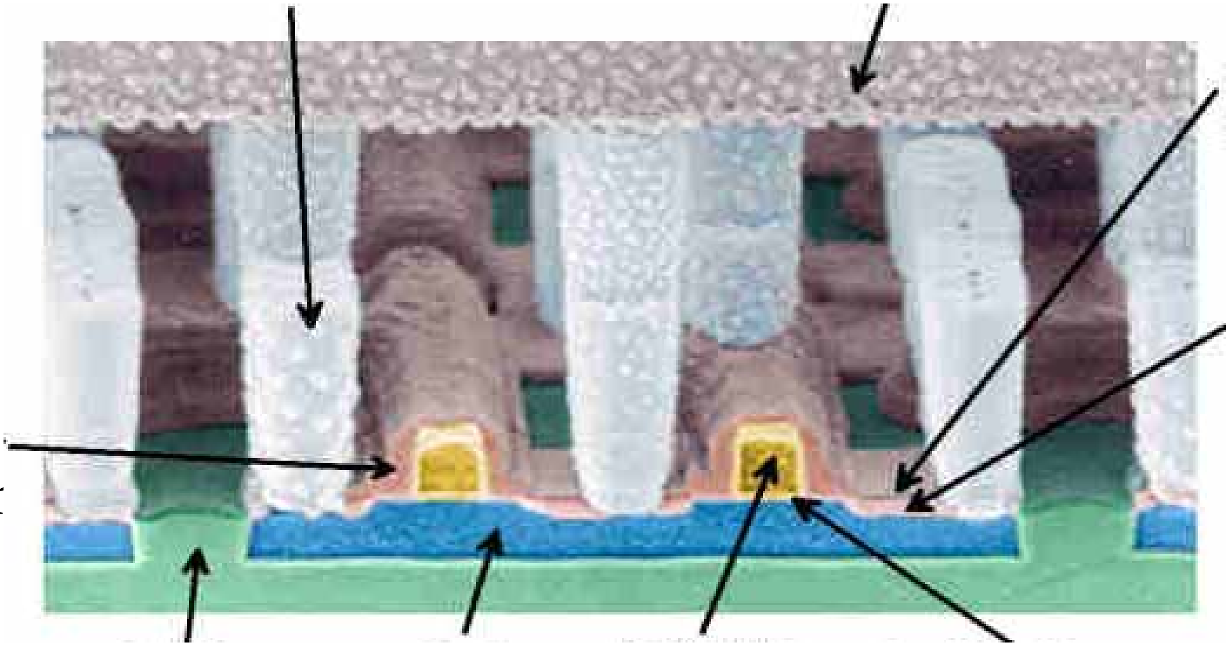
OUTLINE

- Introduction
  - VLSI technologies
  - Layout background
- Electrical characterization
  - Products
  - <u>Components</u>
- Test structures
- Measurements
- Analogue characterization: Mismatch
- Analogue, specific issues
- Compact modeling

CONTRIBUTIONS

- **International Electron Device meeting**
- **Symposium on VLSI Technology and Circuits**
- **International Conference on Microelectronic Test Structures**
- **European Solid-State Device Research Conference**
- **Advanced IC Design Course (Europractice-EFPL)**
- **Dr. G. Croce, G. Ricotti (STM-TPA)**
- **Dr. D. Cantarelli, G. Fontana, R. Annunziata, C. Riva, A. Marmiroli, C. Giambelli, P.Fantini, L. Bortesi, K. Giarda, Dr. A. Maurelli**
- **Prof. A. Lacaita (Politecnico di Milano)**

SUBMICRON DEVICES



W Plug

Al interconnects

Silicided Source/Drain

Source/Drain junctions

Oxide spacer

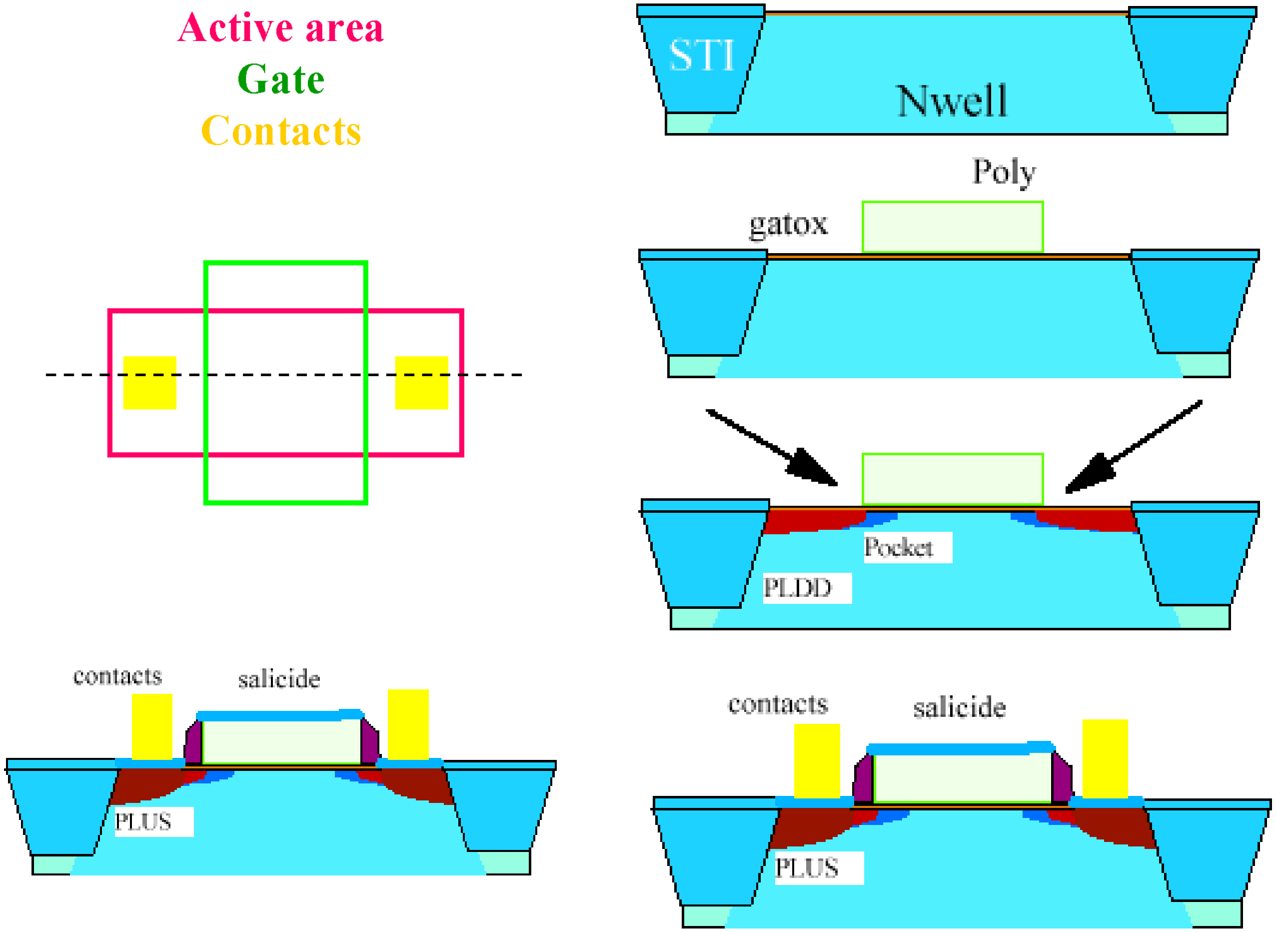
Silicon oxide

Silicon

Polysilicon gate

Gate oxide

SUBMICRON MOSFETs



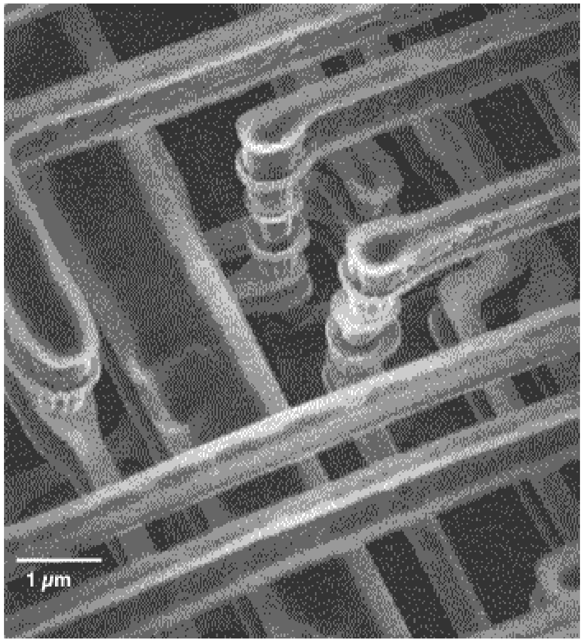
-Isolation
-Well

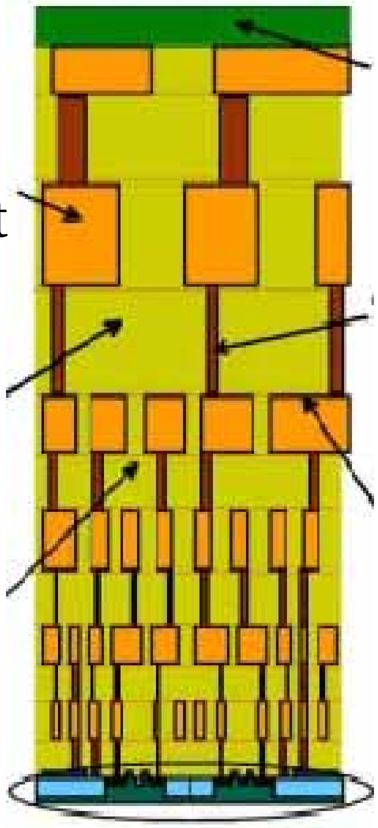
-Gate oxide
-Gate definition

-Light Doped Drain

-Spacer
-Drain (plus)
-Salicide
-Contacts

SUBMICRON TECHNOLOGIES





BACK END

Cu interconnect

Low K dielectric

Si_3N_4 Etch stop

FRONT END

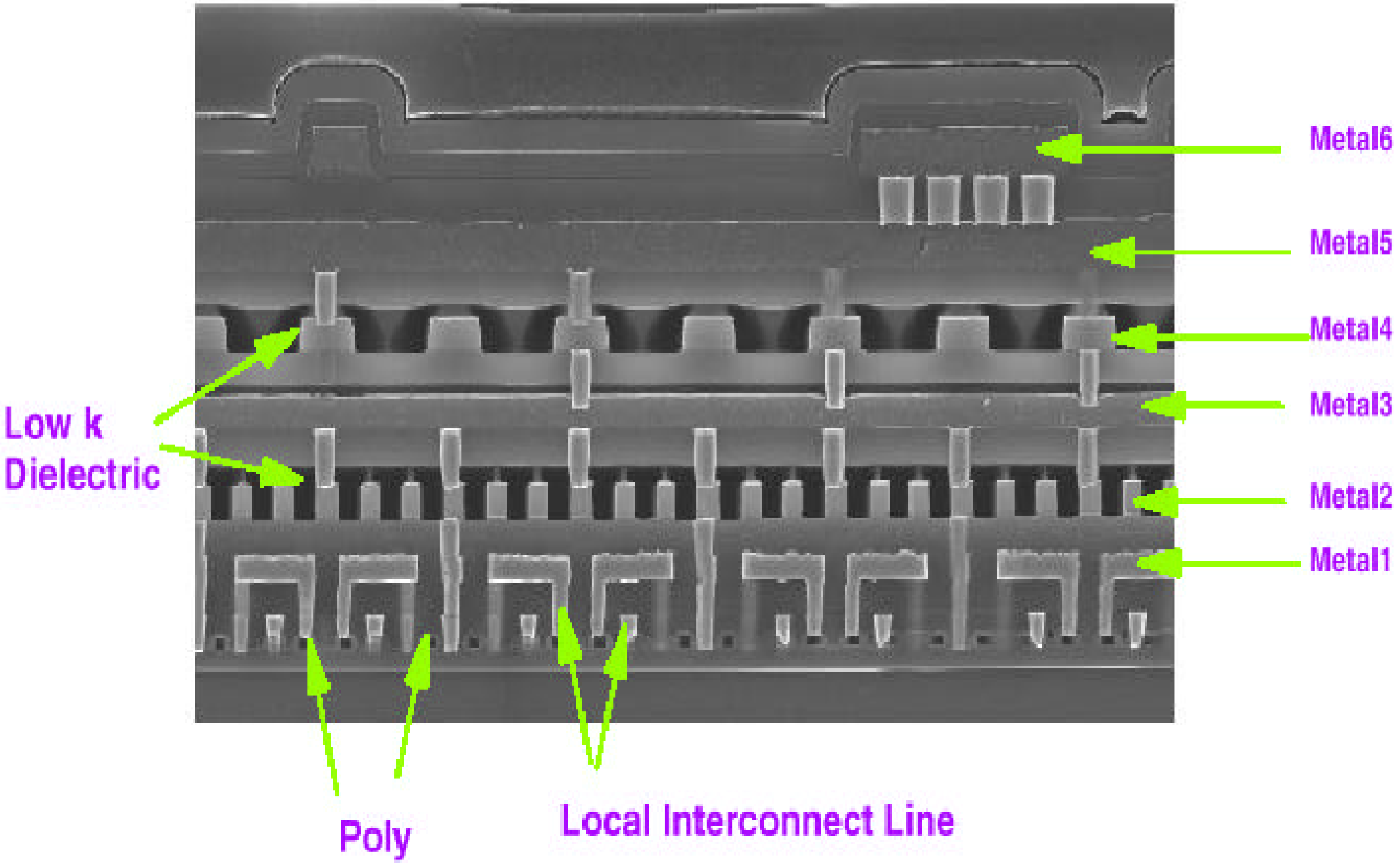
Cap Layer

Cu Vias

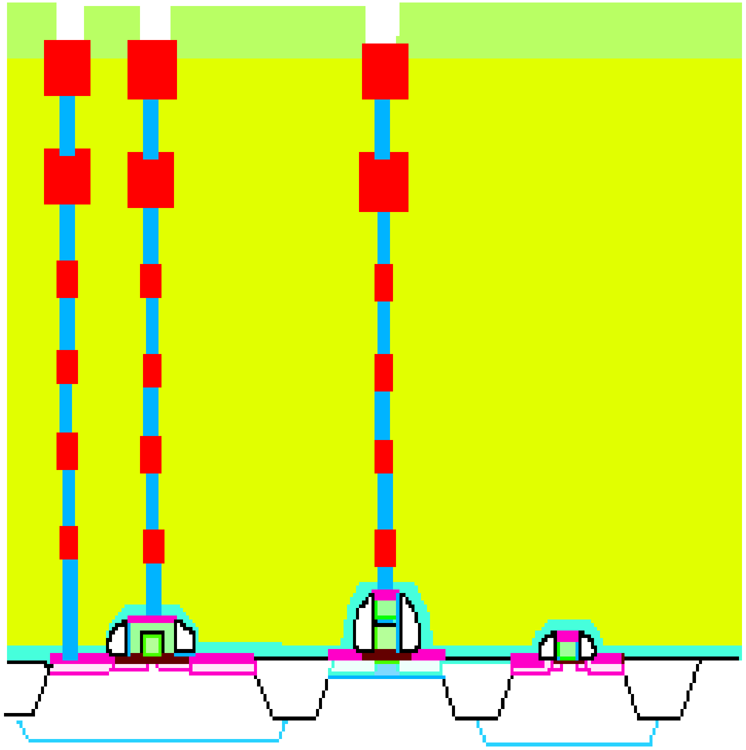
Diffusion barrier

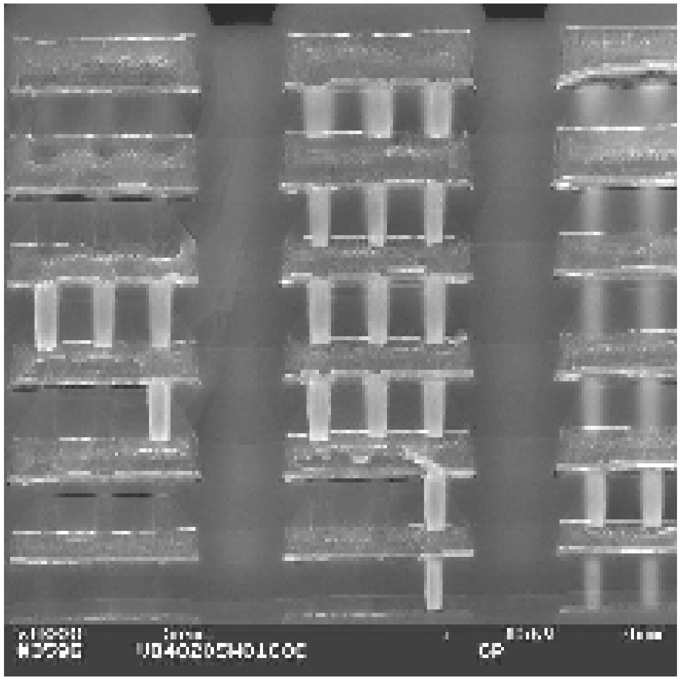
Active device

6 metal layer 0.18μm Technology SEM cross section

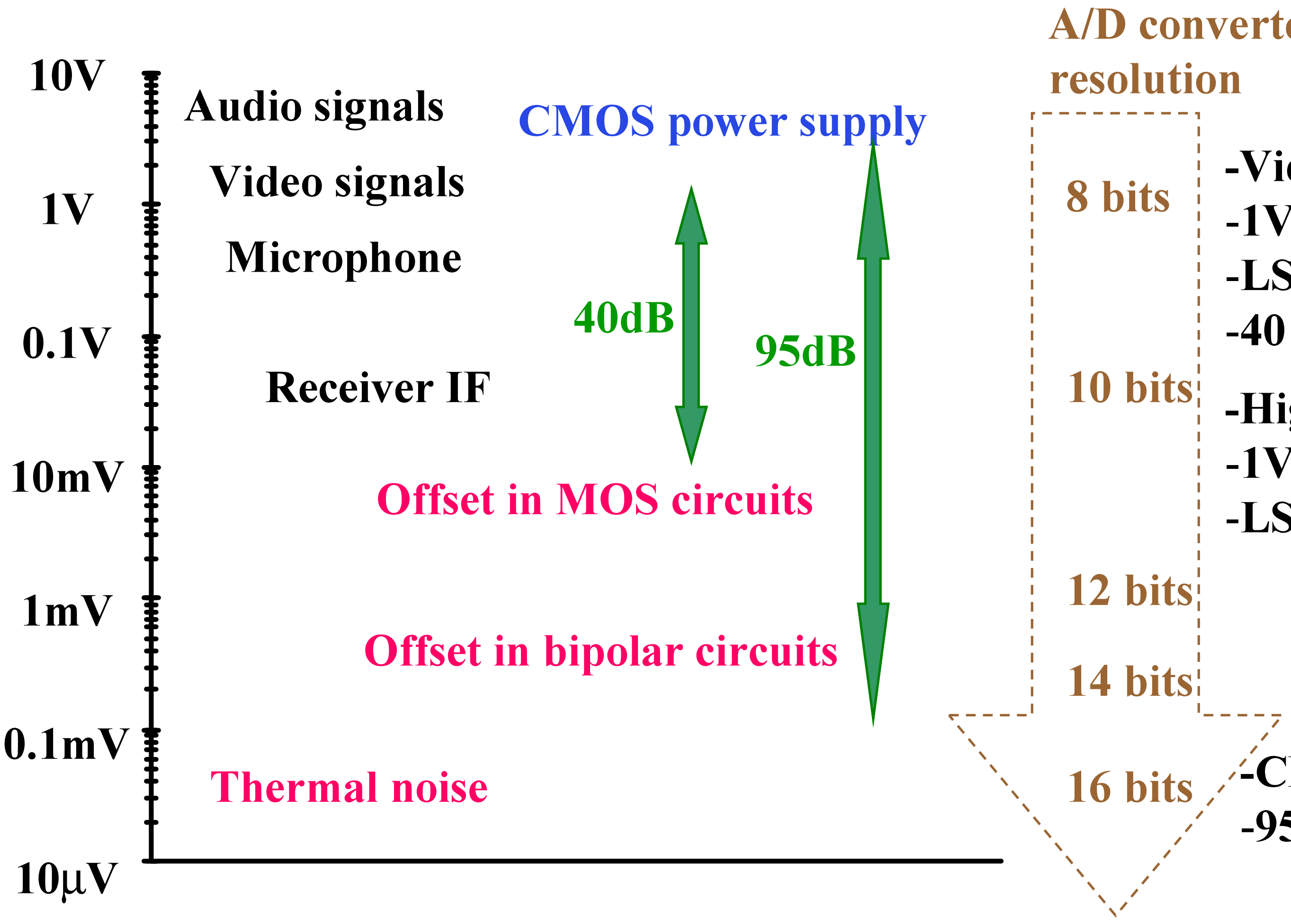


6 metal layer 0.18μm Technology





Small signals:
orders of magnitude, bits and %'s



Audio signals

Video signals

Microphone

Receiver IF

CMOS power supply

Offset in MOS circuits

Offset in bipolar circuits

Thermal noise

A/D converter resolution

8 bits

- -Video signals processing
- -1V signal in 256 levels
- -LSB < 4 mV
- -40 db => 1% accuracy

10 bits

- -High resolution video
- -1V signal in 1204 levels
- -LSB < 1 mV

12 bits

14 bits

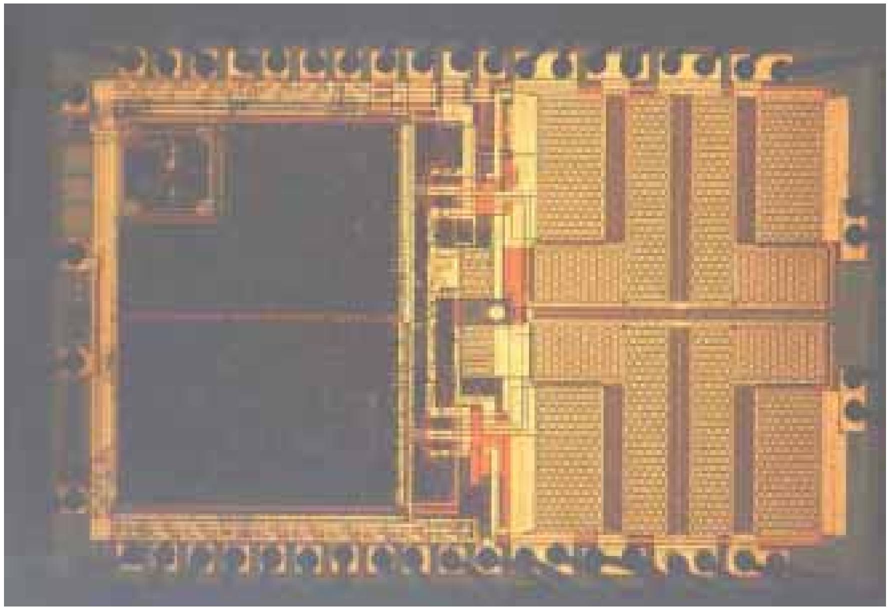
16 bits

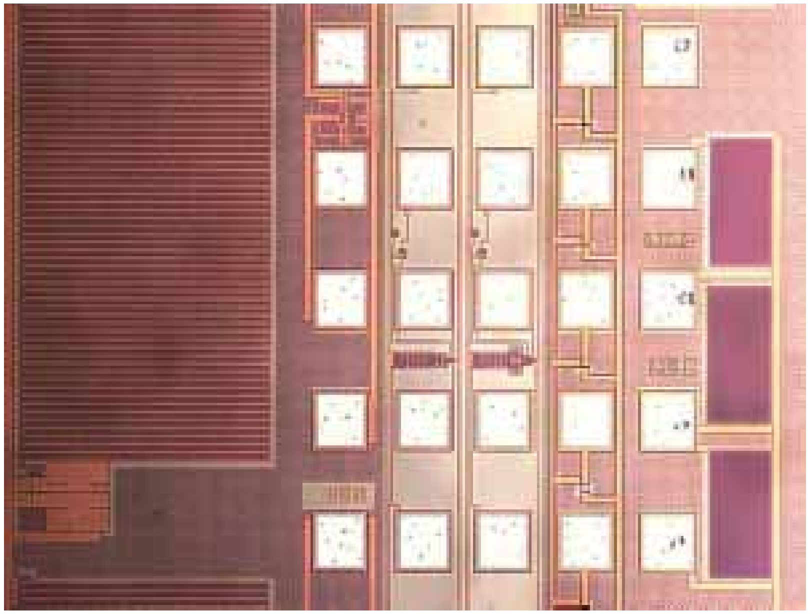
- -CD audio
- -95 dB => 0.0018% accuracy

ELECTRICAL CHARACTERIZATION

PRODUCTS (CIRCUITS IN VLSI TECHNOLOGIES)

ELEMENTARY DEVICES / STRUCTURES





PRODUCTS
electrical characterization

-**EWS** (Electrical Wafer Sort):

- 1 or 2 step characterization on wafer

-**FINAL TEST**:

- After packaging
- Possible ‘burn-in’ tests (e.g. 24h biased) to screen early failures
- Possible ‘speed’ tests

EWS and FINAL TEST:

- Product dependent:
  - Digital / Analog / mixed circuits
  - => different testers / complexity

DEVICES / STRUCTURES
electrical characterization

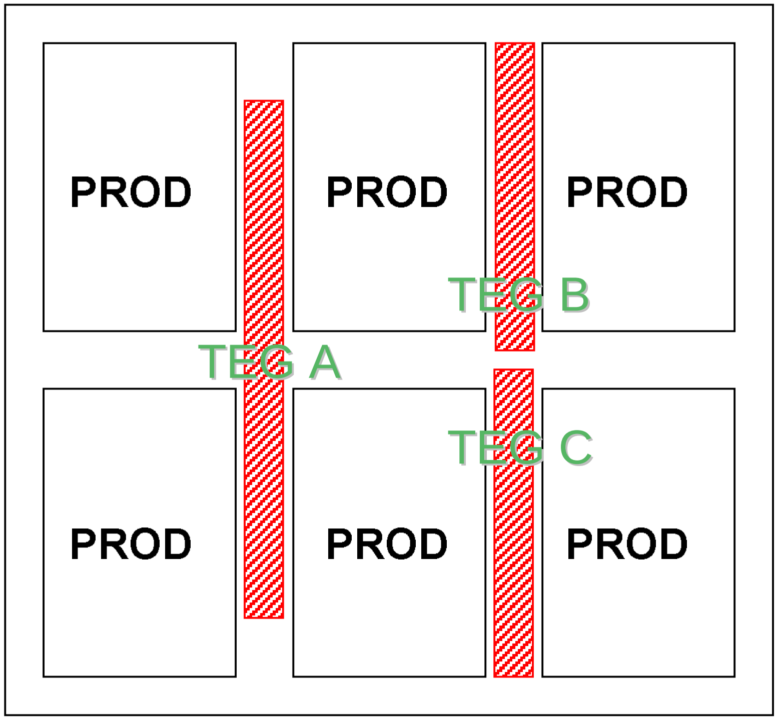
All these elementary components are arranged in a "TEST PATTERN" i.e. a set of different test structures (a collection of single structures, active and passive, and small test circuits) for:

- <u>process development</u> (large set)
  designed for process characterization, layout rules definition, and device modeling
- <u>defectivity</u>: yield optimization/forecast
- <u>process control</u> (minimum set)
  to track and keep aligned device electrical properties from lot to lot

Process Control TEG (1)

✓ Only a few TEGs in available scribing (saw) lanes

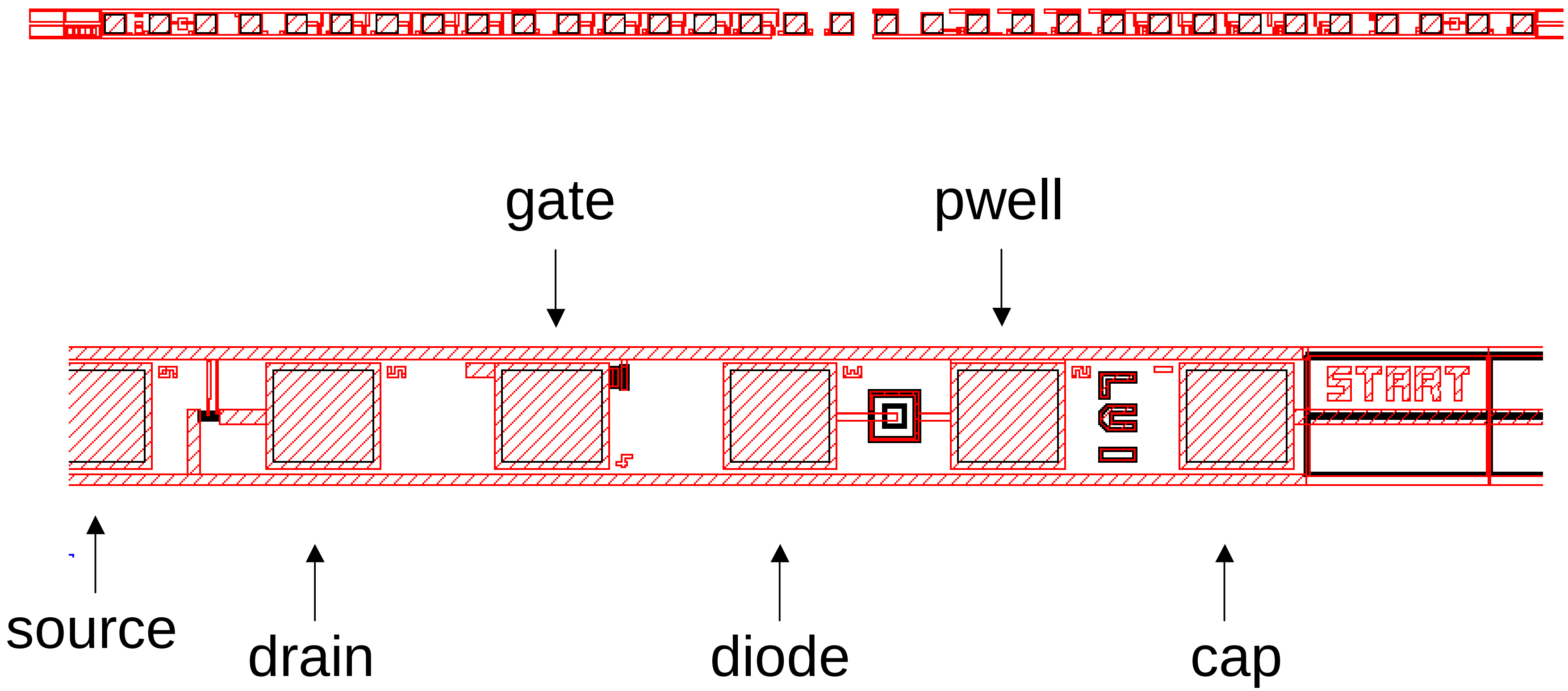
TEG = Testing Evaluation Group



✓ Possible wafer mapping

✓ Used for parametric testing:
  - -e.g. 9 sites/wafer
  - -testing speed requirements
  - -selected measurements

Process Control TEG (2): layout



gate

pwell

source

drain

diode

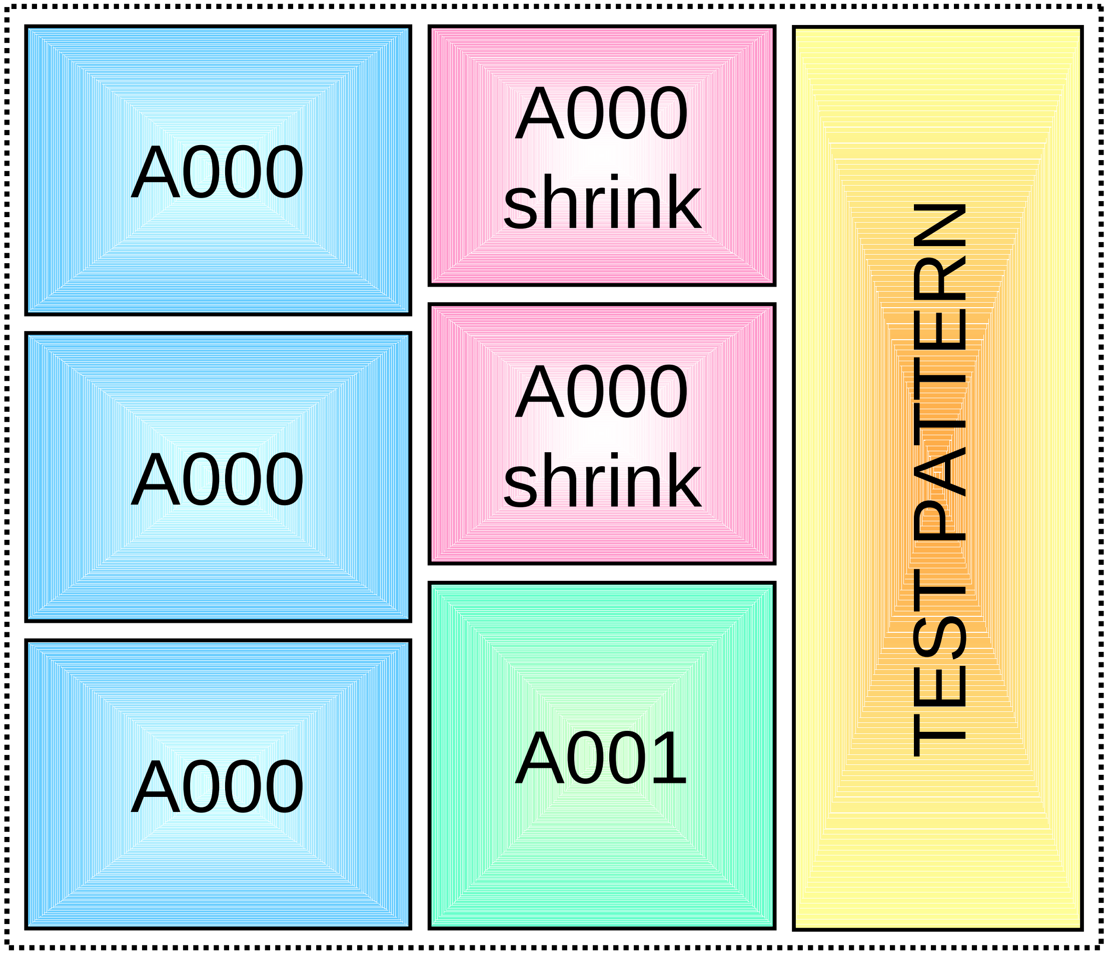
cap

Must: minimize number of pads, and series resistance

Process Control TEG (3)

- Only a few TEGs in available room (depending on scribing lanes number in exposure field)
- Only small structures, but some large ones (usually capacitors) on top or bottom of the pads
- Width: max 100 µm
- Length: e.g. 5120 µm (32 pads) plus external structures
- Pad dimensions: e.g. 80x80 µm
- All what need to monitor a “production” process:
  - ✓ Transistors, resistors, via chains, parasites, cells, diodes, capacitors, bipolars, “special” structures (e.g. for damage evaluation)

Process Development Test Pattern (1)



Large available room: part of exposure field, corresponding to one or more product prototypes

A large number of TEGs is drawn

Process Development Test Pattern (2)

- Almost complete set of structures
  - Transistor: all types, stepped in length and width
  - Diodes: small and large, area and perimeter
  - Oxide Capacitor: small and large, area and perimeter
  - Parasites: all types, stepped design rules

    to check isolations, leakage, breakdown, unwanted MOS, …
  - Design rules: lithographic limits, robustness

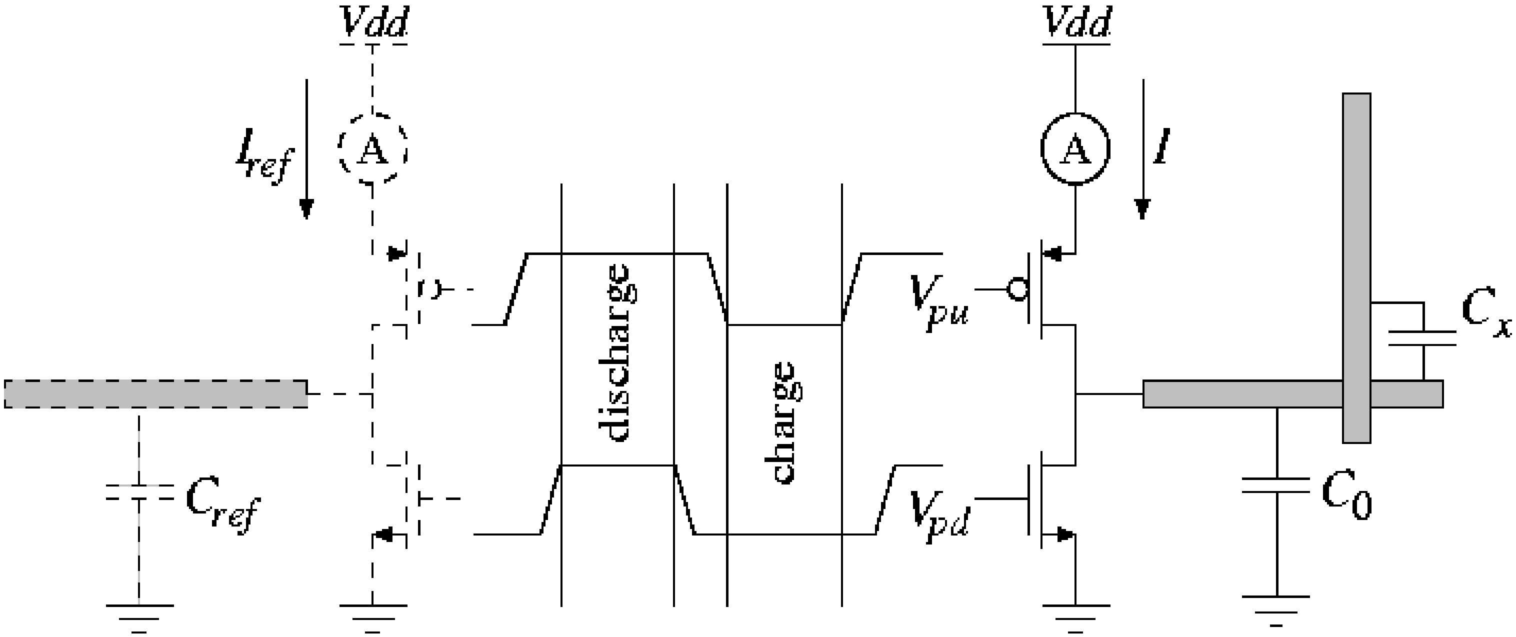
    e.g. contact-gate distance, ...
  - Resistors: stepped widths
  - Van der Pauw, Kelvin, Cross-Bridge resistors
  - Specific devices if released by the technology:

    e.g. DMOS, Non Volatile Memory cells, …

Process Development Test Pattern (3)

- Model Extraction Structures:
  - Parasitic Interconnection Capacitors / transducers
  - Matched pairs (analogue characterization)
- Other structures:
  - Ring Oscillators (dynamic characterization, model validation,…)
  - Electro Static Discharge protections, I/O buffers
  - Test chip (critical circuit blocks, demonstrators,…)
- Wafer Level Reliability Development:
  - e.g. structure for electromigration studies

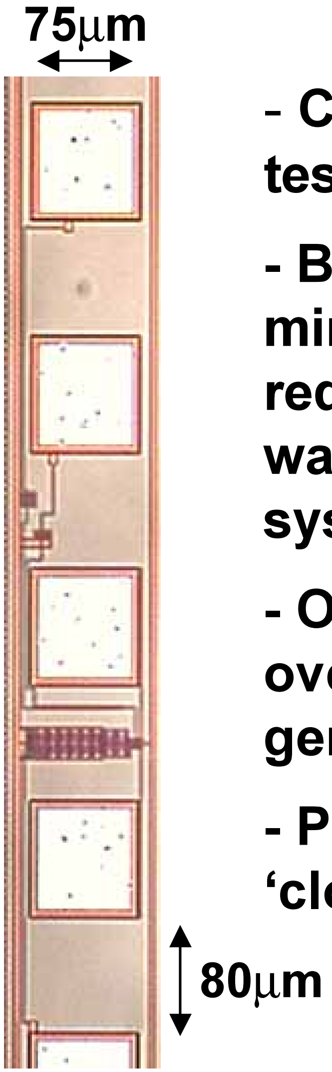
On-chip Interconnect capacitance measurements (1): Charge Based Capacitive Measurements method



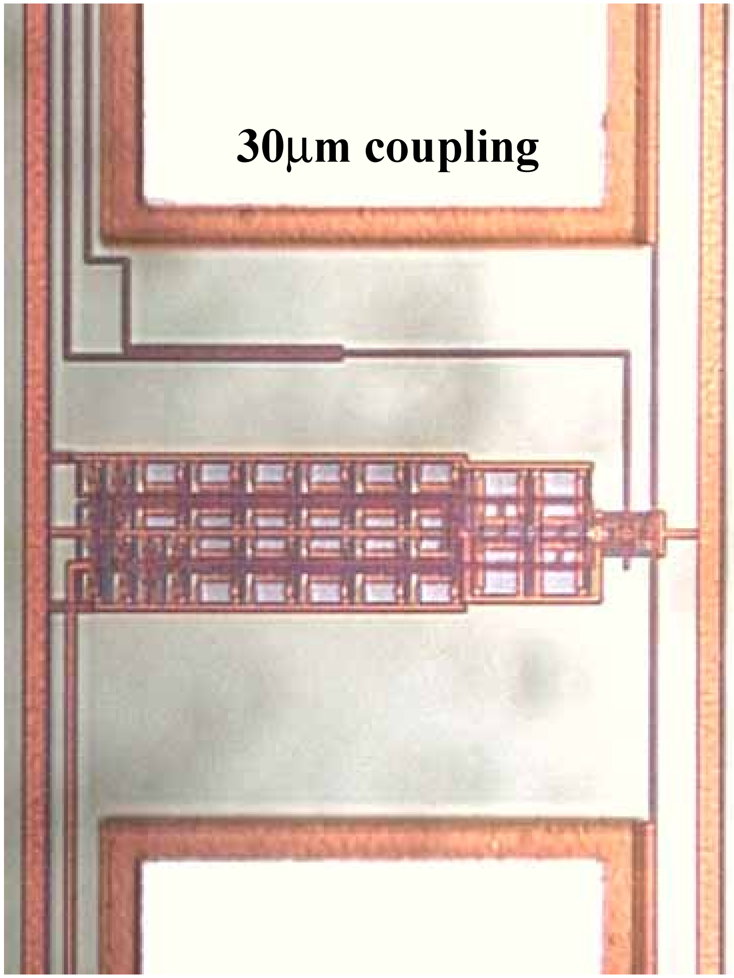
- non overlapping signal => no short circuit current
- f limited to fully charge/discharge C =>
- I = average (charging) current

$$C = \frac{I}{V_{dd} f}$$

On-chip Interconnect capacitance measurements (2): evolution (cross-talk based) and implementation



- Configuration for in line testing
- Buffered aggressors to minimize AC requirements on the on-wafer measurement system
- On-chip non-overlapping signal generator
- Pins: biases, aggressor, 'clock'



Cmeasured = 2.8fF

Defectivity Test Pattern

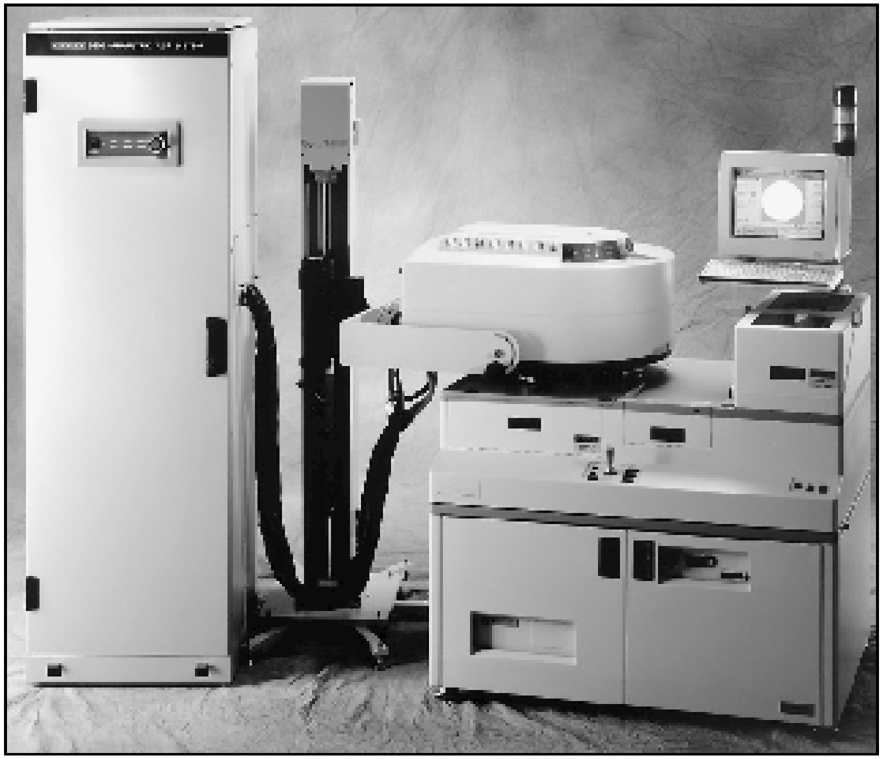
Generally is a “simple” circuit (inverter chains) designed to test the process as a whole: the signal has to cross ‘all’ the layers and the design should be as complex as a product.

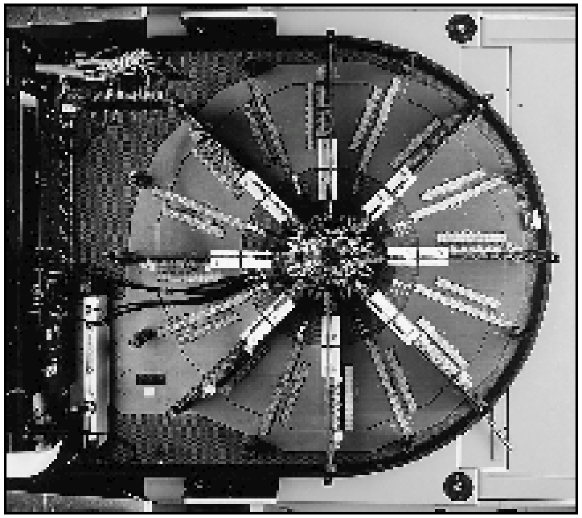
Large device/structure number:

e.g. 5 million MOSFETs
25million contacts/vias
1mm^2 of gate oxide area

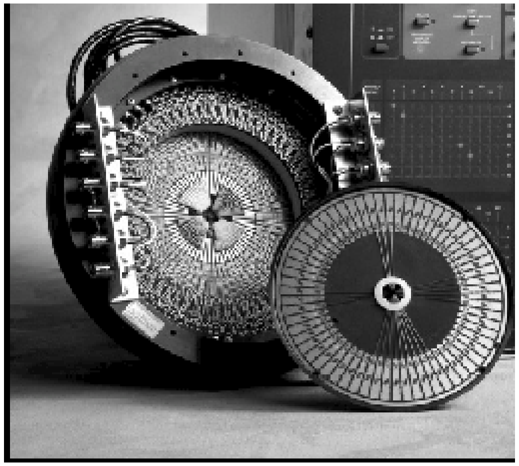
Wafer testability, easy failure analysis, possibility of packaged (life) tests, and to track defect density

On wafer measurement systems





Range:
0-200V
0-1A

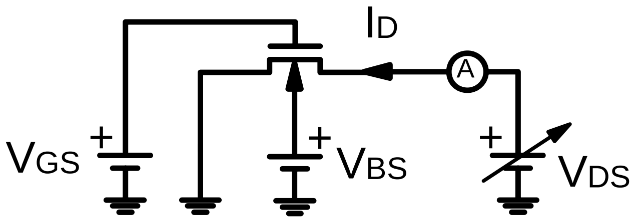


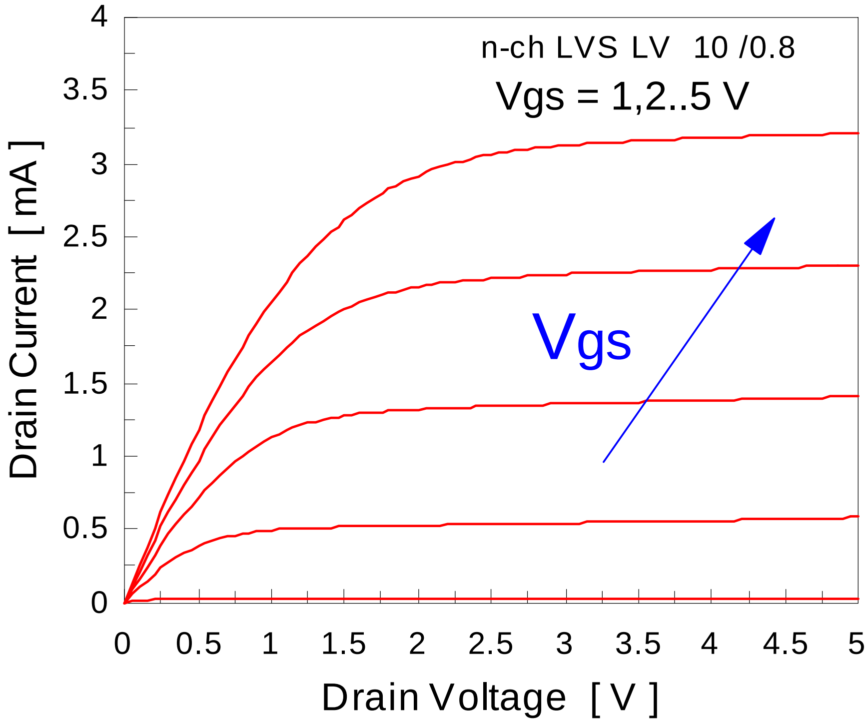
Requirements:
- -automatic, semi-automatic, manual
- -possible T measurements (-40…+125C)
- -high accuracy or high speed

(e.g. µV/fA resolution, 0.1% accuracy)

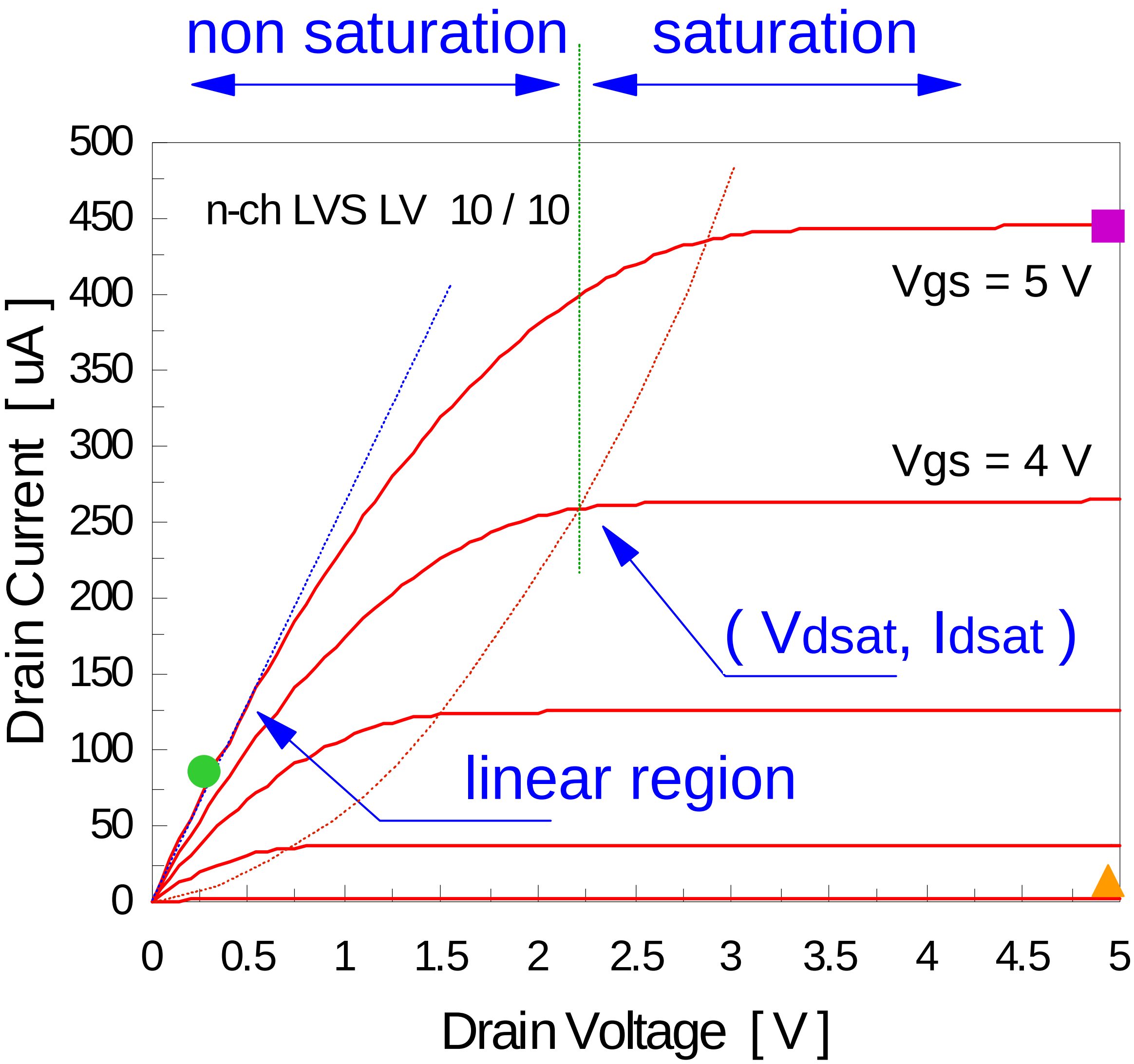
Output characteristics – 1

- Main constant parameters:
  - W_{NOM}, L_{NOM}, V_{GS}, V_{BS}
- Independent variable:
  - V_{DS}
- Measured variable:
  - I_D





Output characteristics – 2



Parametric testing parameters:

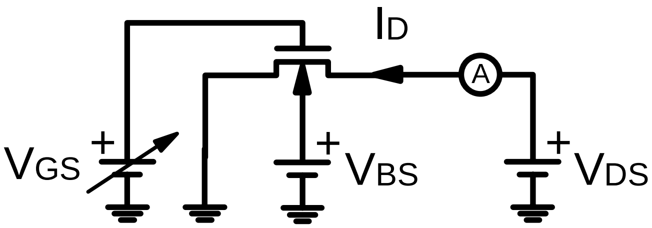
■ IDsat
@ Vg=Vd=VDD

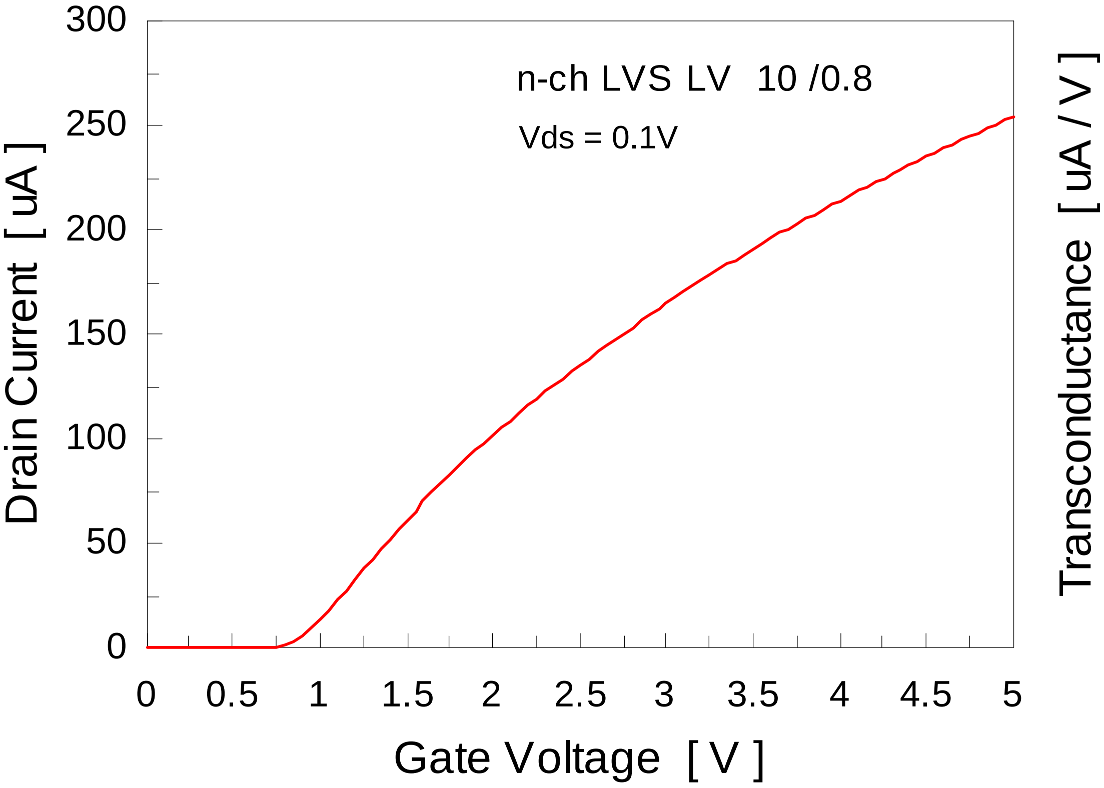
● Ron = Vd/Id
@ Vg=VDD
Vd=100mV

▲ Ioff (best on large W)
@ Vg=0V
Vd=VDD

Transfer characteristics – 1

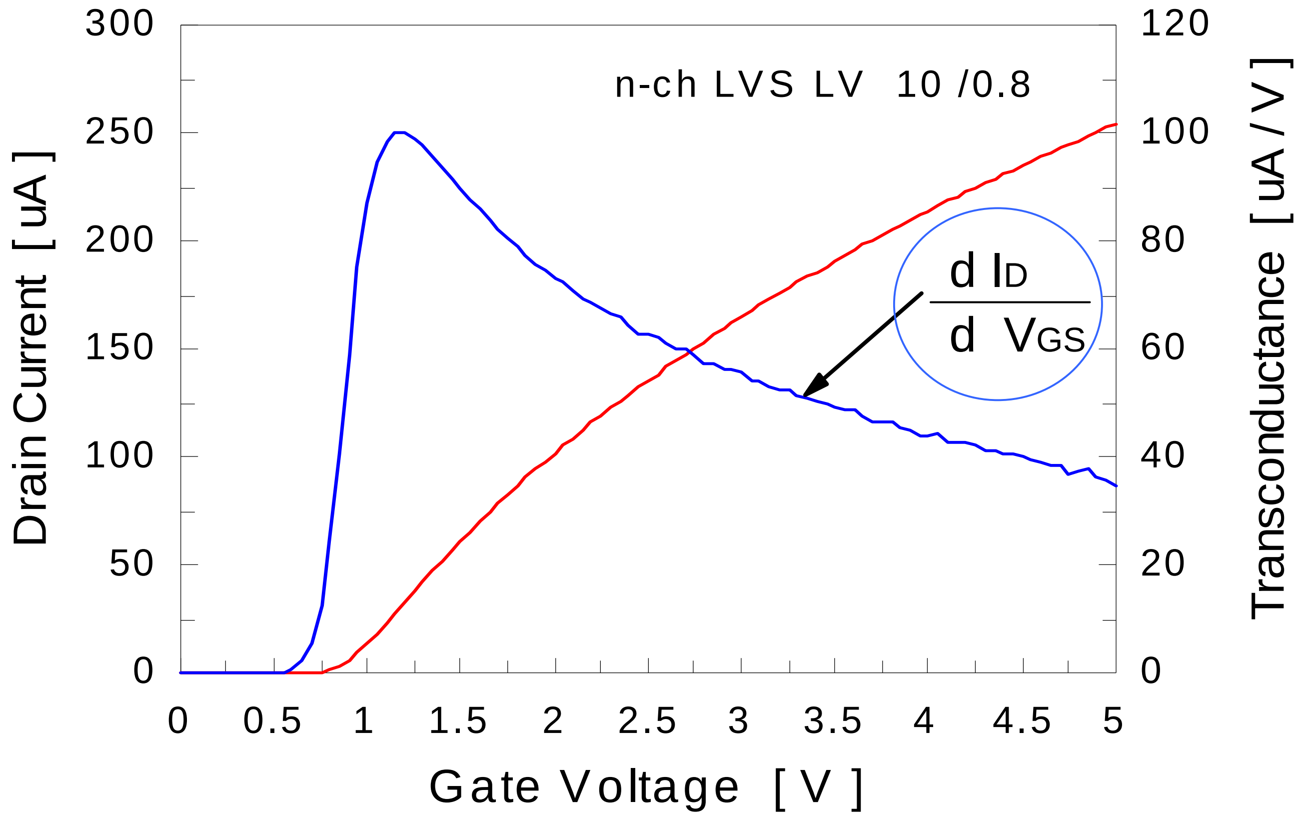
- Main constant parameters:
  - W_{NOM}, L_{NOM}, V_{DS}, V_{BS}
- Independent variable:
  - V_{GS}
- Measured variable:
  - I_D



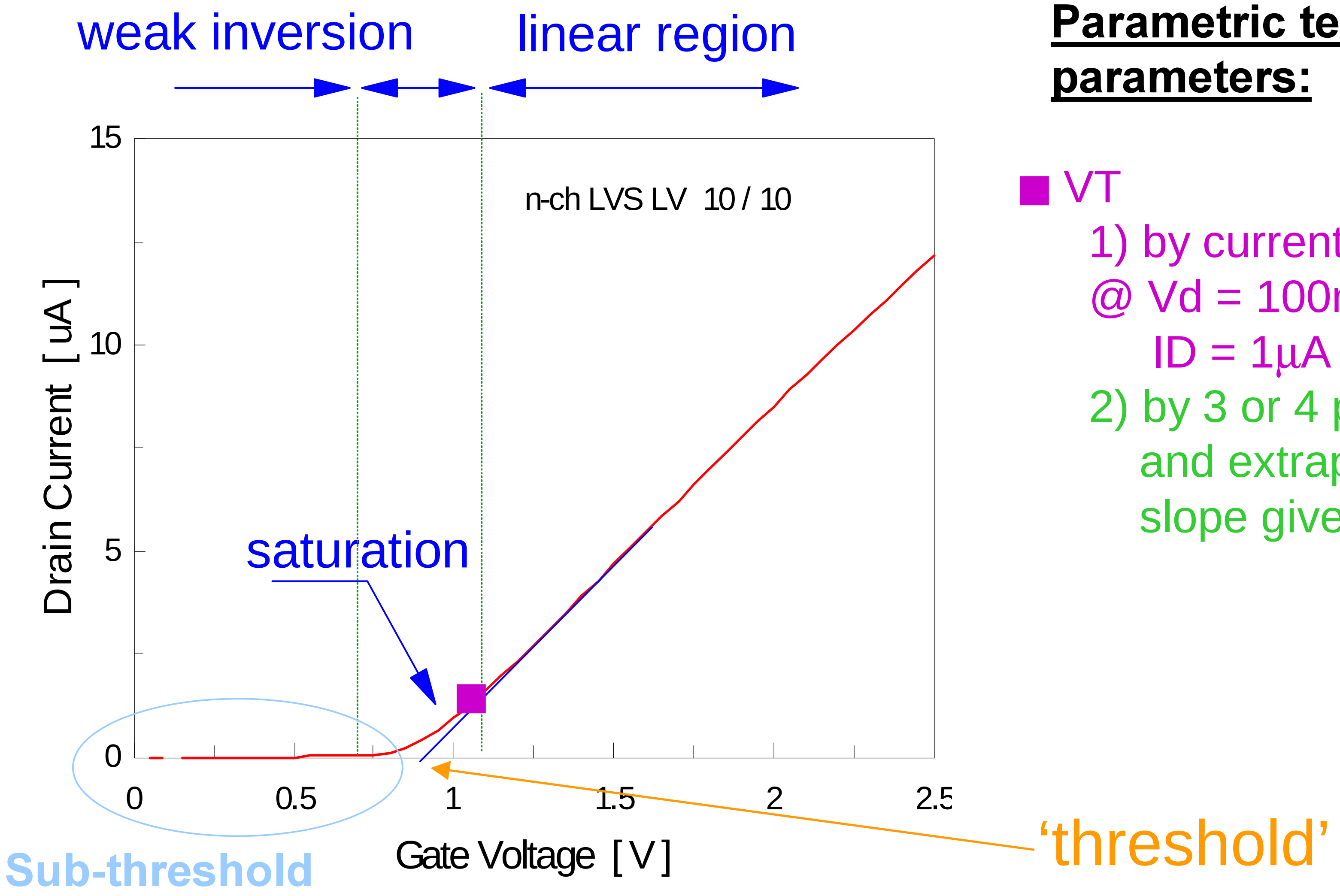


Transfer characteristics - 2 transconductance

- Parameters:
  - V_{DS} = 100 mV
  - V_{BS}= 0 V
  - W_{NOM} = 10 µm
  - L_{NOM} = 0.8 µm



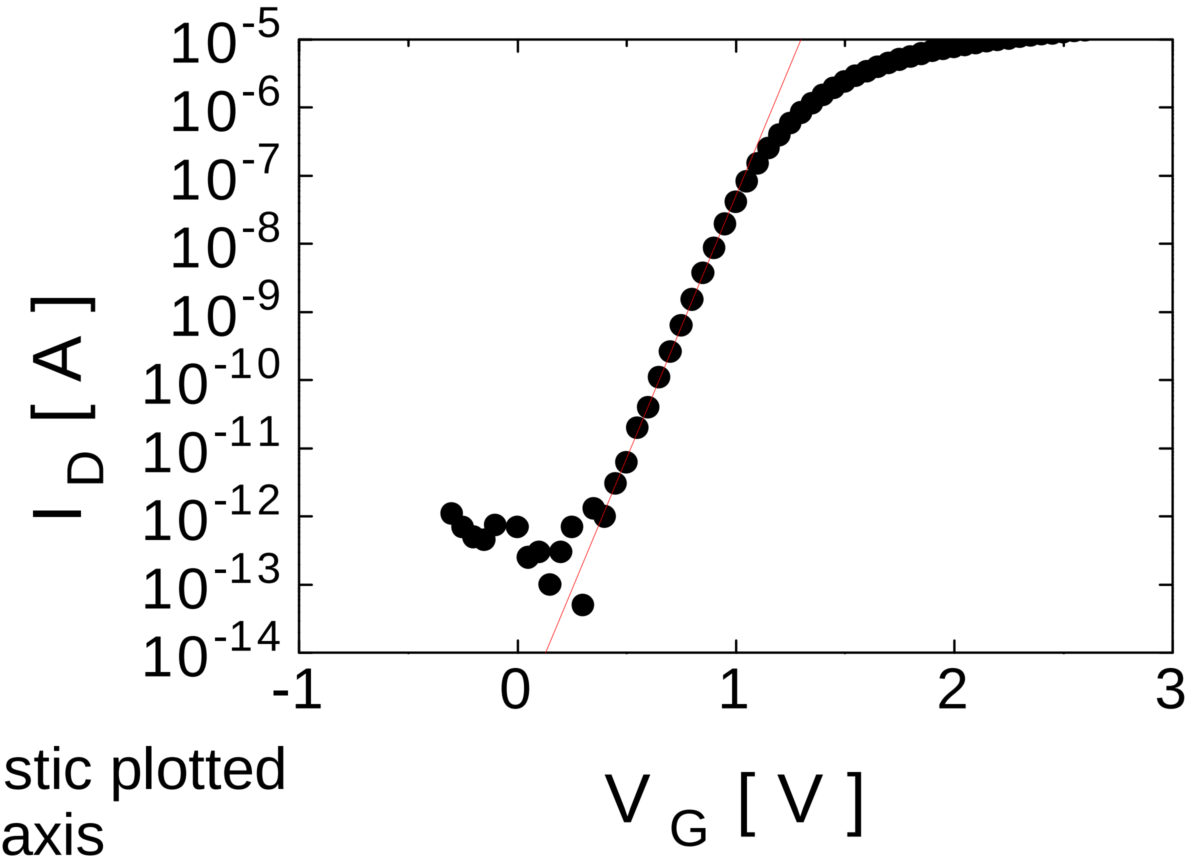
Transfer characteristics - 3
threshold (VT), β



Parametric testing parameters:

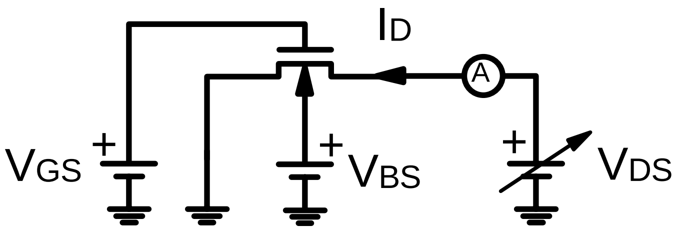
- VT
  1) by current
  @ Vd = 100mV
  ID = 1μA
  2) by 3 or 4 points
  and extrapolation
  slope gives β

Transfer characteristics – 4 Sub-threshold

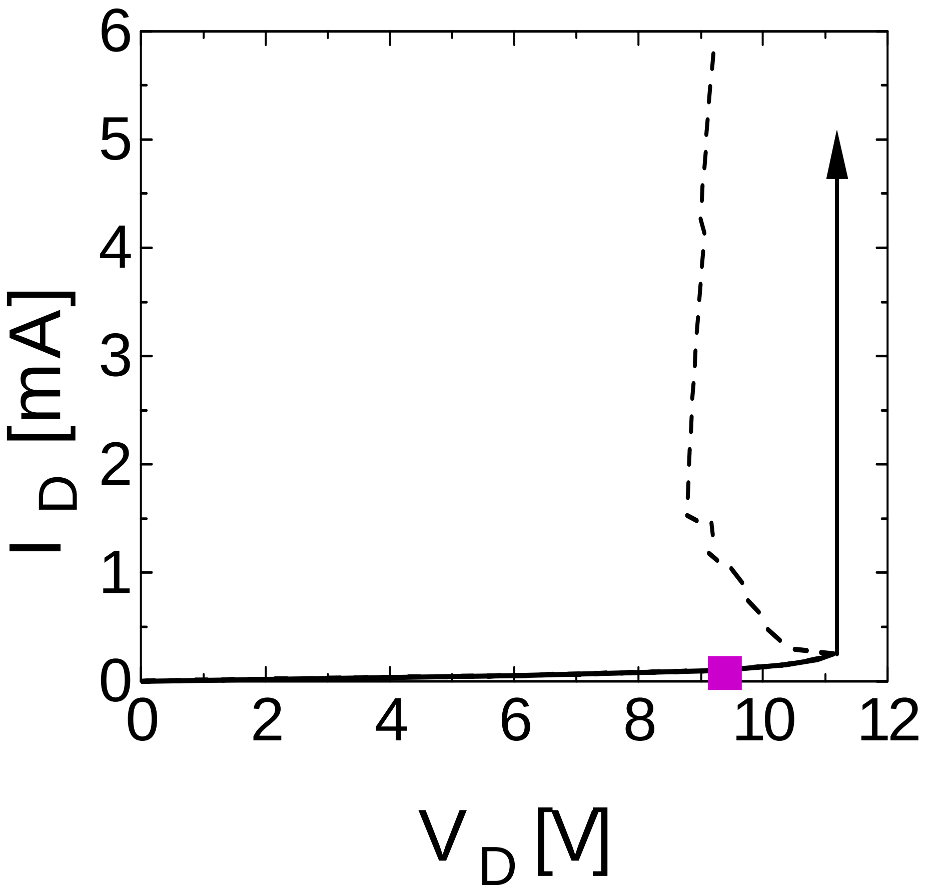


- transfer characteristic plotted with logarithmic y-axis
- normally the used sub-threshold parameter is the reverse of slope: 1/slope measured in mV/dec

Snap-back - 1



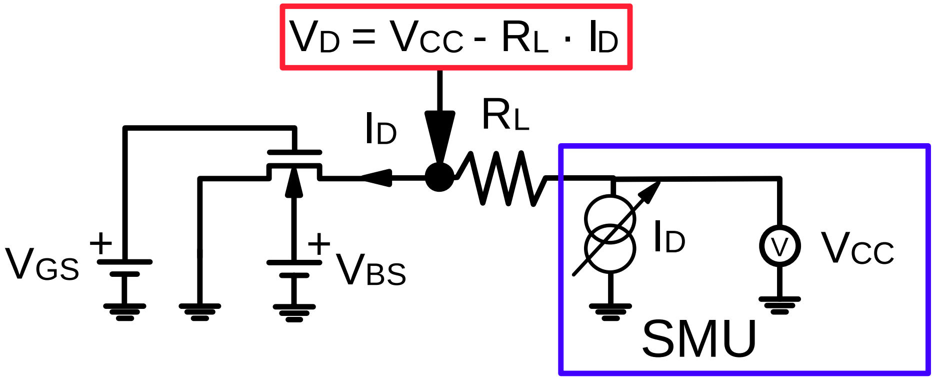
- Snap back curve is exactly an output characteristic, but
- If the measurement is made like a standard output curve, forcing a ramp voltage on the drain node, it is impossible to see the region at negative resistence.



<u>Parametric testing parameters:</u>

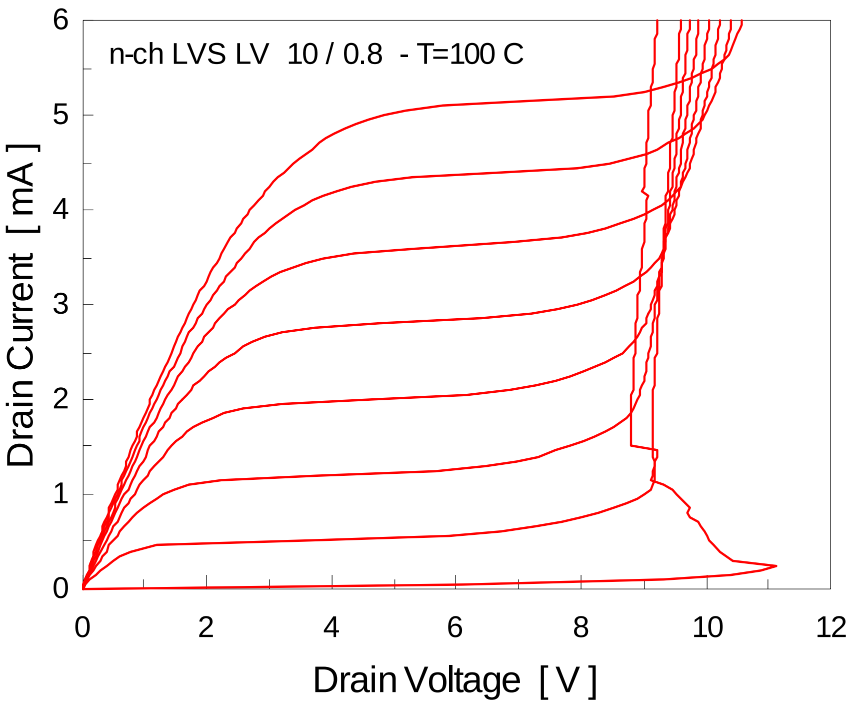
■ BV (often by current) @ Vg = 0V, ID = 10nA

Snap-back - 2



$V_D = V_{CC} - R_L \cdot I_D$

It is necessary to use a resistence on the drain to reduce the risk of heavy damaging of the sample

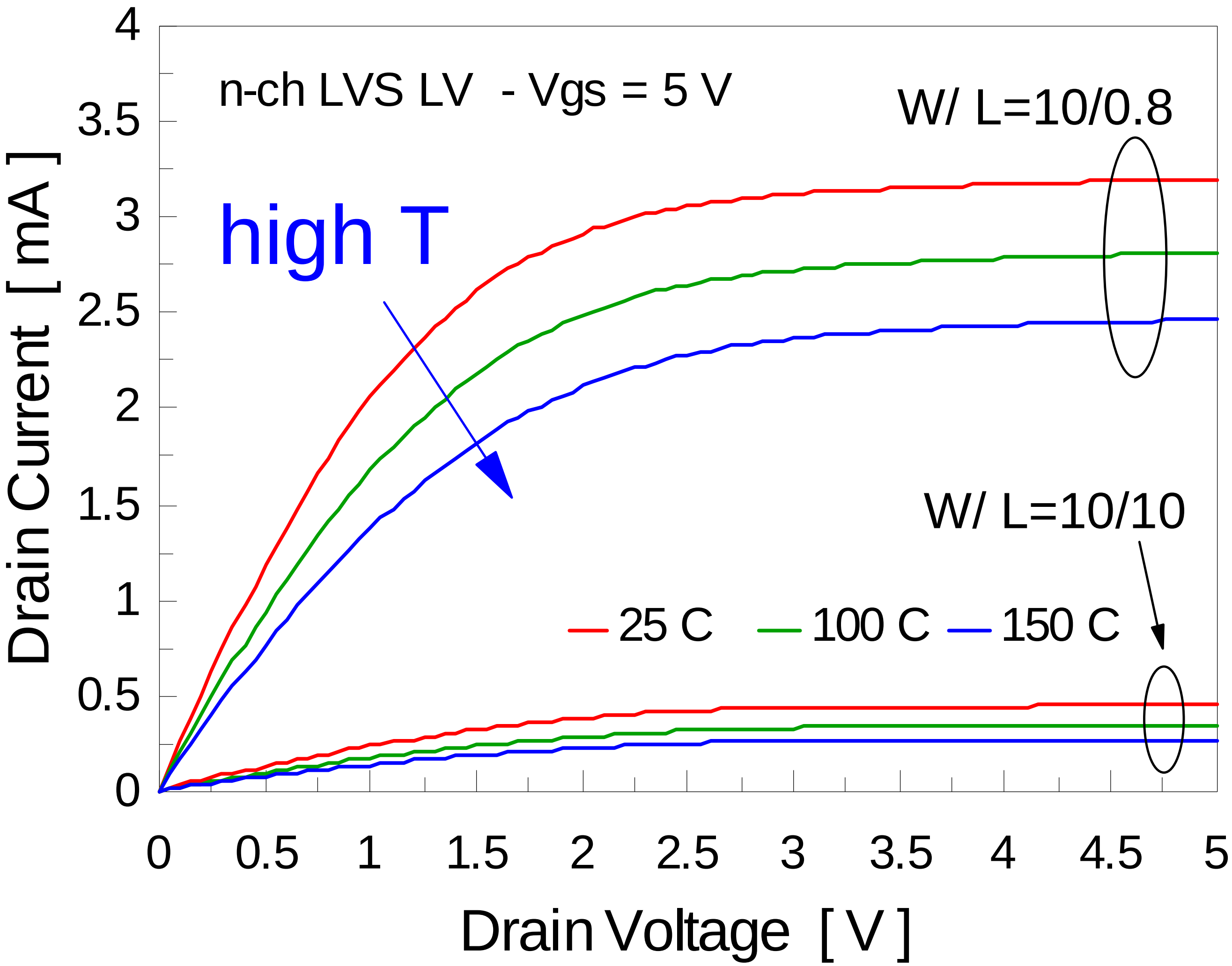


To measure characteristics with a negative resistance:

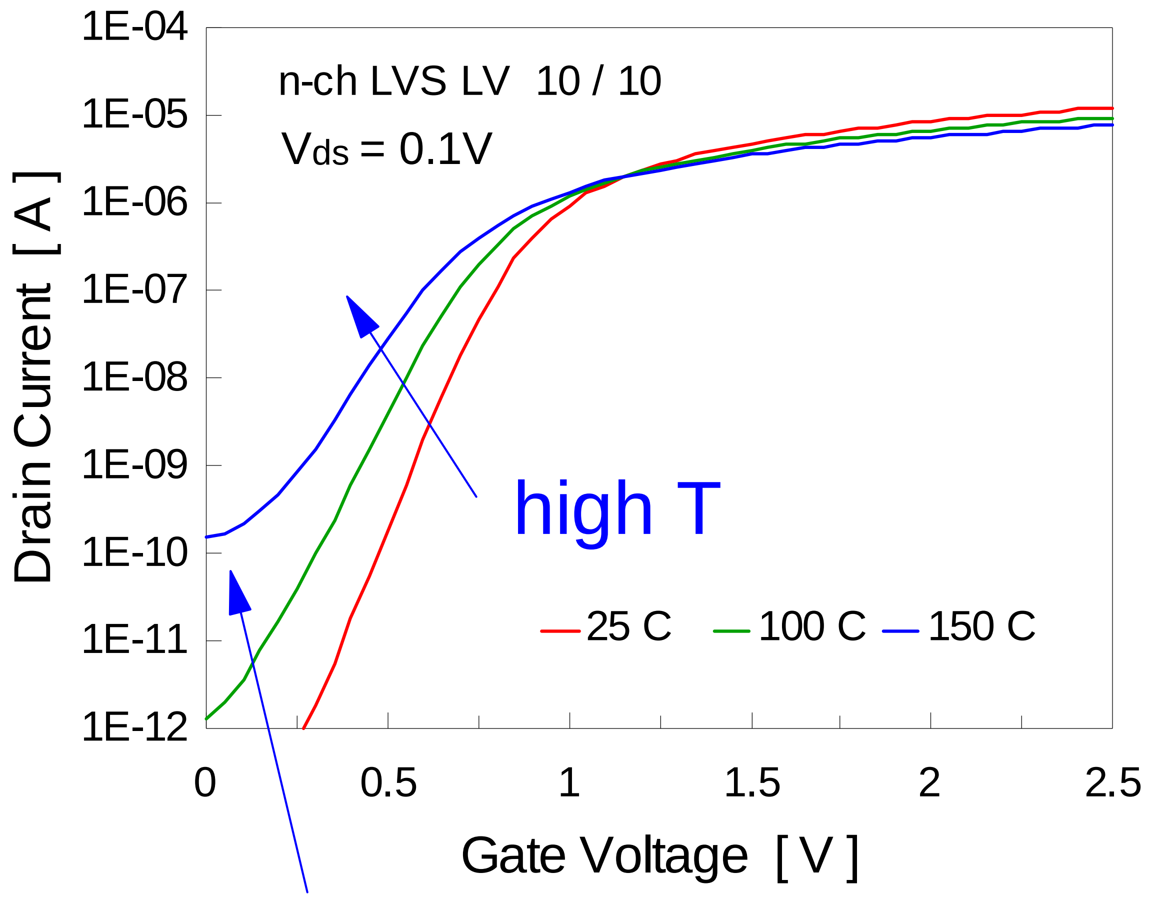
-use and external load resistance higher than the negative one

-force the current and measure the voltage

Temperature measurements -1



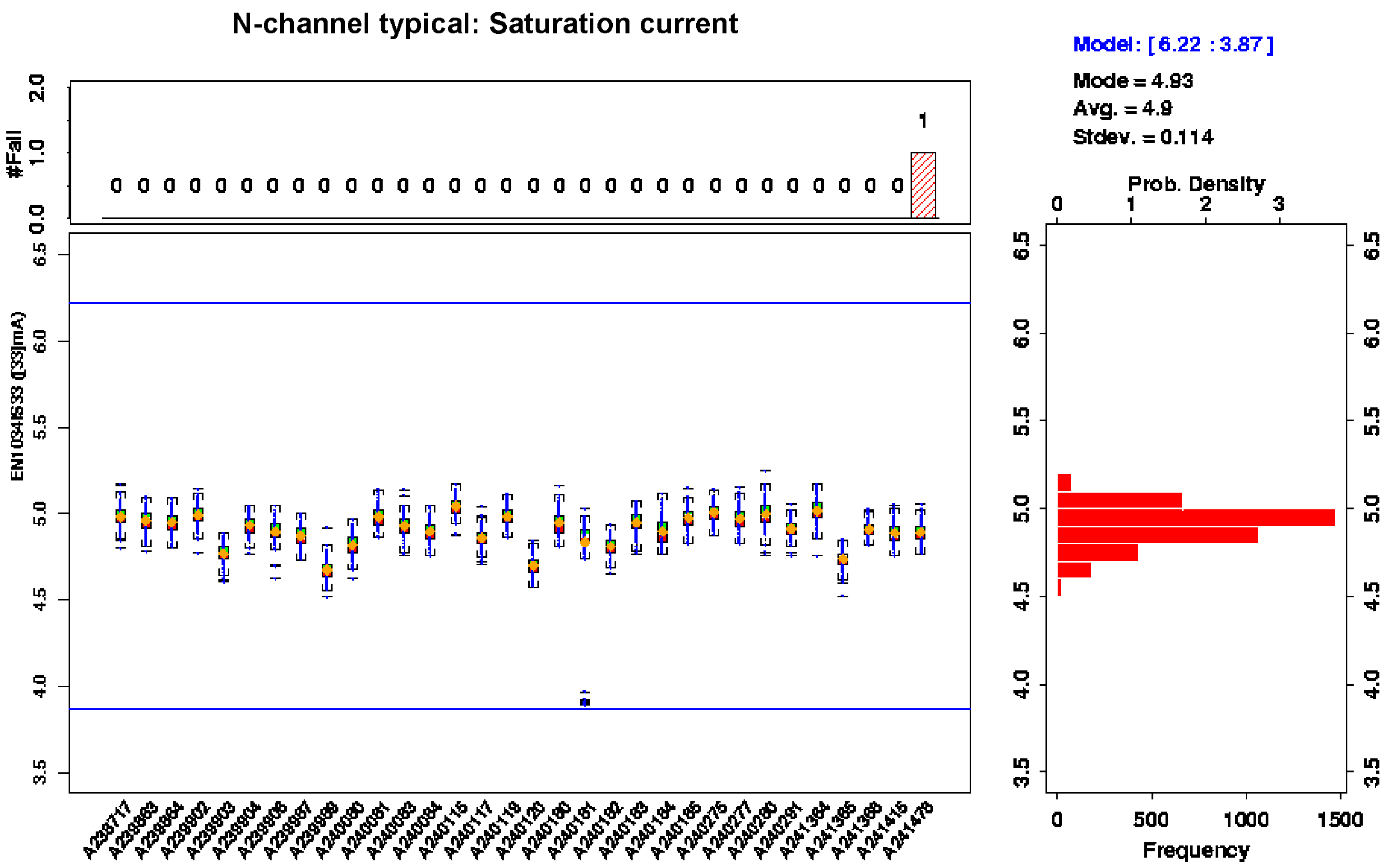
Temperature measurements - 2



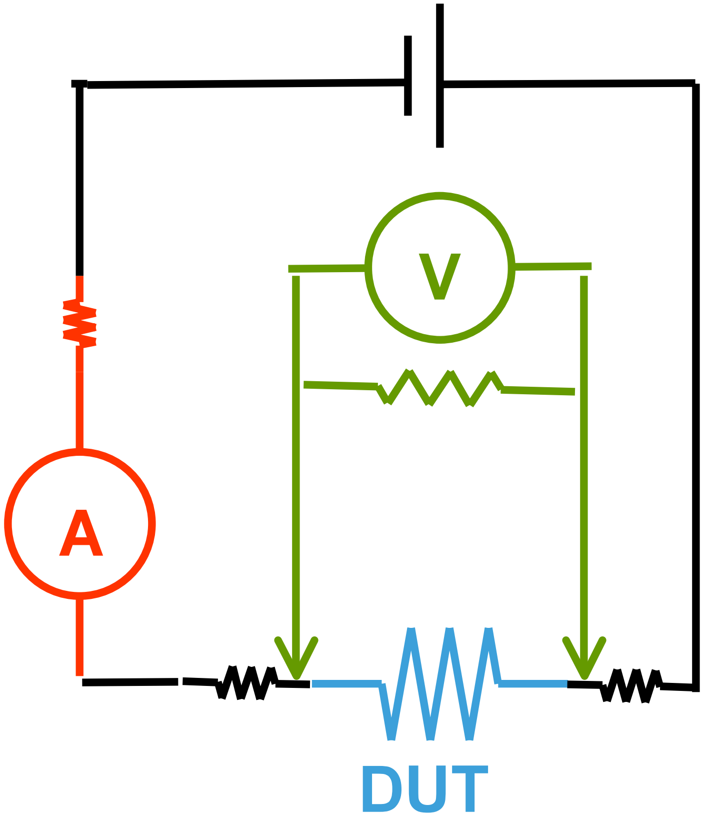
high T

exponential increase of
leakage current

Trend chart


N-channel typical: Saturation current
Model: [6.22 : 3.87]
Mode = 4.93
Avg. = 4.9
Stdev. = 0.114
#Fail
0.0
1.0
2.0
0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
1
EN1034533 (533|mA)
3.5
4.0
4.5
5.0
5.5
6.0
6.5
A238717
A239963
A239964
A239902
A239903
A239904
A239906
A239987
A239988
A240080
A240081
A240083
A240084
A240115
A240117
A240119
A240120
A240180
A240181
A240182
A240183
A240184
A240185
A240275
A240277
A240280
A240281
A241384
A241385
A241388
A241415
A241478
Prob. Density
0
1
2
3
0
500
1000
1500
Frequency

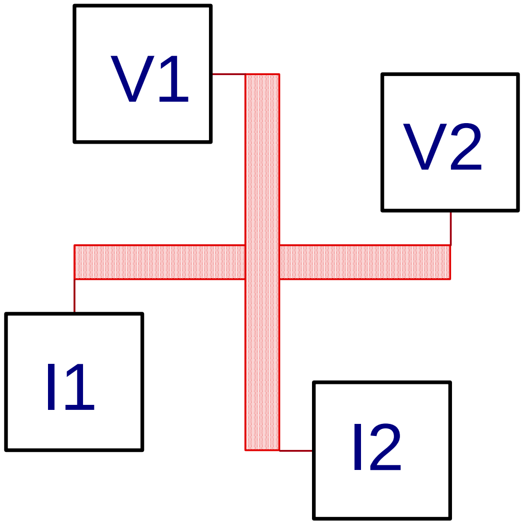
Resistance measurements issues: Kelvin measurements



-Non ideality of:
sources, voltmeters and ammeters
(undesired loading effects)
-Cable and contact resistances
(additional resistance contribution
measured)
-Other effects:
Joule heating (may change R)
Stray currents paths (leakage in
semiconductors – light effects!)

Resistance test structures

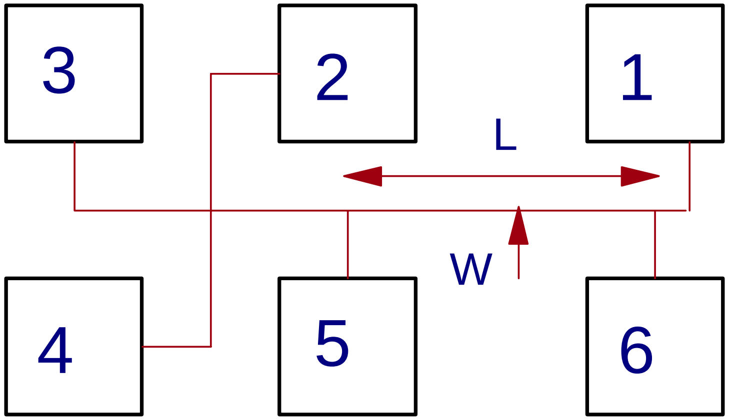
- Cross: based on Van der Pauw measurement



$Rs = 4.53 \times V/I$

Sheet resistance

Kelvin structure



$Rs = (\pi/\ln2) \times (V32/I45)$

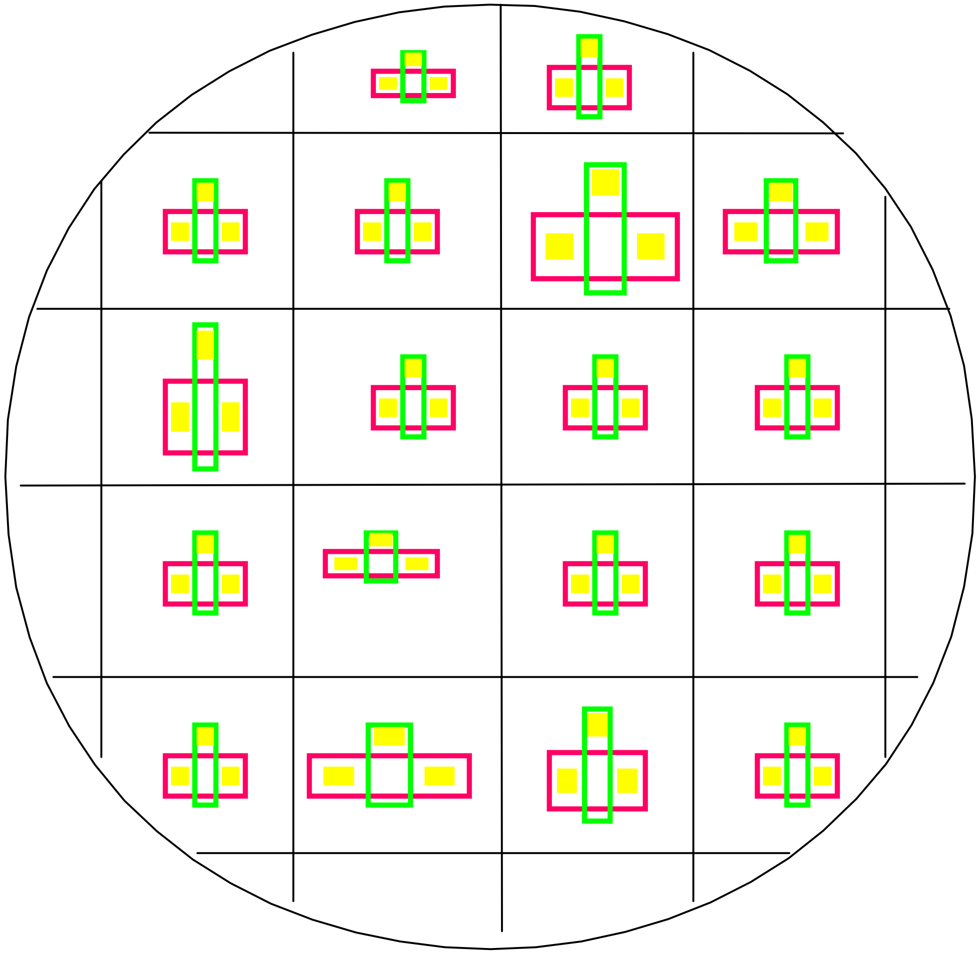
$W = Rs \times L \times (I41/V56)$

Sheet resistance
Dimensional control (W)
Resistance

MATCHING

- Transistor matching: ‘characterization of differences between closely spaced identical transistors’
- Material from: Hans Tuinhout, Maarten Vertreght (Philips Research Labs) et al., IEEE ICMTS short courses ’98 and ’99, Medea workshops
- Parametric spread
- Matched pairs and their layout
- Analogue circuits & matching
- Matching characterization and modeling

PARAMETRIC SPREAD



Variation of transistor properties (spread) is due to deterministic variations across the wafer:

-critical dimensions: ΔCD
-layer thickness: Δt
-furnace temperatures: ΔT
-uniformity of chemicals: ΔC

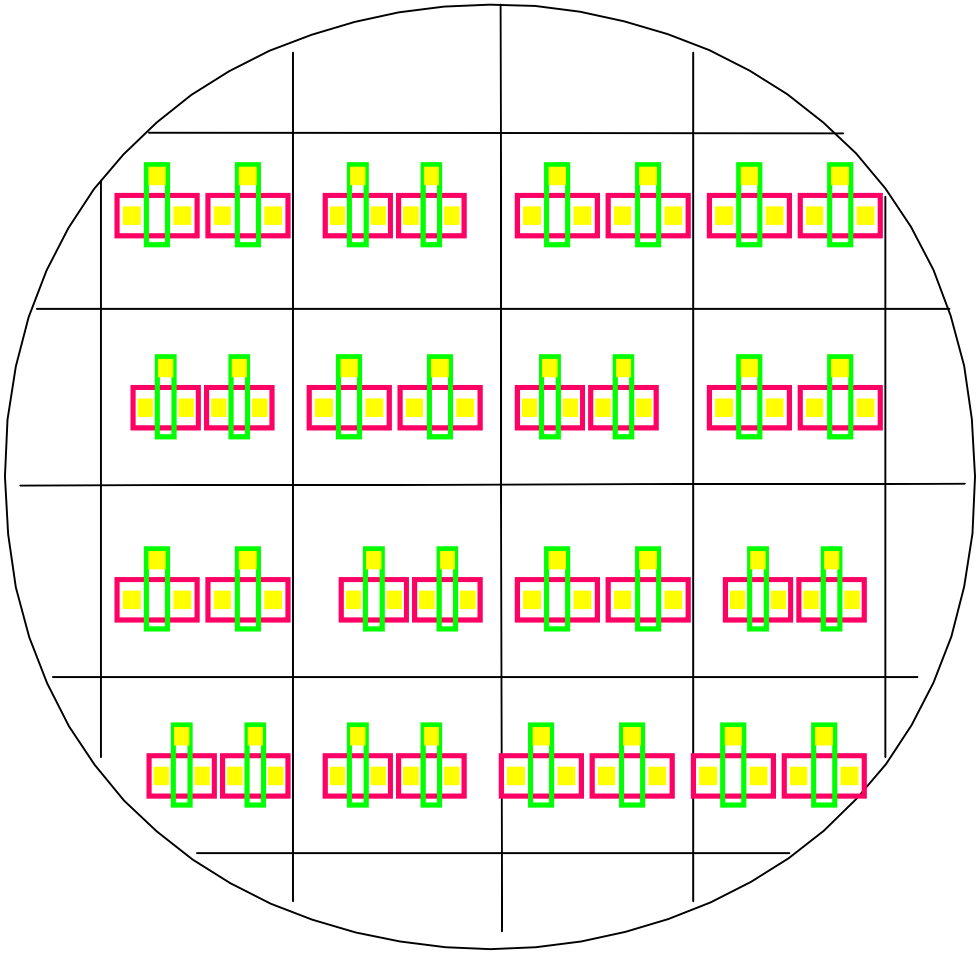
⬇

Resulting variation of electrical transistor properties (spatial parametric variations):

-currents: 5-15%
-voltages: 10-50mV

Solution: better process control and equipment improvements, or….

MATCHED PAIRS



Differences between **identically designed components** placed at a small distance in an identical environment:

MISMATCH

Electrical transistor properties show much smaller differences:
-currents: 0.01-5%
-voltages: 0.2-10mV

Due to the small distance between the components, observed differences are not caused by deterministic effects but by **stochastic** (random effects)

Rules for absolute values and matching

- **ABSOLUTE VALUES**:
  - **Good control of geometries: e.g. avoid structure uncertainties due to folding, end effects, clearance…**
  - **Non minimum dimensions**
- **MATCHING:**
  - **Same: structure, temperature (*), shape, size, orientation, surroundings, neighborhoods**
  - **Common centroid geometries**
  - **Minimum distance**
  - **Non minimum size**

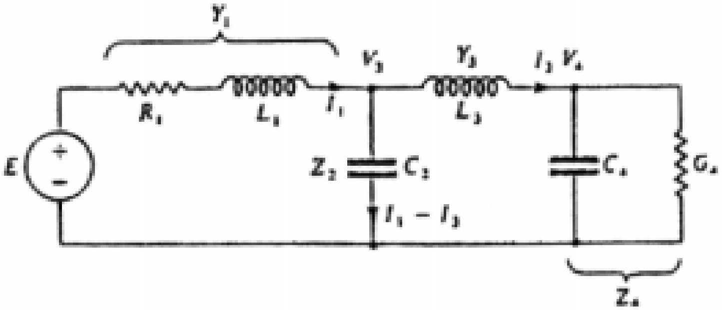
(*) also during transients, place on same distant isotherm

From: E. Vittoz “Advanced CMOS & BiCMOS IC Design ’99”

MATCHING & DESIGN

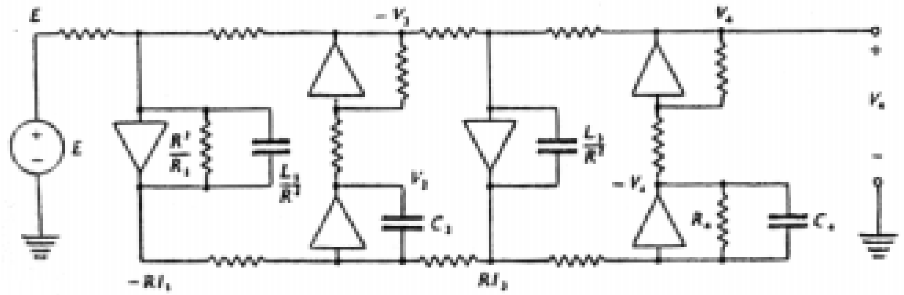
- BACKGROUND:
  - The absolute electrical values of devices varies wafer to wafer and lot to lot (e.g. 10-30%)
  - If a design is based on RATIOS of electrical quantities the variations are reduced (e.g. 0.1-1%)
  - The absolute accuracy is replaced with matching accuracy
  - Many analogue circuits are based on using pairs or multiples of supposedly identical components: current mirrors, differential pairs, opamps, comparators, A/D, D/A, PLL,...
- MISMATCH is defined as:
  - “...the random differences between identically designed devices caused by time-independent random variations in physical quantities (doping, oxide)”
- MISMATCH therefore cannot be completely removed but can be reduced by applying appropriate design rules and can be measured/monitored

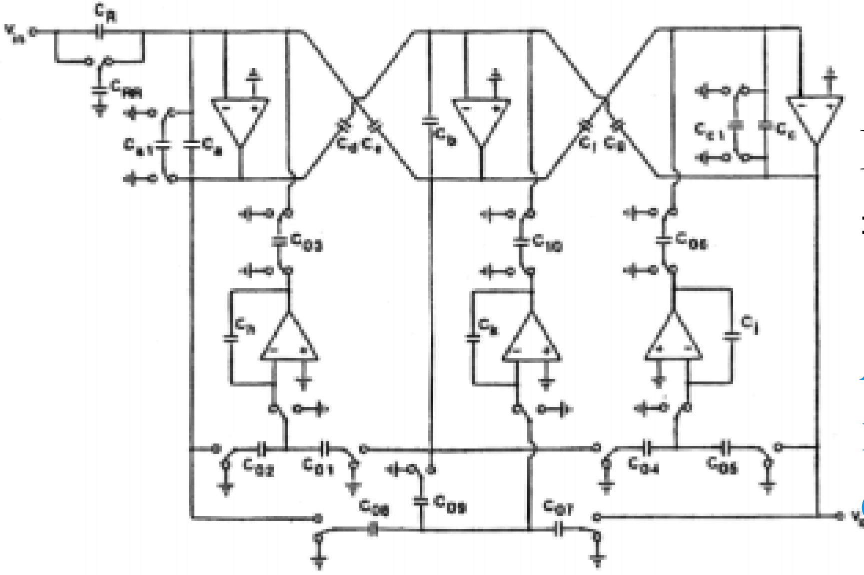
Circuit evolution



Example: from a discrete LRC filter…

…to active RC filter:
OPA⇔L, but discrete R…

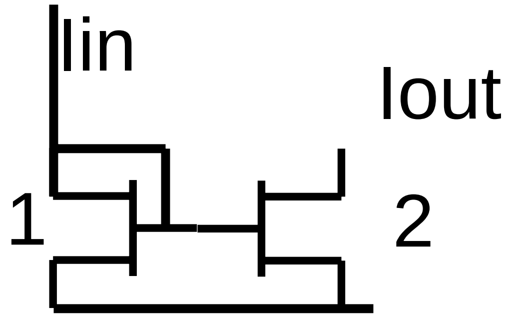




…to switched-capacitor filter:
R replaced by [MOS] capacitors
⇒ <u>Fully integrated</u>

Absolute accuracy of R&C (10-30%) replaced with matching accuracy of C (0.05-0.2%)

Current mirrors



- High Rout => high L
- Iout=Iin(W2/L2)/(W1/L1)
- For matching: L1=L2
- For good matching: large Vgs-Vt
  so Vt mismatch is unimportant, but
  I matching is “gain” matching in the limit:
- Example: NMOS, Vt=0.5V
  $\sigma(\Delta id/Id)$:

W/L(um/um)	@ Vg=	0.7V,	1.1V,	1.8V
0.5/0.18		20%,	9%,	3%
30/10		0.5%,	0.2%,	0.1%

MATCHING assumptions and implications - 1

- Random matching is composed of many single events of a mismatch generating process
- The effects on a parameter are so small that the contributions to the parameter can be summed
- The effects have a correlation distance much smaller than the area of interest (the active area of the components)

Valid for: distribution of doping ions, oxide charges, mobility fluctuation, grains, etc.

Implications:

Occurrences of these events are mutually independent (Poisson Statistics)

Central limit theorem: Let X1, X2…Xn be independent random variables which are identically distributed, then P=X1+X2…+Xn is asymptotically normal distributed

=>

MATCHING assumptions and implications -2

- This will result in a Normal (Gaussian) distribution of the random mismatch amplitude
- If the occurrence of the single events in P are mutually independent:
  - The average value of the event density Fp is constant
  - The mean value of events in an area WL will be WLFx
  - The variance of events in an area WL is σ^2=WLFx
  - Or, per unit area:

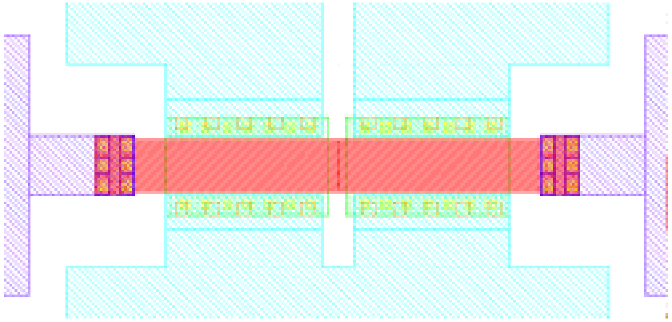
$$\sigma \propto 1/\mathrm{sqrt}(WL)$$

D.O.E. MOSFET matched pairs

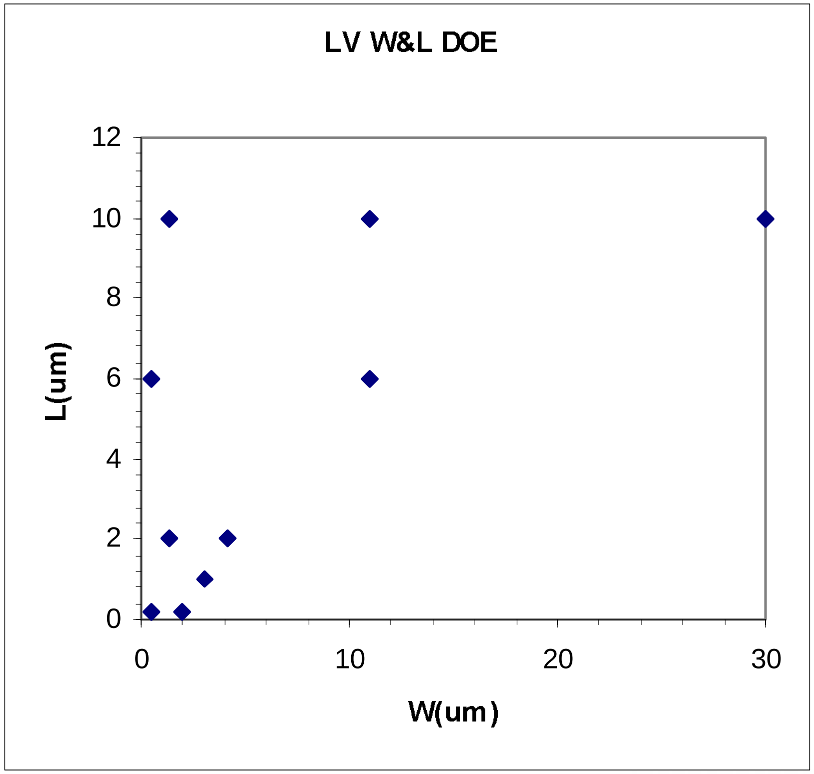
- A ladder of matched pairs with different size is done for each device of interest: e.g. C, R, MOS (see the example below)

LV	
W(um)	L(um)
30	10
11	10
11	6
1.4	10
4.2	2
0.5	6
3.1	1
1.4	2
2	0.18
0.5	0.18

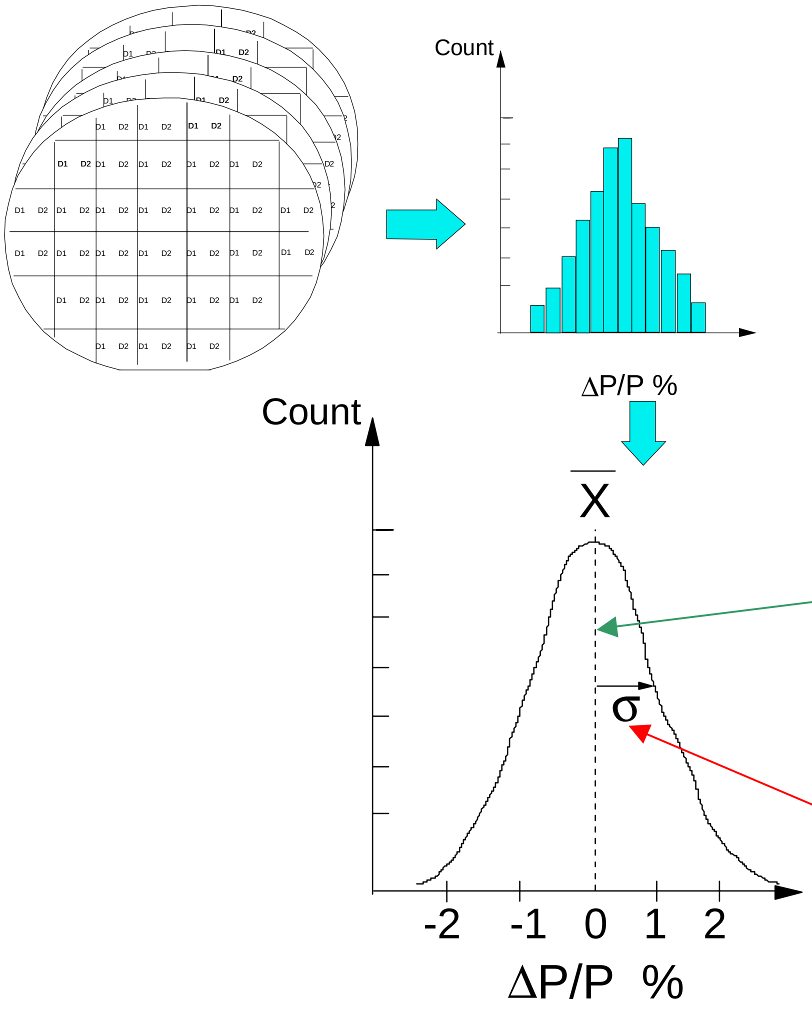
HV, LV_nat	
W(um)	L(um)
30	10
11	10
11	6
1.4	10
4.2	2
0.72	6
3.1	1
1.4	2
2	0.64
0.72	0.64



Min. spacing & Gate protected



Matching measure & modeling-1



Vth:

$\Delta P = P1 - P2$

Beta, Id, R, C:

$\Delta P/P(\%) = 200*(P1-P2)/(P1+P2)$

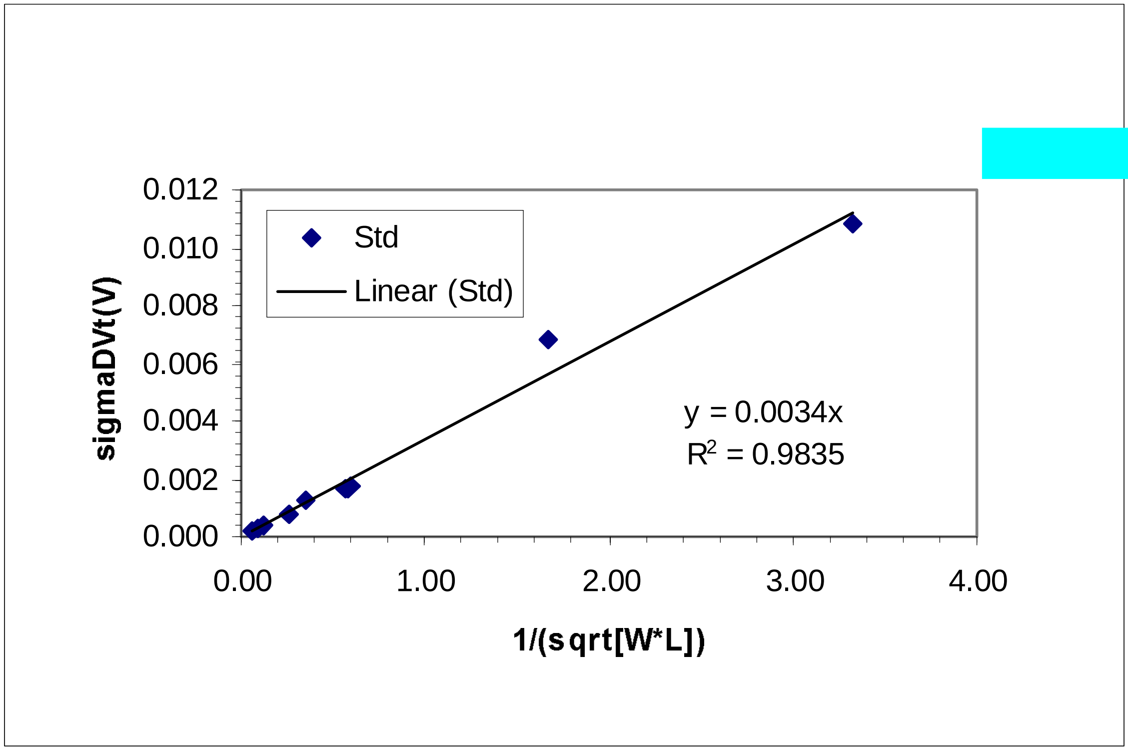
In a well designed pair the difference is close to 0
The mean indicates an OFFSET, a 'systematic mismatch'

σ represents the MATCHING, the physical stochastic (Random) effects

The characterization is done for all the pairs of the DOE

Matching measure & modeling-2

Plot sigma(ΔP) or sigma(ΔP/P) versus 1/sqrt(W*L)



$$\sigma_{\Delta VT} = \frac{A_{vt}}{\sqrt{W \times L}}$$

ΔVT = VT1 – VT2,

A_{VT} (mV.µm),

For other parameters, e.g.:

$$\sigma_{\left(\frac{\Delta beta}{Beta}\right)} = \frac{A_{beta}}{\sqrt{W \times L}} + B_{beta}$$

A_{beta} (%.µm) and B_{beta} (%)

At first order larger devices gives better matching

MATCHING measurement challenges

- Matching characterization deals with SMALL DIFFERENCES (current or voltages)
- Measurement system <u>short term repeatability</u> is very important:
  - Stability of meters and sources
  - Temperature stability (e.g. thermo-chuck control in +/-0.1 º C)
- BJTs are more critical: Ic varies 0.1% per 0.01ºC!
- Careful should be paid on resistance drop (Kelvin structures)
- Statistical sample dimension is a tradeoff between speed and statistical uncertainty: robust statistical estimation techniques (outliers…) are required
- ….

Analog versus digital

	Signal represented by:	**Electrical processing with:**
DIGITAL	**numbers (codes)**	**regeneration**
ANALOG	**physical values (V, I, Q, f)**	**No regeneration**

⇩

Related Layout Topics:		**Distortion**	**Noise**
-variety of sizes and shapes	■		■
-absolute values (as few as possible)	■		
-matching (designs based on <u>ratios</u>)	■	■	
-parasitics	■	■	
-long-range coupling		■	■

From: E. Vittoz “Advanced CMOS & BiCMOS IC Design ’99”

Parasitic effects

- Various types:
  - Capacitance: to ground or from node to node
  - Series resistance of layers / parallel conductances
  - Leakage currents, re-collection of minority carriers
  - Long-range coupling
- Results in various effects:
  - Speed/bandwidth reduction
  - Degradation of precision
  - Distortion of characteristics, CMRR degradation,…
  - Noise / feed-through / interactions / losses
- Solution: eliminate, minimize, compensate (by matched structures)

From: E. Vittoz “Advanced CMOS & BiCMOS IC Design ’99”

Long-range coupling

- **Cohabitation on same chip of :**

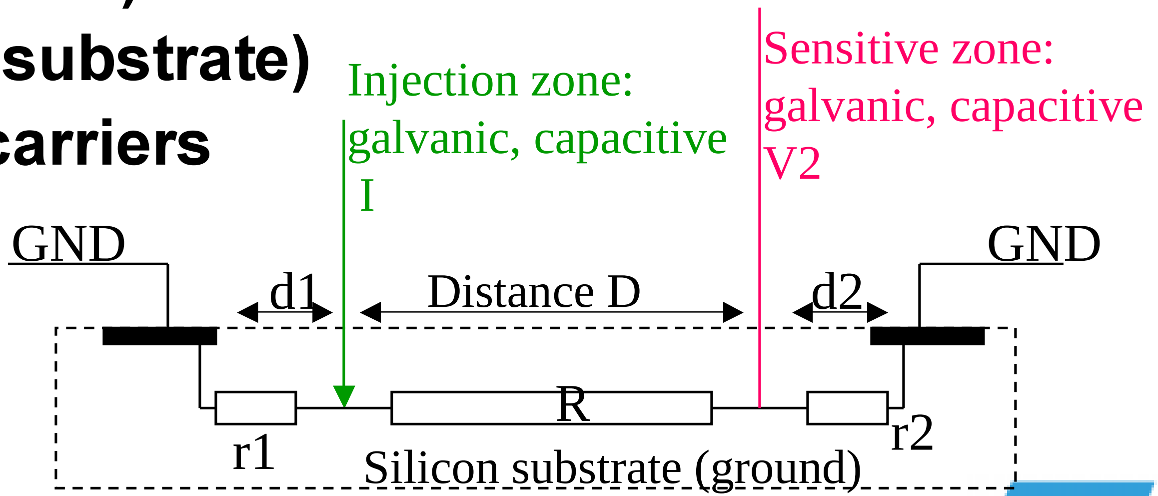
Digital/High level analog (V) - <u>120dB attenuation required</u> - Low level analog (µV)

- **Coupling mechanisms:**
  - **Power lines: use separate V+, V-, GND, wide wires**
  - **Resistive (through substrate) (*)**
  - **Capacitive (in air)**
  - **Thermal (via substrate)**
  - **By minority carriers**

(*) If $R \gg r1, r2$

$V2 \approx I*r1*r2/R$

=> Min d1, d2; Max D; well



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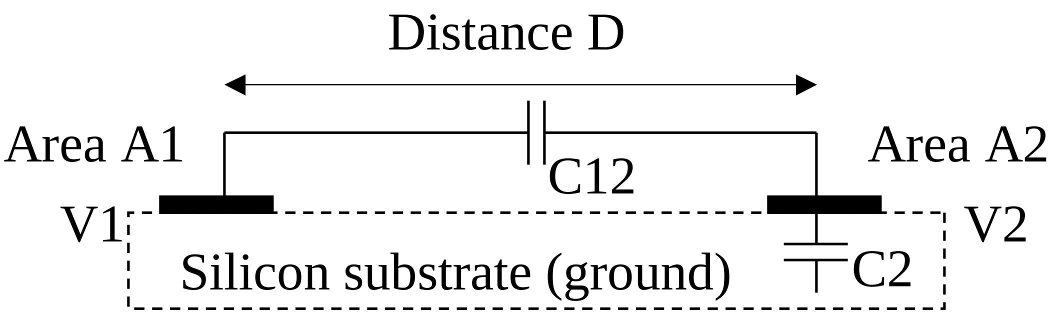
Capacitive coupling through air



A1, A2: diffusions (drain), interconnects

Hypothesis: C12<<C2

$$V2 \approx V1*C12/C2$$

If $D^2 \gg A1$ and $A2$ then $C12 \approx \dfrac{\varepsilon 0*A1*A2}{2*\pi*D^3}$

Examples for 120dB attenuation:

A1(µm2)	A2(µm2)	C2(fF)	C12max(F)	Dmin(µm)
10	10	5	5E-21	30
10000	10	5	5E-21	300
10000	10000	100	100E-21	1120

Improvements: reduce A1, A2; increase D; shield A1 or A2

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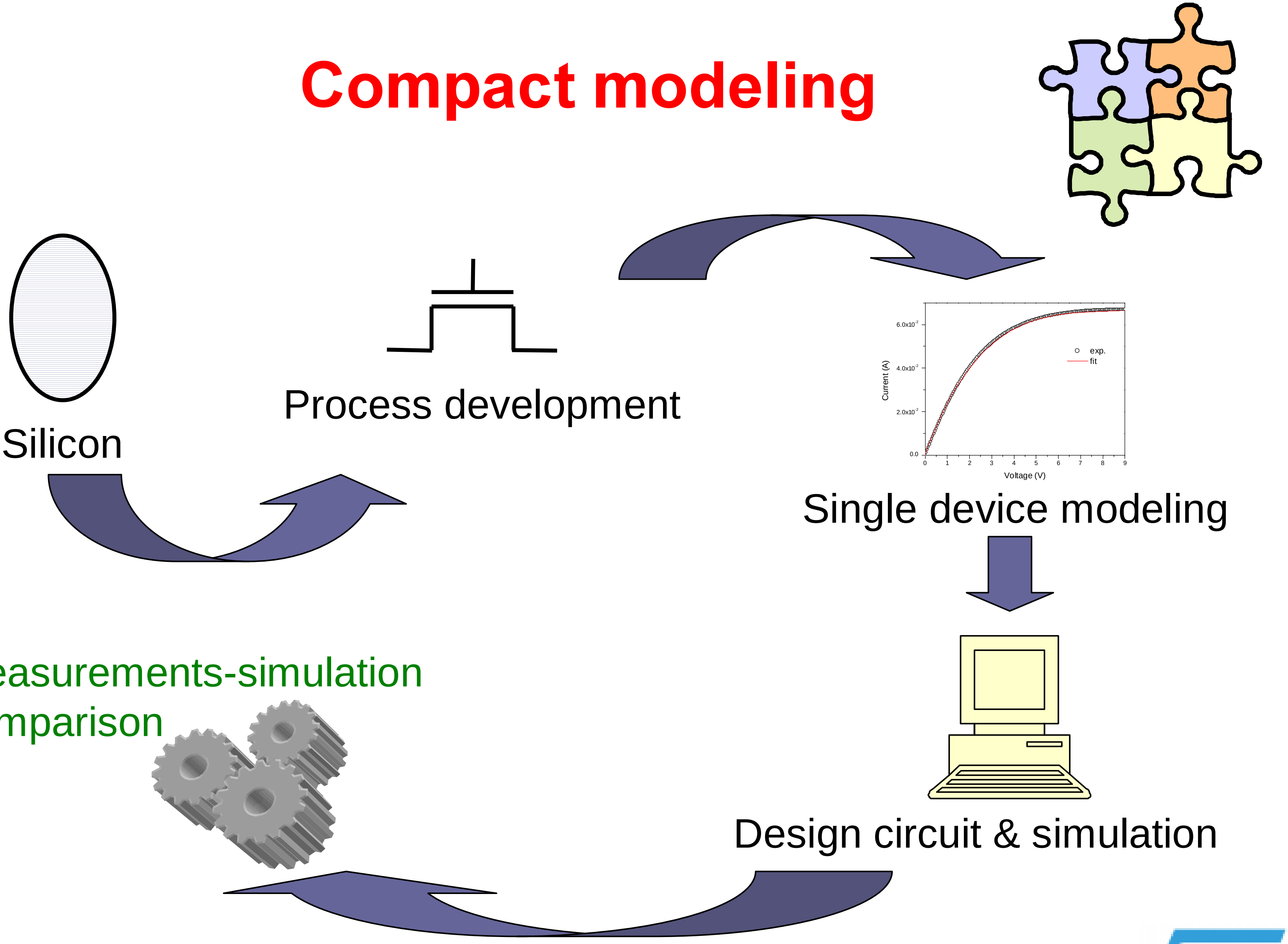
Compact modeling



Silicon

Process development

Single device modeling

Design circuit & simulation

Measurements-simulation comparison

Compact model: definition

✓ A compact model describes the device electrical behavior by using analytical functions containing parameters:

$$I_S = \beta \bullet G_3 \bullet \frac{V_{GT3} \bullet V_{DS1} - \left(\frac{1+\delta_1}{2}\right) \bullet V_{DS1}^2}{\{1+\theta_1 \bullet V_{GT1} + \theta_2 \bullet (u_s - u_{s0})\} \bullet (1+\theta_3 \bullet V_{DS1})}$$

$$V_{GT3} = 2 \bullet m \bullet \phi_T \bullet \ln(1+G_1)$$

$$G_1 = \exp\left(\frac{V_{GT2}}{2 \bullet m \bullet \phi_T}\right), \quad V_{GT2} = V_{GS} - V_{T2}$$

$$V_{T2} = VTOR + bodyeffect + DIBL + staticfeedback$$

MOSFET Models ‘philosophy’

➢ I generation ⇒ start from a simple physical device description (a small number of parameters)

➢ II generation ⇒ use a strong mathematical approach in order to grant the simulation robustness (number of parameters diverges)

➢ III generation ⇒ recover the physical approach considering the phenomena complexity due to down-scaling technology (large number of parameters)

⇩

BSIM3/4 & Philips MOS Model 9/11 (MM9/11)

Modeling issues

✓An accurate and extensive electrical characterization in a large operating bias and temperature domain is needed

✓Extract a model card consists in finding the best values of model parameters in order to picture the real device behavior.

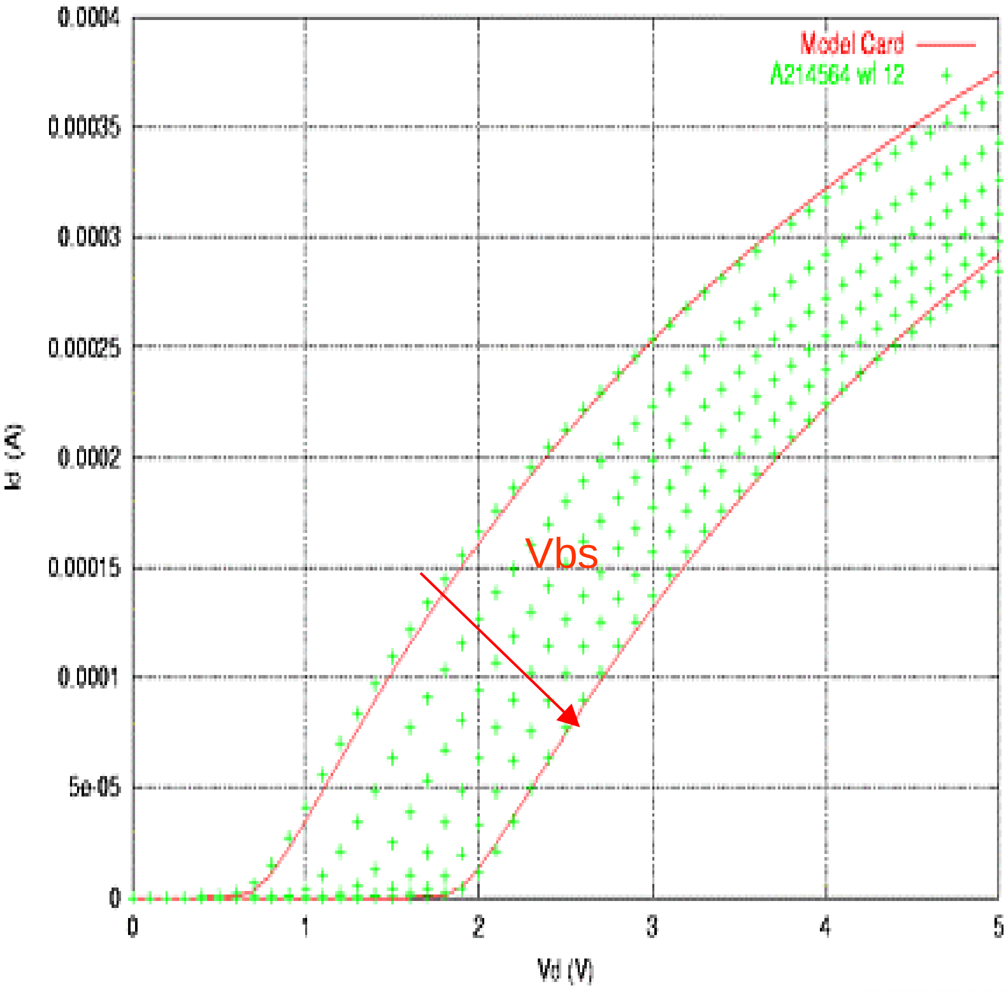
✓ For an ***accurate model card***

A good matching between the *model capability* in picturing the device experimental behavior and the *capability* to find out the best fit parameters.

‘Process alignment’ to model card

- **Comparison measurements – - model cards:**

Analytical measurements with parameters (e.g. Vbs)



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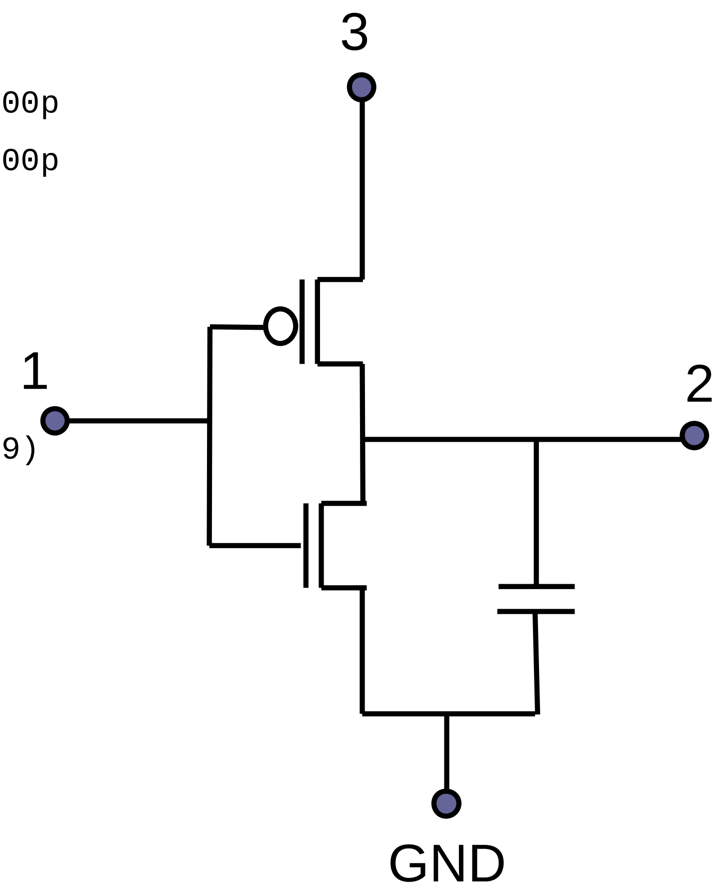
A MOS model card

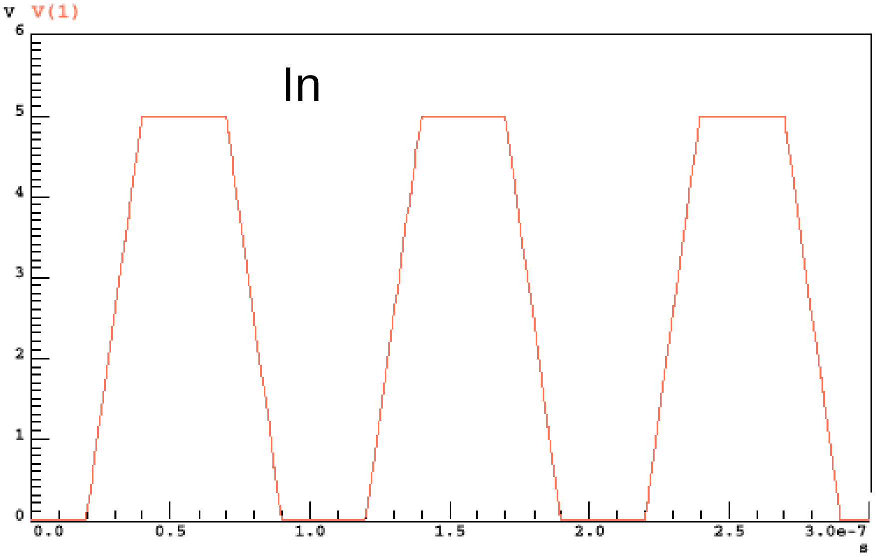
```
*{ENMM9_TYP} CMOST7X/CMOST7Y NLVLVS TYPICAL CURRENT
.MODEL ENMM9
+ NMOS  LEVEL = 59
+ TOX     = 9E-9           TR      = 27
+ LER     = 2.516084E-7    LVAR    = 0              LAP     = 4.419579E-7
+ WER     = 9.858698E-6    WVAR    = 4.748338E-8    WOT     = 7.065096E-8
+ VTOR    = 0.3803098      SLVTO   = 5.096637E-8    SL2VTO  = -9.97384E-15
+ SWVTO   = -1.170478E-8   STVTO   = -6.269264E-4   BETSQ   = 2.339437E-4
+ ETABET  = 1.8406012      THE1R   = 1.0359661      SLTHE1R = 1.860615E-7
+ FTHE1   = 2.6984018      WDOG    = 4.83065E-7     SWTHE1  = -2.539185E-8
+ STTHE1R = -2.847537E-3   STLTHE1 = -5.46098E-10   THE2R   = 0.1711789
+ SLTHE2R = 1.627924E-8    SWTHE2  = 3.503206E-8    STTHE2R = 1.070541E-5
+ STLTHE2 = 2.682545E-11   KOR     = 0.55997        SLKO    = -6.603552E-8
+ SWKO    = -5.51674E-8    KR      = 0.4855065      SLK     = -1.088468E-7
+ SWK     = -1.297093E-8   VSBXR   = 0.0442286      SLVSBX  = -2.115393E-6
+ SWVSBX  = -1.346183E-6   PHIBR   = 0.8228605      ZET1R   = 1.5802514
+ SLZET1  = -1.378976E-4   ETAZET  = 0.5            MOR     = 0.4965183
+ SLMO    = 3.23825E-5     STMO    = 8.330824E-5    ETAMR   = 0.34516
+ GAMOOR  = 0.0154123      SLGAMOO = 9.353718E-16   ETAGAMR = 2
+ VSBTR   = 100            SLVSBT  = 0              GAM1R   = 0.0273134
+ SLGAM1  = 7.062739E-9    SWGAM1  = 0              ETADSR  = 0.6
+ VPR     = 2.5114337      ALPR    = 6.881559E-3    SLALP   = 3.728809E-9
+ SWALP   = -2.980343E-9   ETAALP  = 1              THE3R   = 0.1842224
+ SLTHE3R = 5.50539E-8     SWTHE3  = -6.71814E-10   STTHE3R = -6.74519E-4
+ STLTHE3 = -1.51114E-10   A1R     = 99.2108051     SLA1    = -5.756254E-6
+ SWA1    = 1.727926E-5    STA1    = 0.1582689      A2R     = 28.7445013
+ SLA2    = -3.442762E-7   SWA2    = -2.632184E-6   A3R     = 0.6740045
+ SLA3    = -6.53344E-8    SWA3    = -1.351037E-7   IS      = 2.5E-15
+ ALEV    = 3              DCAPLEV = 0              DIOLEV  = 4
+ CJ      = 1.247914e-03   CJSW    = 1.814809e-10   CJGATE  = 2.264910e-10
+ MJ      = 0.409249       MJSW    = 0.354321       COL     = 1.15923E-10
+ CGBO    = 0              PB      = 0.90400        PBSW    = 0.90400
+ JS      = 4.968009e-07   JSW     = 1.3741806e-12  HDIF    = 0.4E-6
```

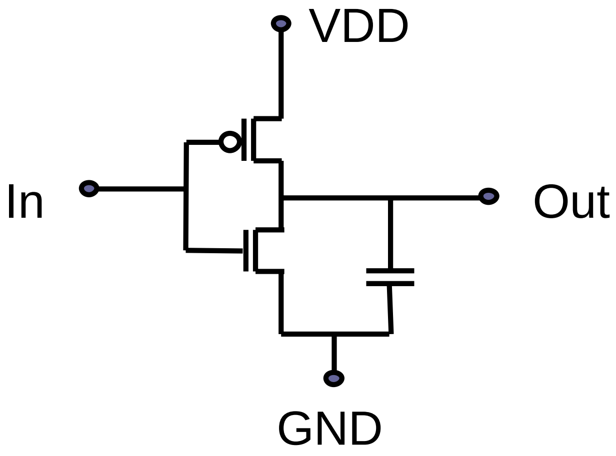
An example of circuitry simulation: CMOS inverter-1

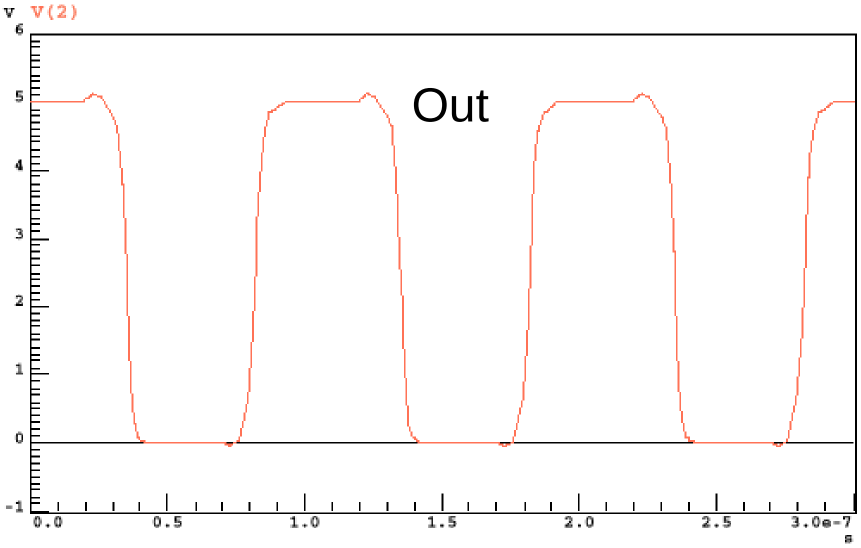
```
* Subcircuit definition
.subckt inv 1 2 3
m2 2 1 0 0 ENMM9 w=10u l=4u ad=100p pd=40u as=100p
m1 2 1 3 3 EPMM9 w=70u l=4u ad=100p pd=40u as=100p
c1 2 0 0.5p
.ends inv
* Electrical source definitions
vdd 6 0 5v
vin 1 0 pulse(0 5 20e-9 20e-9 20e-9 30e-9 100e-9)
* Simulation options & commands
.tran 0.5n 300n uic
.ic v(1)=0
.plot tran v(1) v(2)
.print tran v(1) v(2)
.option eps=0.5e-3 tnom=50 list node
.end
```



An example of circuitry simulation: CMOS inverter-2







CONCLUSIONS

- Electrical characterization of VLSI circuits, devices and technologies is a challenging task
- Component/Structure characterization is required for
  - technology development
  - Modeling => design
  - Process monitoring
- Not only devices but also ‘parasitics’ have to be measured since second and third order effects are growing importance due to active device scaling
- Specific characterization is required for certain applications: e.g. matching for analogue