Summer School in Information Engineering
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Video over wireless:

FPGA design and implementation of a pulse-based echo canceller for DVB-T/H

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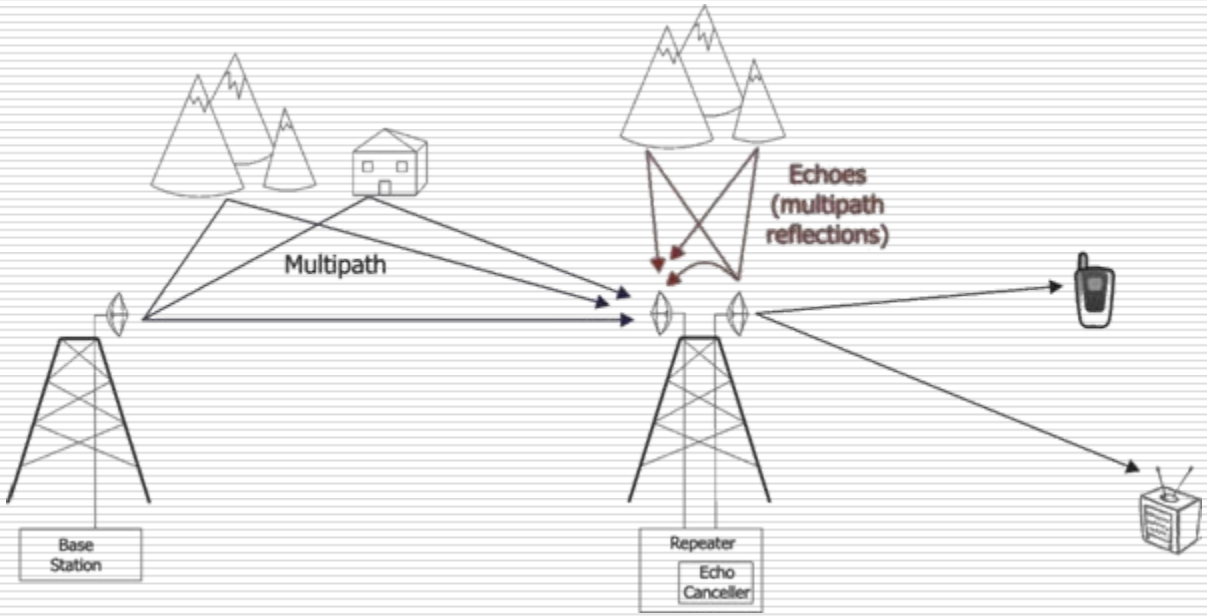
Outline

- Scenario description:
  - Problems and Goals
- Project Flow
- FPGA design and implementation:
  - FPGA development kit features
  - Test-bed implementation
  - Echo Canceller entity
- Measurements:
  - Comparison with theoretical results
  - Resources utilization
  - Matching with Simulation Results

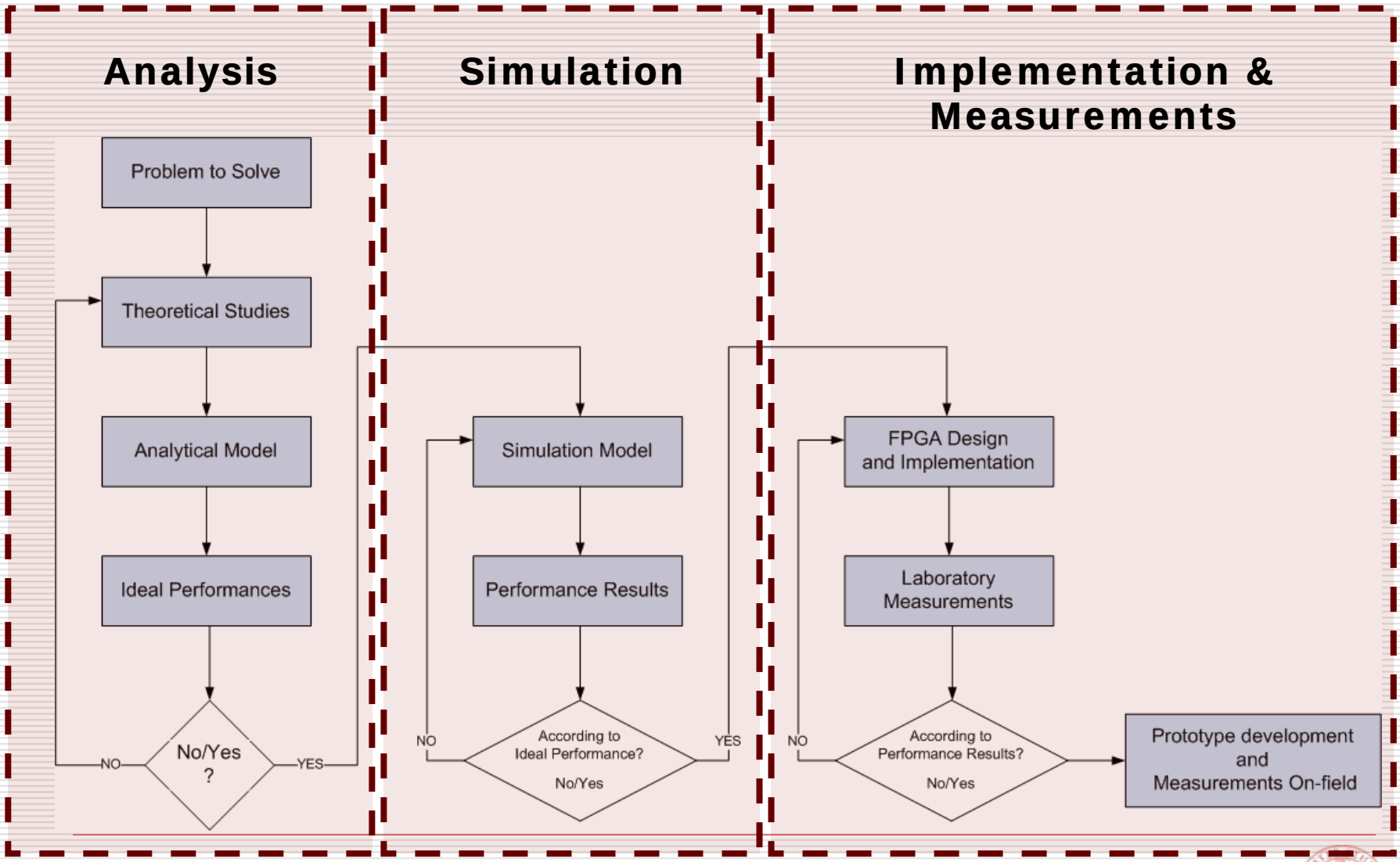
Scenario description: Problems and goals

- **Single Frequency Network (SFN)** constituted by:
  a. a DVB-T/H broadcasting station
  b. an on-channel relay station or repeater (OCR)
  c. many stationary and mobile users



- **Main goal**: covering with the DVB-T signal an area not reachable by the DVB-T broadcast station.

Project Flow



FPGA development kit features

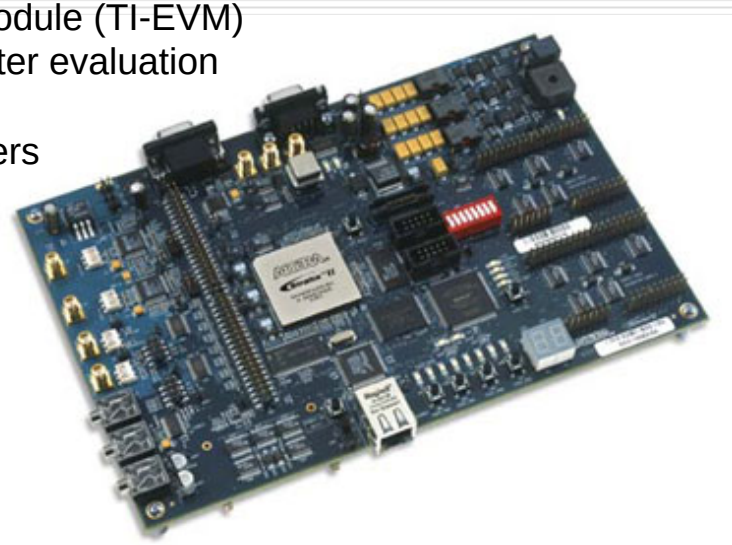
FPGA Stratix II Altera dev. Kit EP2S180F1020C3

Analog I/O:

- Two-channel, 12-bit, 125-million samples per second (MSPS) analog-to digital (A/D)
- Two-channel, 14-bit, 165-MSPS digital-to-analog (D/A)

Digital I/O

- Connector for the Texas Instruments (TI) Evaluation Module (TI-EVM)
- Two 40-pin connectors for Analog Devices' A/D converter evaluation boards
- Mictor connector for Agilent and Tektronix logic analyzers
- RS-232 serial port
- 10/100 Ethernet physical layer/media access control (PHY/MAC) and RJ-45 jack



Memory

- 32-Mbyte SDR SDRAM
- 16-Mbyte flash
- 1-Mbyte SRAM
- 16-Mbyte compact flash

FPGA design and implementation (1)

- **OCR Test-bed implemented on the FPGA board:**

- **BB-OCR Direct relay scheme:**

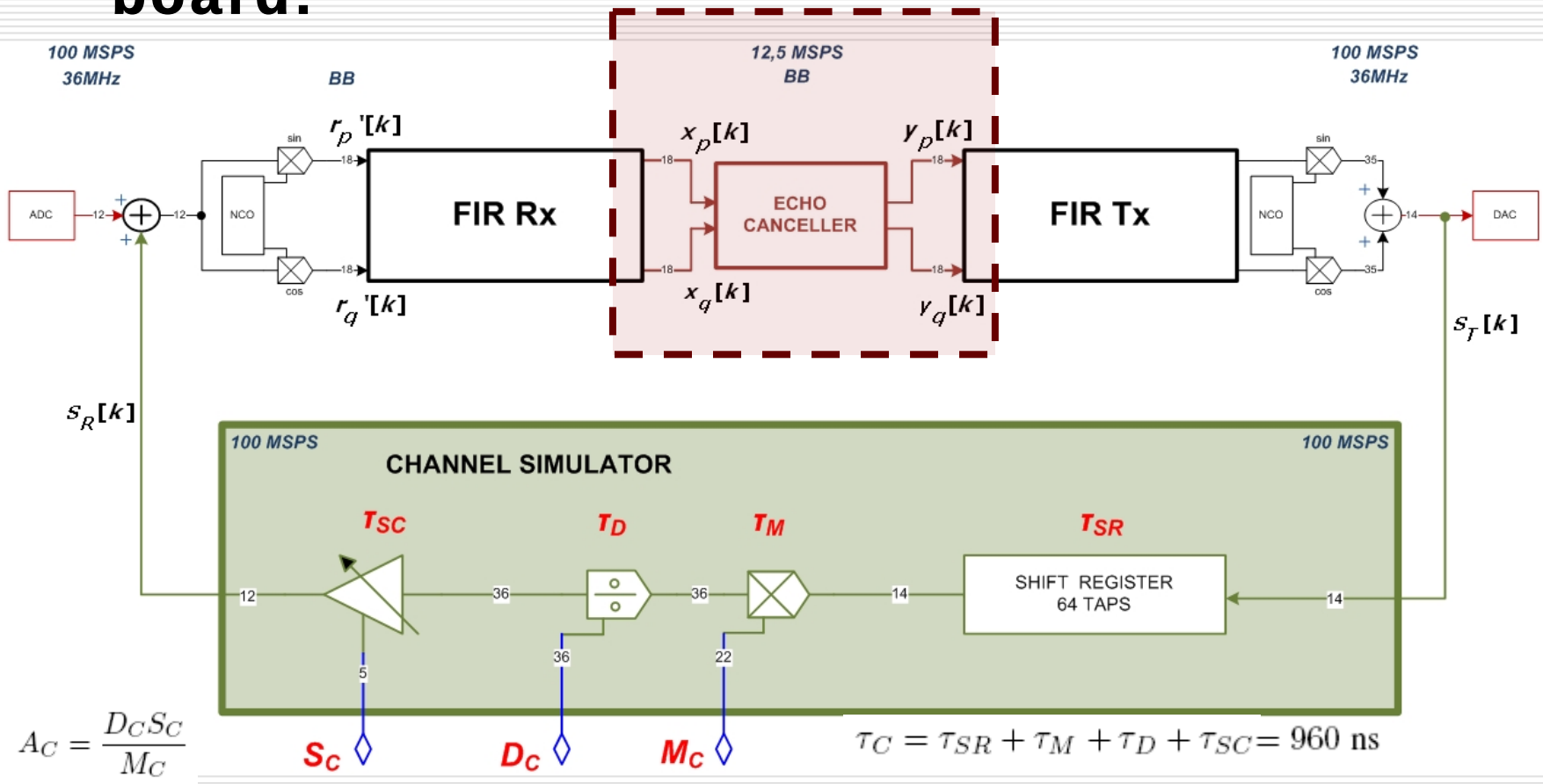
  Low delay techniques, based basically on:

  - **ESTIMATION** of the loop-back channel;
  - **(ADAPTIVE) FILTERING** to cancel the echoes;

	Antenna Isolation	Time Delay	Quality of Tx signal	Selectivity of Rx signal	Mantain Sync.
BB OCR	↓	↑	↑	↑	↑

FPGA design and implementation (2)

- **OCR Test-bed implemented on the FPGA board:**



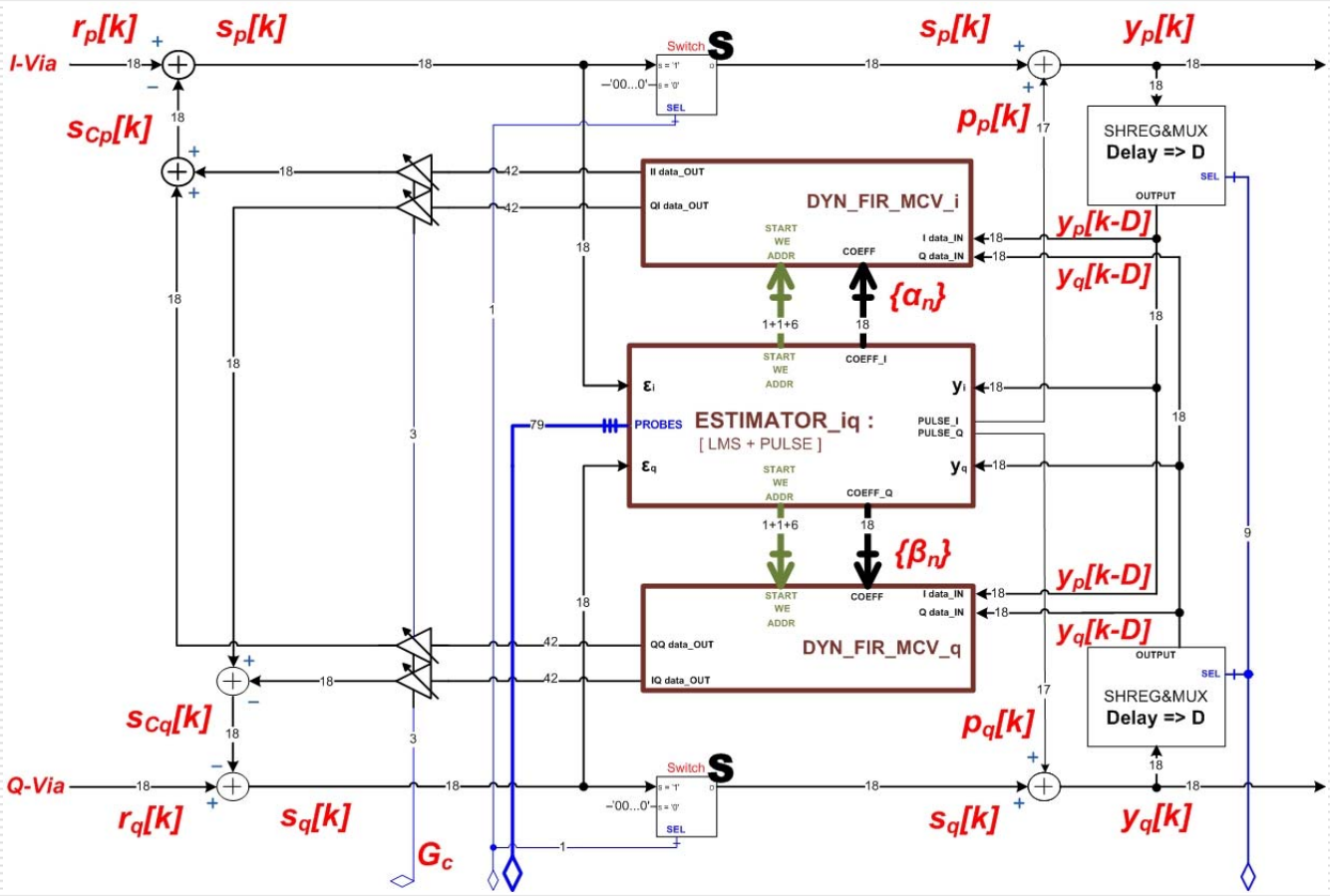
FPGA design and implementation (3)

- **The ECHO_CANCELLER entity:**

- Two operative phases:
  - **start-up**
    - determination of the number and position of the cancelling windows
    - initial coupling channel estimation
    - FIR's set-up
  - **steady state**
    - effective DVB-T signal repetition
    - (fast) echo tracking (LMS algorithm)
    - stability and coupling channel monitoring (periodical check of new echoes, etc.)

FPGA design and implementation (4)

- **The ECHO_CANCELLER entity:**



ESTIMATOR_iq:

implementing the channel pulse estimator, the pulse generator and an additional Least Mean Square (LMS) algorithm working in the *steady-state mode*;

SHREG&MUX:

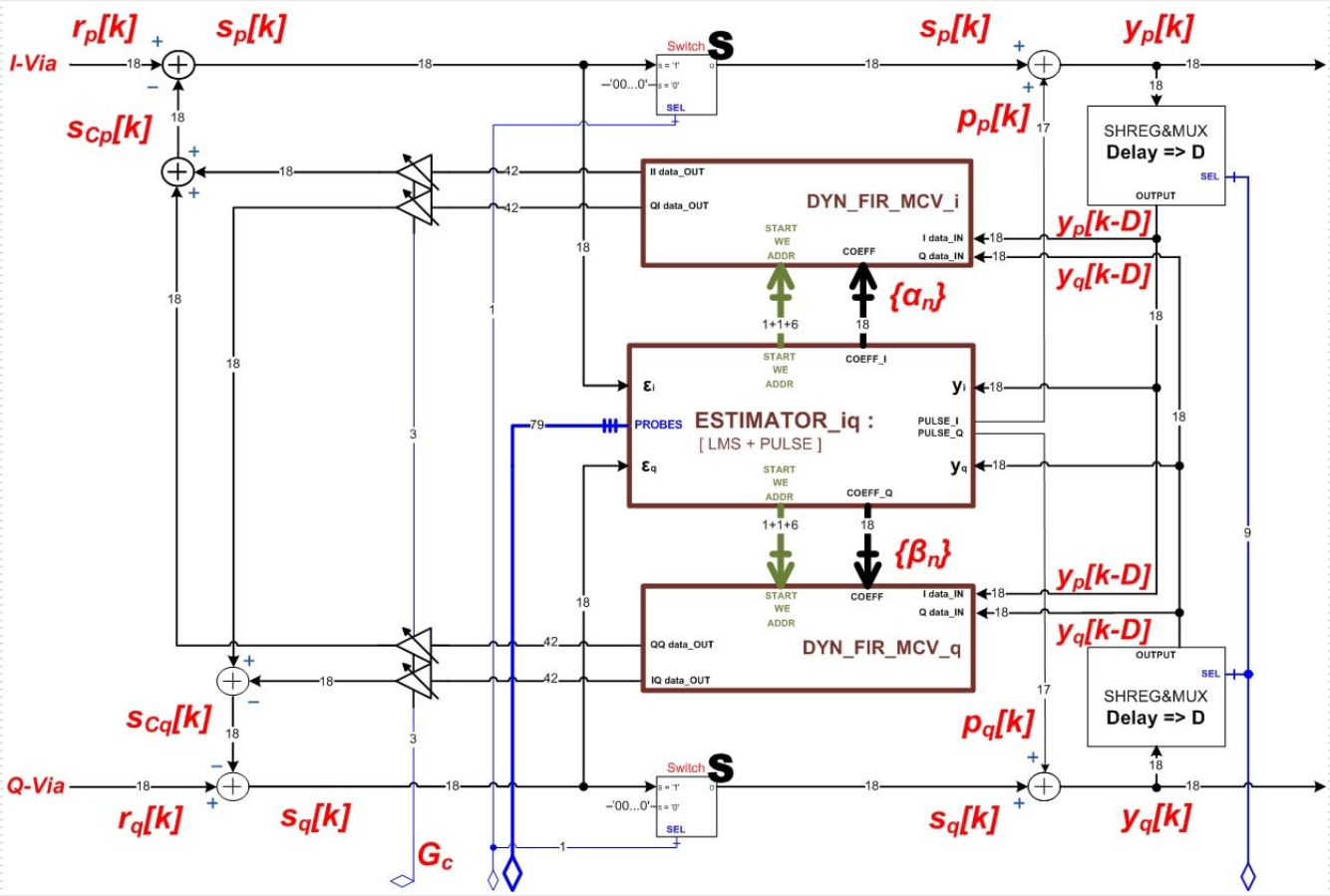
implementing the delay which allows to position the cancelling window inside the overall search window;

DYN_FIR_MCV:

implementing the cancelling FIR filters with dynamically variable coefficients, based on the Multi Cycle Variable (MCV) technology.

FPGA design and implementation (5)

The ECHO_CANCELLER entity:

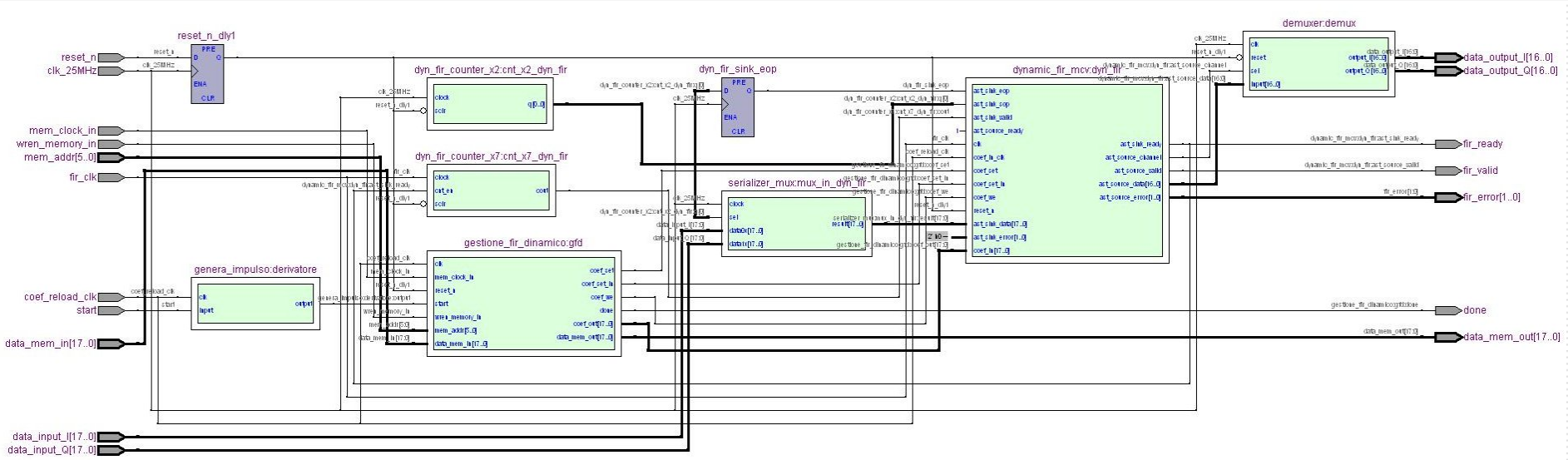


Input-data 18bit;
Output-data 18bit;
Control sig = #15+:

- **ACCP**: # pulse accumulations;
- **SMPL**: # samples;
- **AMPi**: pulse amplitude (I-via);
- **AMPq**: pulse amplitude (Q-via);
- **TIME**: pulse train period;
- **ACCL**: # LMS accumulations;
- **LAMB**: LMS scaling factor;
- **LPRN**: dynamic FIR uploading modality
- **MUX1**: selector of the first cancellation window;
- **MUXn**: selector of the n-th cancellation window;
- **INTR**: circuit switch.

FPGA design: **ECHO_CANCELLER** (1)

- **DYN_FIR_MCV** : the FIR cancelling unit



FPGA design: **ECHO_CANCELLER** (2)

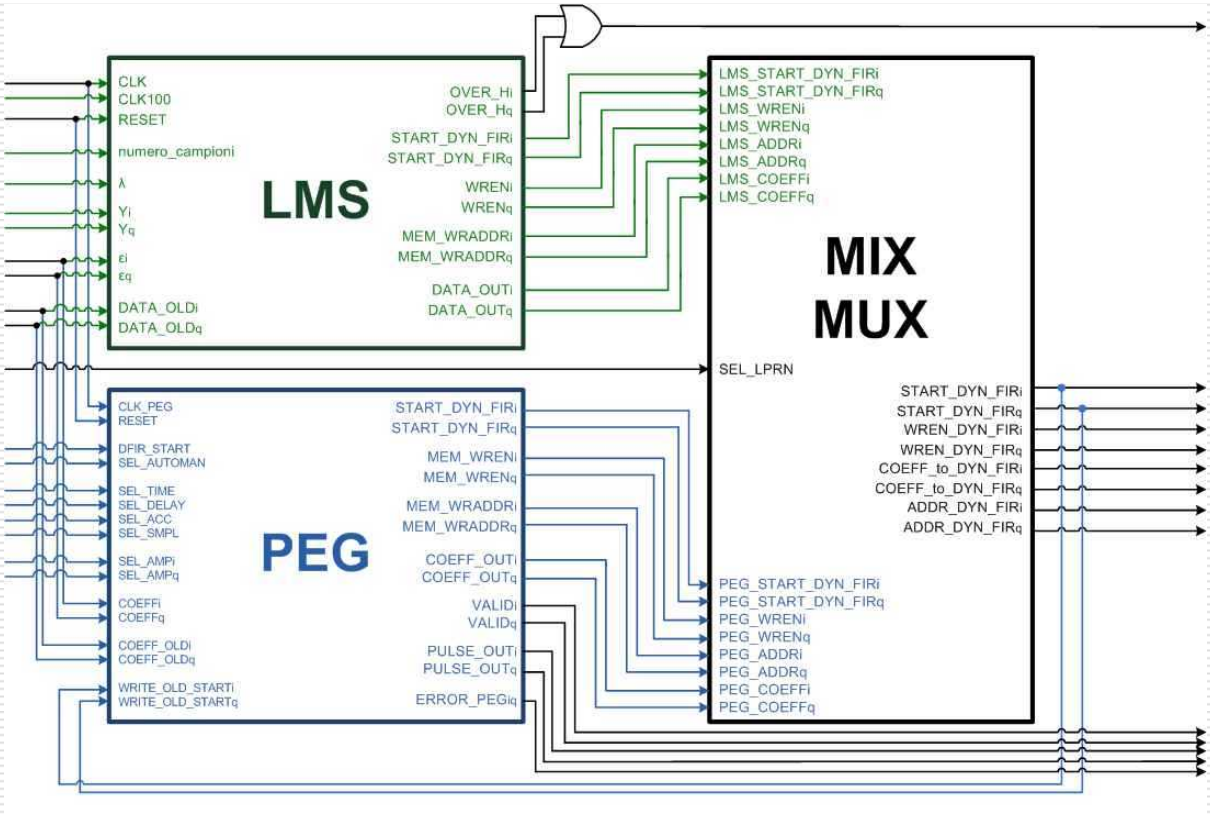
- **DYN_FIR_MCV** : the FIR cancelling unit

PARAMETERS	SET-UP VALUES
Coefficients scaling	Auto with Power 2
Bit Width	18
Device Family	Stratix II
Structure	Variable/Fixed Coefficient: Multi-Cycle
Pipeline Level	1
Data Storage	Logic cells
Coefficient Storage	Memory, M4K
Coefficients Reload	Enabled
Single Clock	Disabled
Force Non-Symmetric Structure	Enabled
Coefficents setsnumber	2
Rate Specification	Single Rate
Add global clock enable pin	Disabled
Number of input channels	2
Input number system	Signed binary
Input Bit Width	18
Output specification: Based on Method	Bit Width Only
Output number system:	Custom Resolution
Bits to keep	9-17-16
MSB	Saturate
LSB	Truncate
Clocks to compute	7
Multiplier Implementation	DSP Blocks
Coefficients	56

7*25MHz = 175 MHz

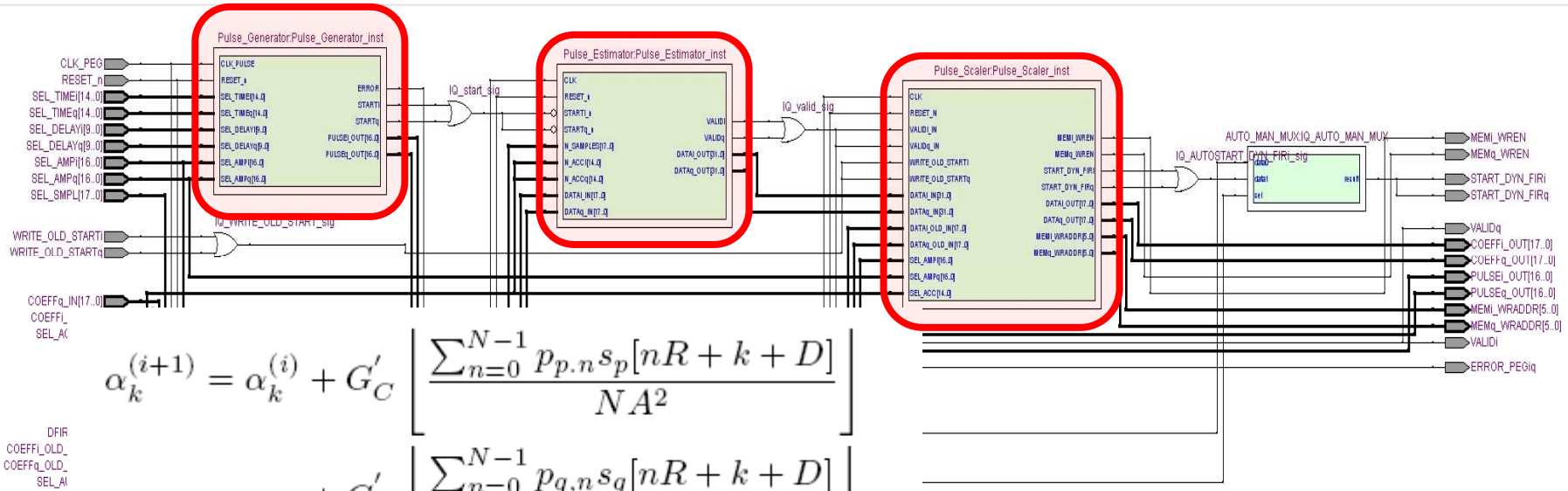
FPGA design: **ECHO_CANCELLER** (3)

- **ESTIMATOR_iq** : the estimator of the feedback channel coefficients



FPGA design: **ECHO_CANCELLER/ESTIMATOR_iq** (1)

- **PEG** : the pulse generator and estimator unit



$$\alpha_k^{(i+1)} = \alpha_k^{(i)} + G_C' \left\lfloor \frac{\sum_{n=0}^{N-1} p_{p.n} s_p[nR+k+D]}{NA^2} \right\rfloor + G_C' \left\lfloor \frac{\sum_{n=0}^{N-1} p_{q,n} s_q[nR+k+D]}{NA^2} \right\rfloor$$

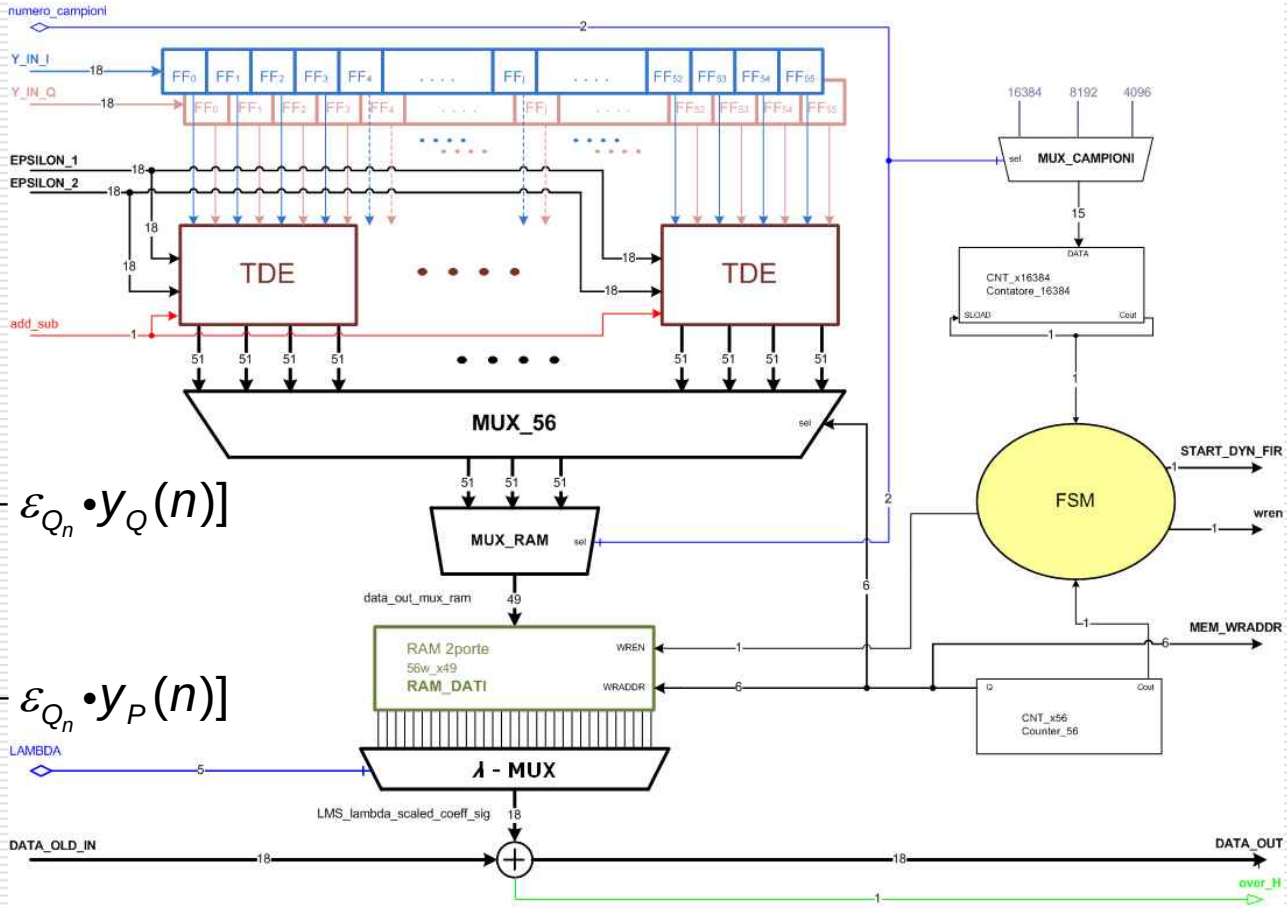
$$\beta_k^{(i+1)} = \beta_k^{(i)} + G_C' \left\lfloor \frac{\sum_{n=0}^{N-1} p_{q,n} s_p[nR+k+D]}{NA^2} \right\rfloor - G_C' \left\lfloor \frac{\sum_{n=0}^{N-1} p_{p.n} s_q[nR+k+D]}{NA^2} \right\rfloor$$

FPGA design: **ECHO_CANCELLER/ESTIMATOR_iq** (2)

- **LMS** : the Least Mean Square estimator unit

$$\underline{h}_P(m+1) =$$
$$= \underline{h}_P(m) + \lambda \bullet \mathrm{E}[\varepsilon_{P_n} \bullet y_P(n) + \varepsilon_{Q_n} \bullet y_Q(n)]$$

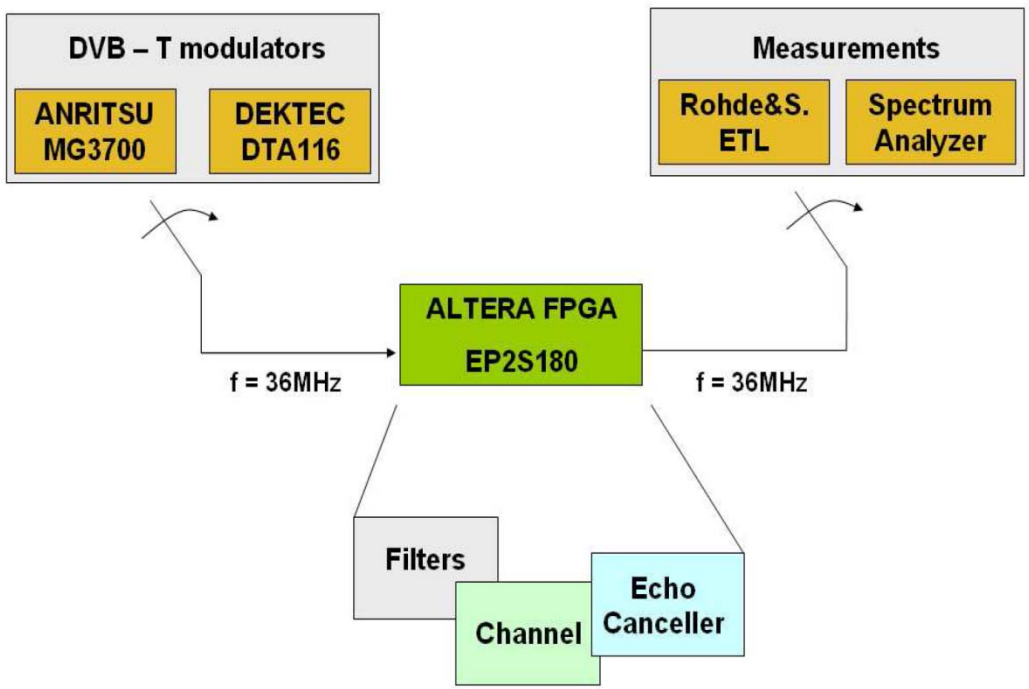
$$\underline{h}_Q(m+1) =$$
$$= \underline{h}_Q(m) + \lambda \bullet \mathrm{E}[\varepsilon_{P_n} \bullet y_Q(n) - \varepsilon_{Q_n} \bullet y_P(n)]$$



Measurements:

Workbench configuration:

conceptual scheme realized to test the echo canceller



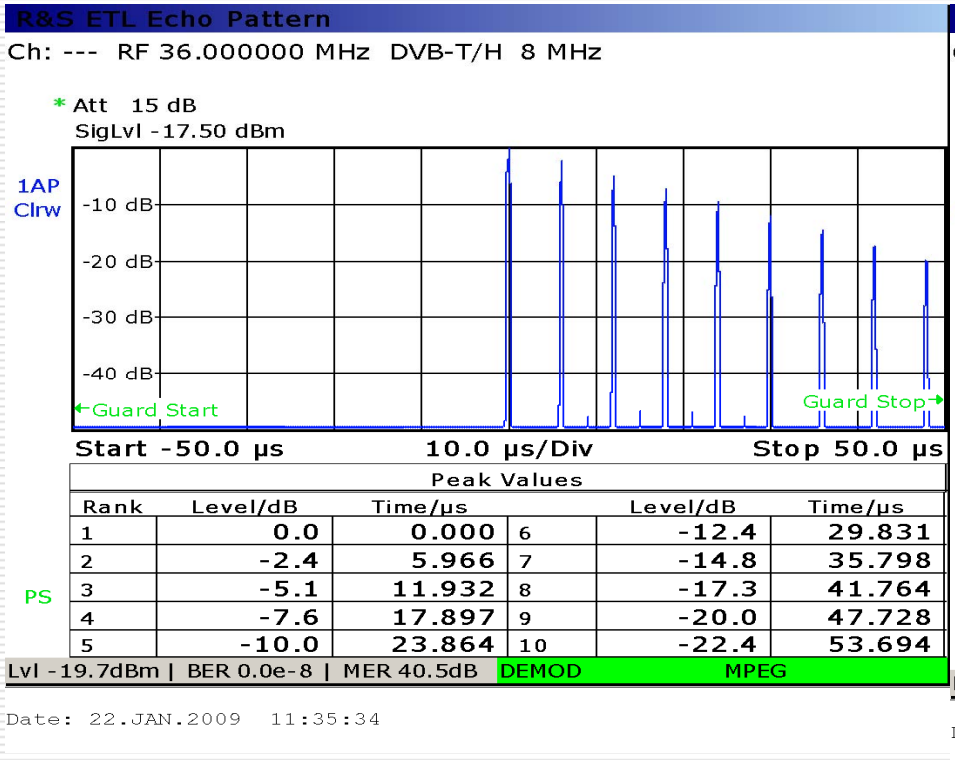
- DVB-T Modulators:

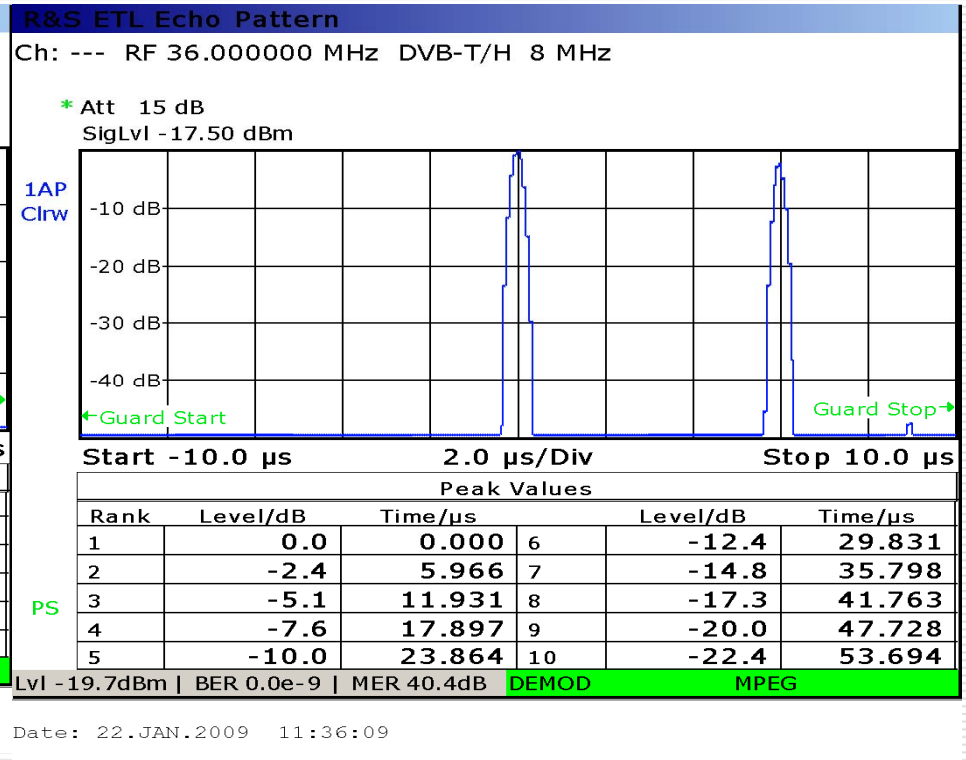
	MG3700	*DTA116*
Power Lvl	−40 dBm : 10 dBm	−14 dBm
Freq. Range	250 KHz : 3 Ghz	36 MHz
MER	44 dB	41 dB

- Digital Oscilloscope
- Spectrum Analyzer
- Network Analyzer
- TV - Analyzer

Measurements: (echo canceller off)

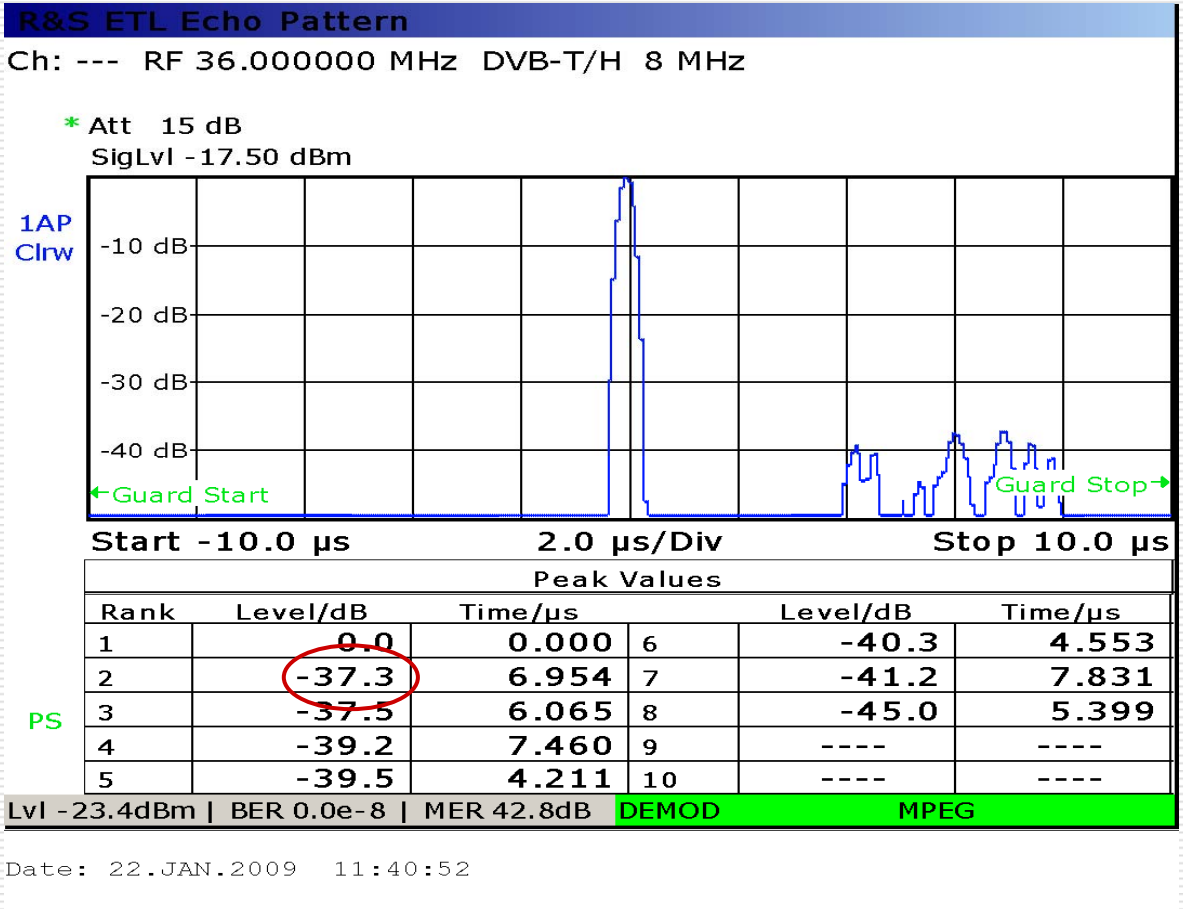
- Measured impulse response of the channel between the modulator and the demodulator.





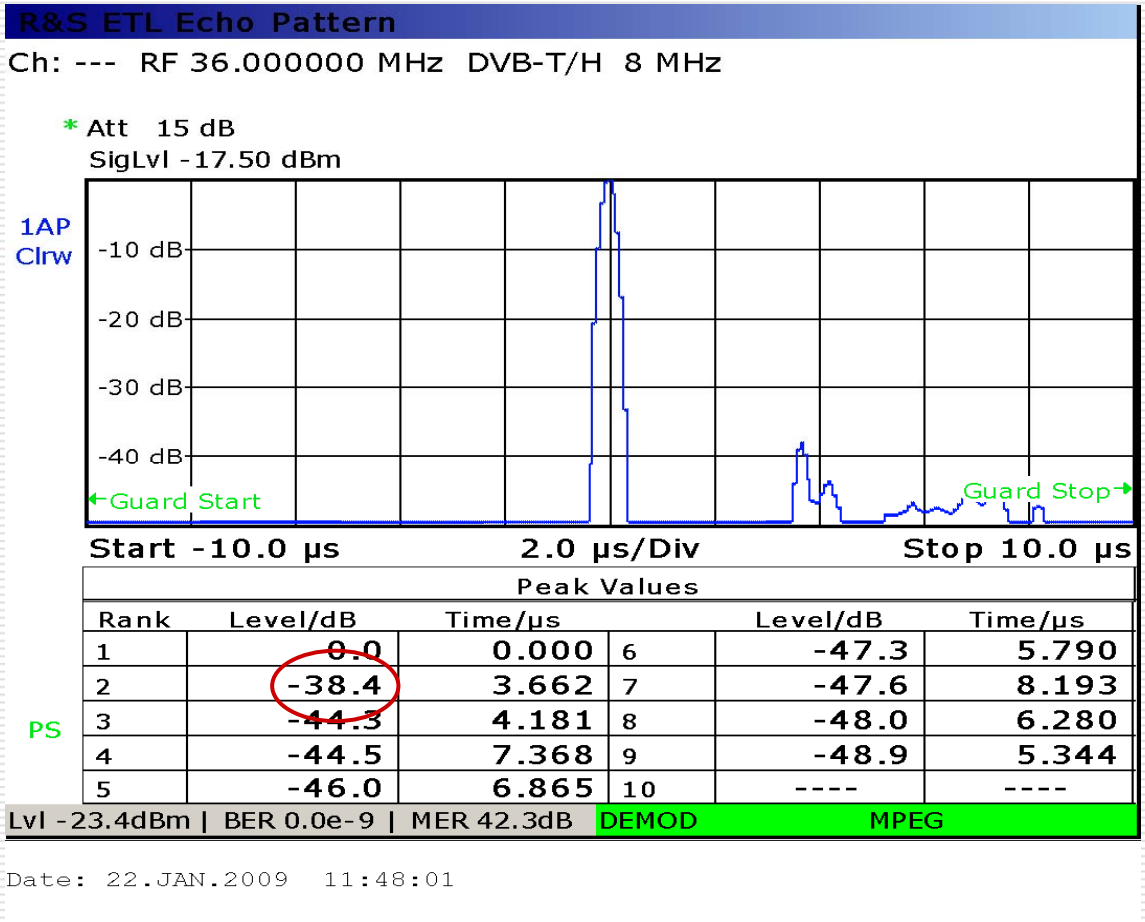
Measurements: (start-up mode)

- Echo suppression when the echo level is ***0.2dB*** *lower* than the input DVB-T signal



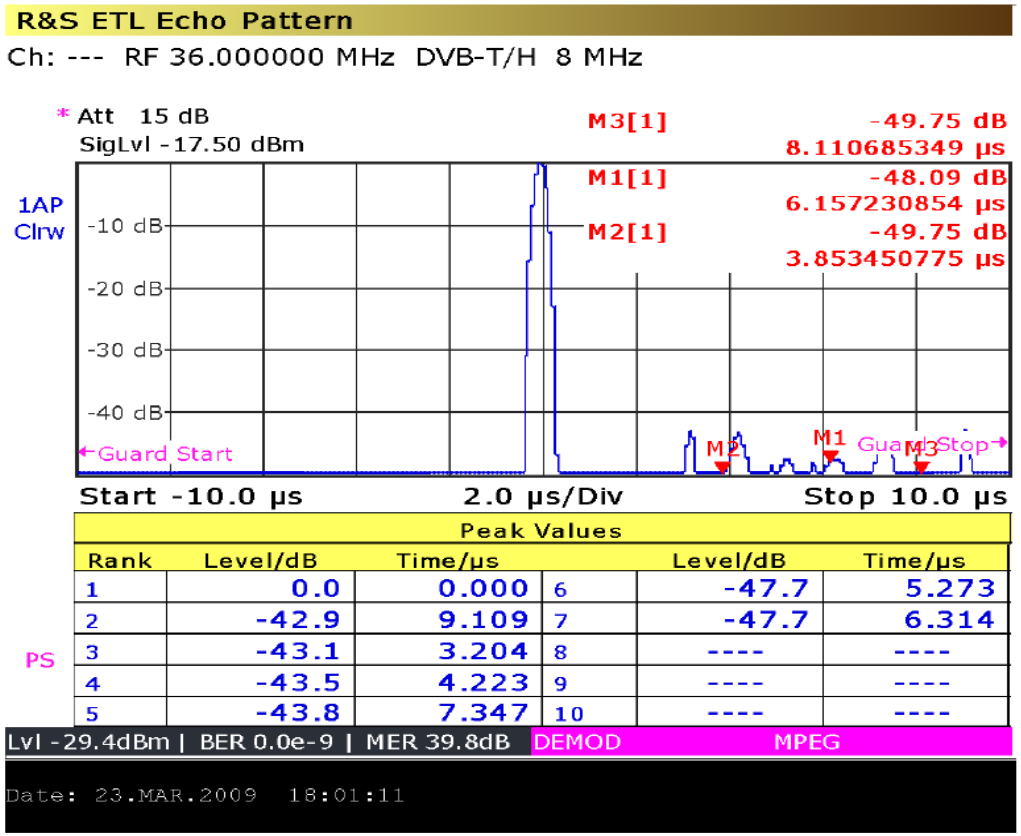
Measurements: (steady-state mode)

- Echo suppression when the echo level is ***0.2dB*** *lower* than the input DVB-T signal



Measurements: (complete procedure)

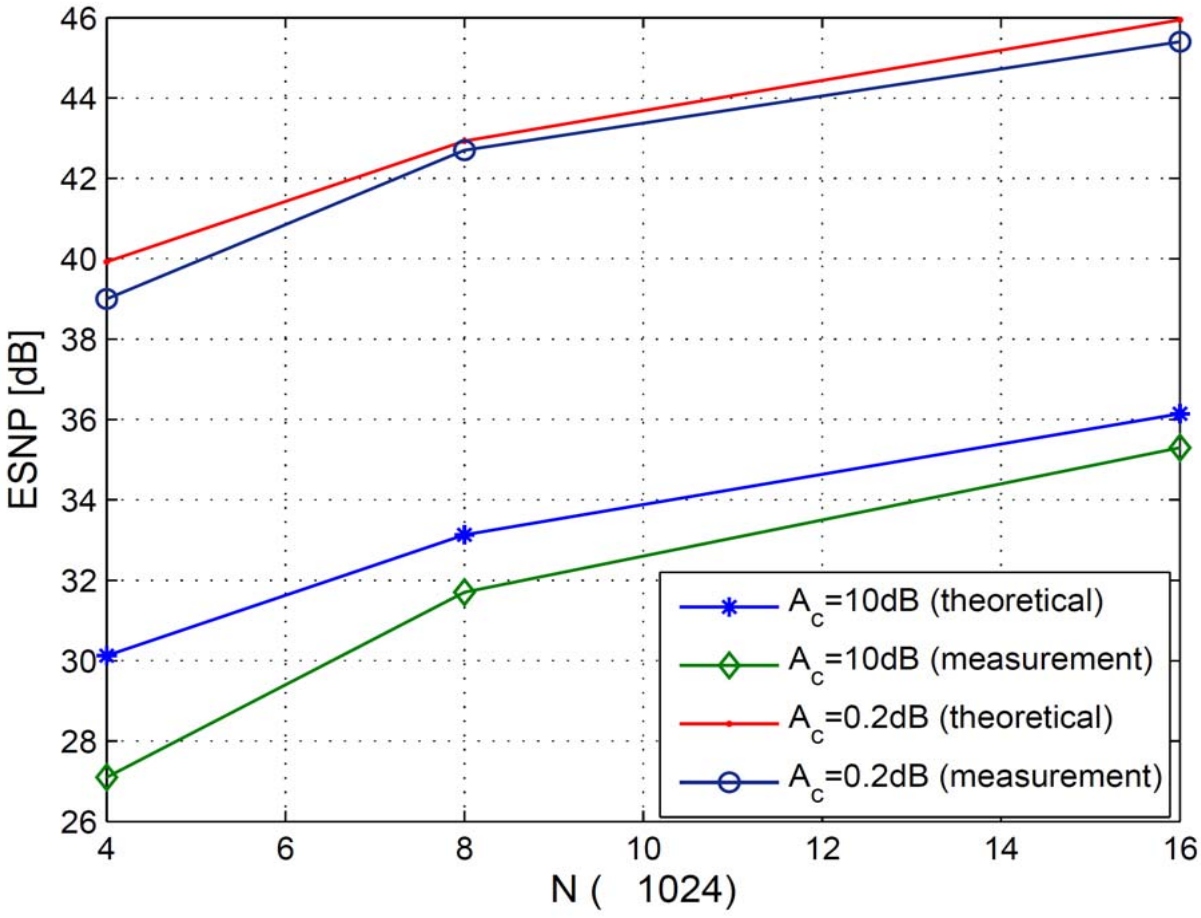
- Echo suppression when the echo level is ***10dB*** *higher* than the input DVB-T signal



FPGA Resources Utilization

Flow Status	Successful - Wed May 06 17:24:14 2009
Quartus II Version	8.0 Build 231 07/10/2008 SP 1 SJ Full Version
Revision Name	Testbed_EC_200
Top-level Entity Name	Testbed_EC_2_00
Family	Stratix II
Device	EP2S180F1020C3
Timing Models	Final
Met timing requirements	N/A
Logic utilization	35 %
Combinational ALUTs	34,791 / 143,520 (24 %)
Dedicated logic registers	33,243 / 143,520 (23 %)
Total registers	33380
Total pins	137 / 743 (18 %)
Total virtual pins	0
Total block memory bits	1,632,205 / 9,383,040 (17 %)
DSP block 9-bit elements	216 / 768 (28 %)
Total PLLs	2 / 12 (17 %)
Total DLLs	0 / 2 (0 %)

Measurements vs. Simulation Results



ESNP = Echo Suppression at Nominal Position

$$\mathrm{ESNP} \triangleq \frac{\mathbb{E}\left\{|s_0(\tau^*)|^2\right\}}{\mathbb{E}\left\{|s_1(\tau^*)|^2\right\}}$$

It is an over-estimation of the actual Echo Suppression

Thank you !

For more information
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