

**Summer School in Information Engineering
Brixen, June 29th – July 3rd, 2009**

**Video over wireless
Multistage Filters: design, implementation and
measurements for DVB-T systems**

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Overview

- WiLab – Wireless Communication Laboratory
- Main research goals: FIR filters and their performance
- Multistage architecture! What? Why? How?
- Numerical results
- Measurement examples on network analyzer

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www.wilab.org

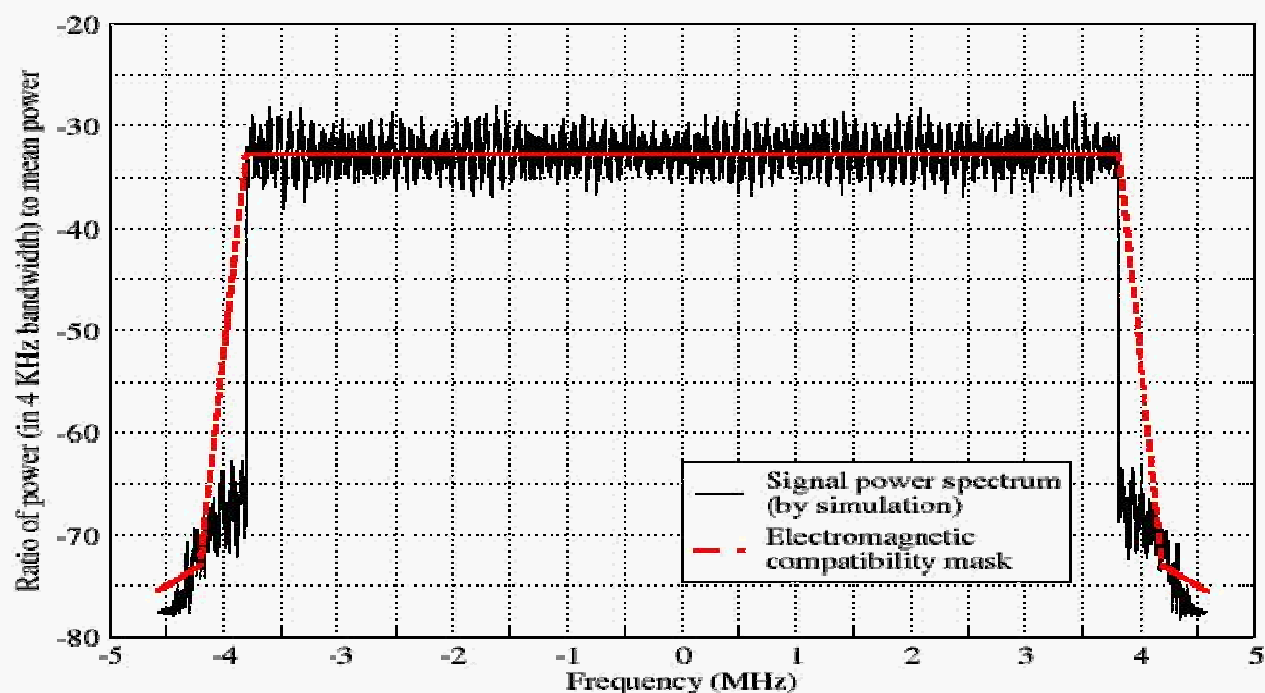


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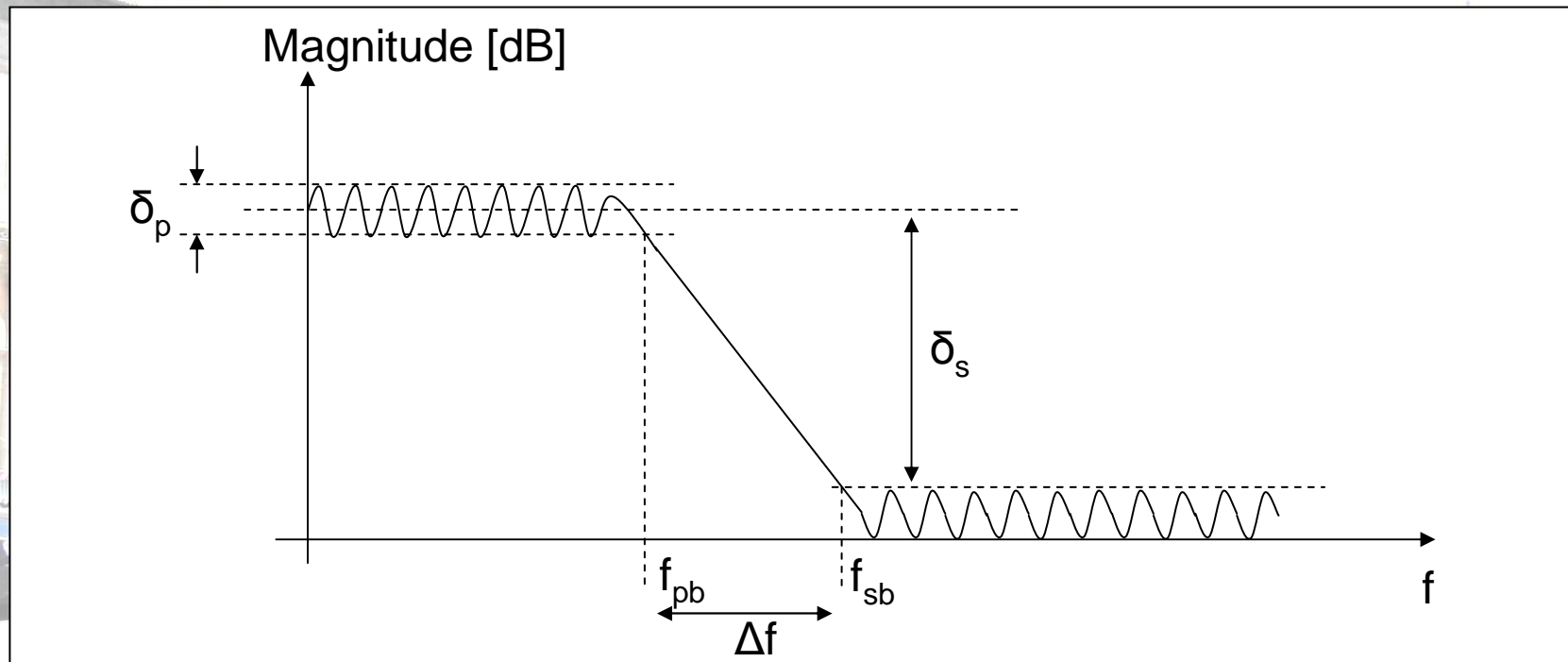
Main research goals

Finite Impulse Response (FIR) for DVB-T/H modulators and repeaters:



Project and design: How? What designer need?

Amplitude characteristic:

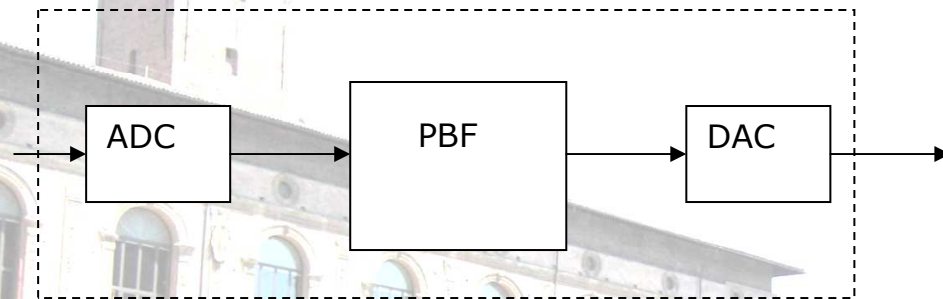


Group Delay [GD] performance is not clearly always reported on requirements plain!

Related to DVB-T system, designer has to consider it

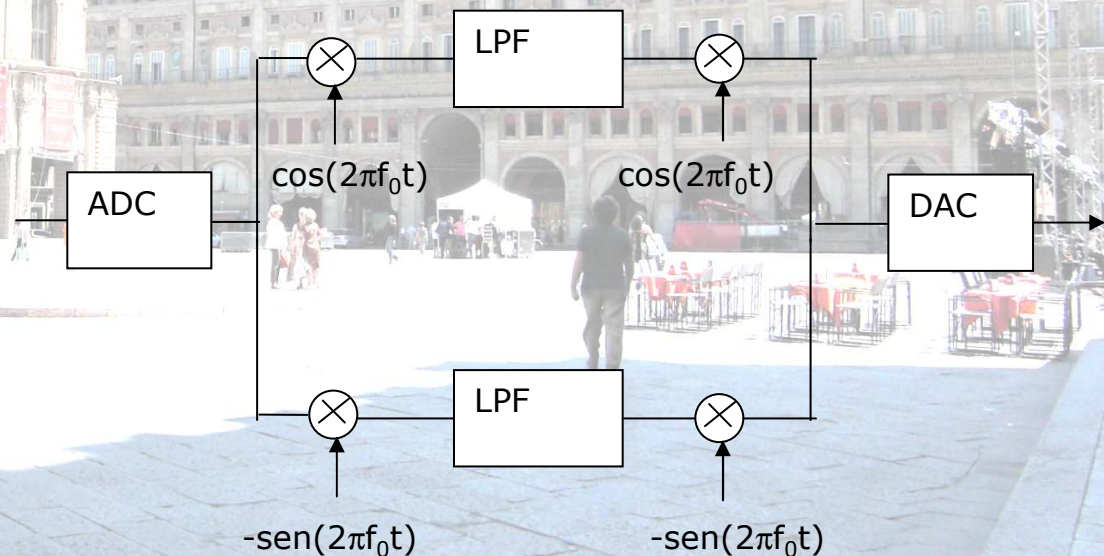
→ strong constraint!

Pass band signal: possible filtering architecture



Band Pass Solution

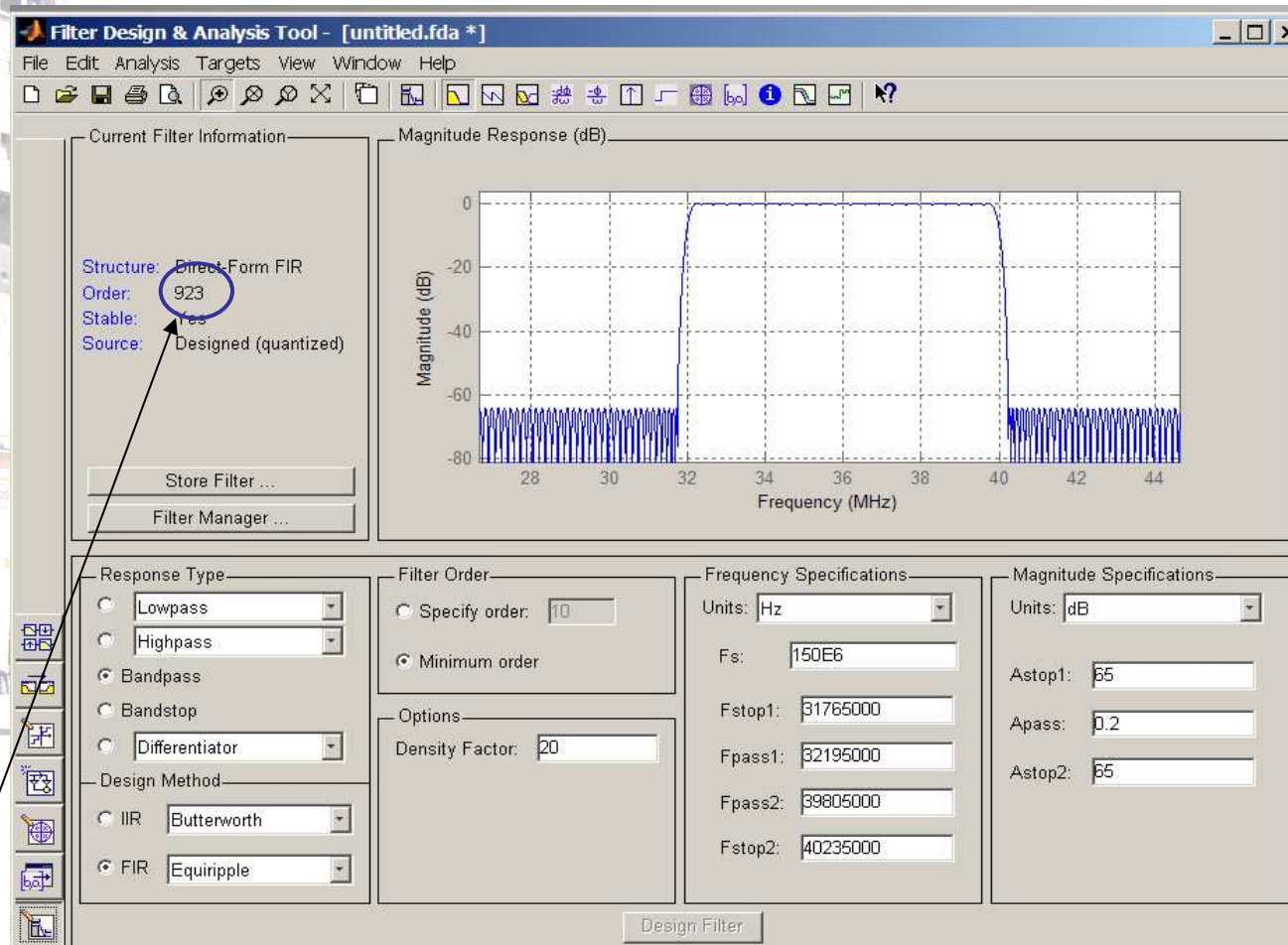
Low Pass Solution



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Pass Band Solution



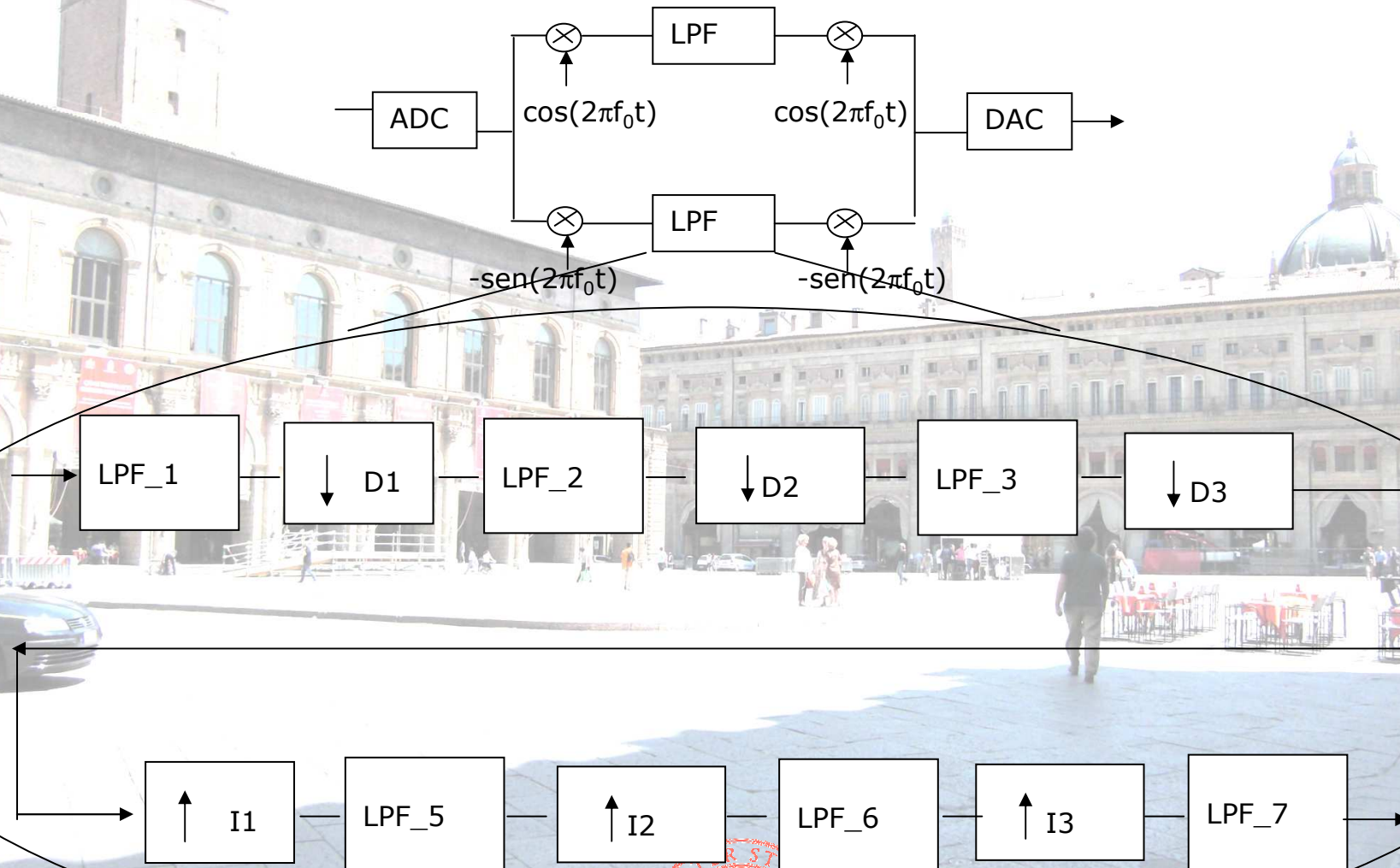
924 taps + Interpolator filter (move from $f_s=150\text{Ms/s}$ to $f_s=300\text{Ms/s}$)



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Multi-stage filters: classic architecture

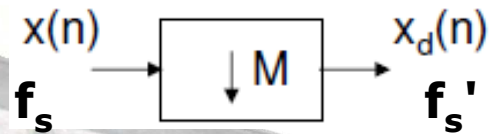


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Decimation basics

Downsampler

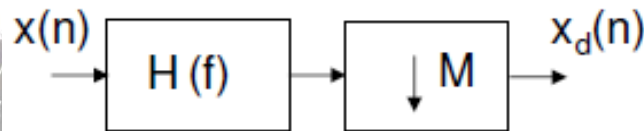


$$f'_s = f_s / M$$



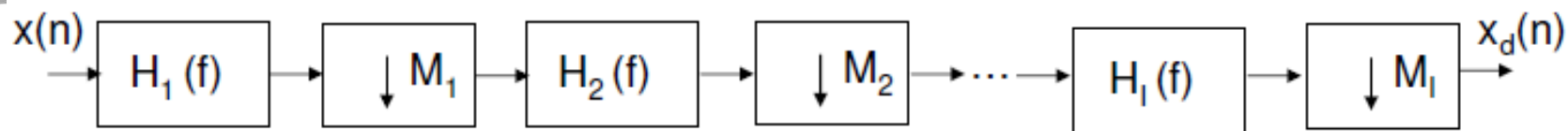
Problem: Periodic spectral repetition closer than $x(n)$

Decimator



Solution: A FIR filter before to avoid aliasing!

Multistage Decimator

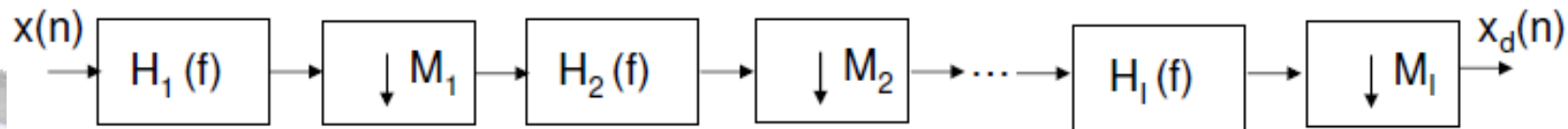


$$M = M_1 M_2 \dots M_I$$

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Multistage filters



This chain permits to minimize number of taps (and then the area occupied on board) for strong requirements, but...

GROUP DELAY IS COMPLETELY FORGOTTEN!!

I: # di stadi ↑

N: # di prese ↓

Group Delay ↑

$$\tau_g = \frac{1}{f_s} \sum_{i=1}^I \frac{N_i - 1}{2} \prod_{k=1}^i M_{k-1}$$

Group Delay formula

$$N \cong \frac{-20 \log_{10}[\sqrt{\delta_p \delta_s}] - 13}{14.6 \Delta f} f_s + 1$$

Number of Taps (REMEZ approximation)

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Decimation factor: which is the right order?

$$M = M_1 M_2 \cdots M_I$$

We derive this formula to analyze which is the right order for decimation factor:

$$\begin{aligned}\hat{\tau}_g &\cong A(I) \left[\sum_{i=1}^{I-1} \frac{1}{\frac{f_{s_i}}{M_i} - F} + \frac{1}{\Delta f} \right] \\ &\cong \frac{A(I)}{\Delta f} + \frac{A(I)}{\frac{f_s}{M_1} - F} + \frac{A(I)}{\frac{f_s}{M_1 M_2} - F} + \cdots + \frac{A(I)}{\frac{f_s}{M_1 M_2 \cdots M_{I-1}} - F}\end{aligned}$$

Group Delay Minimization Criteria:

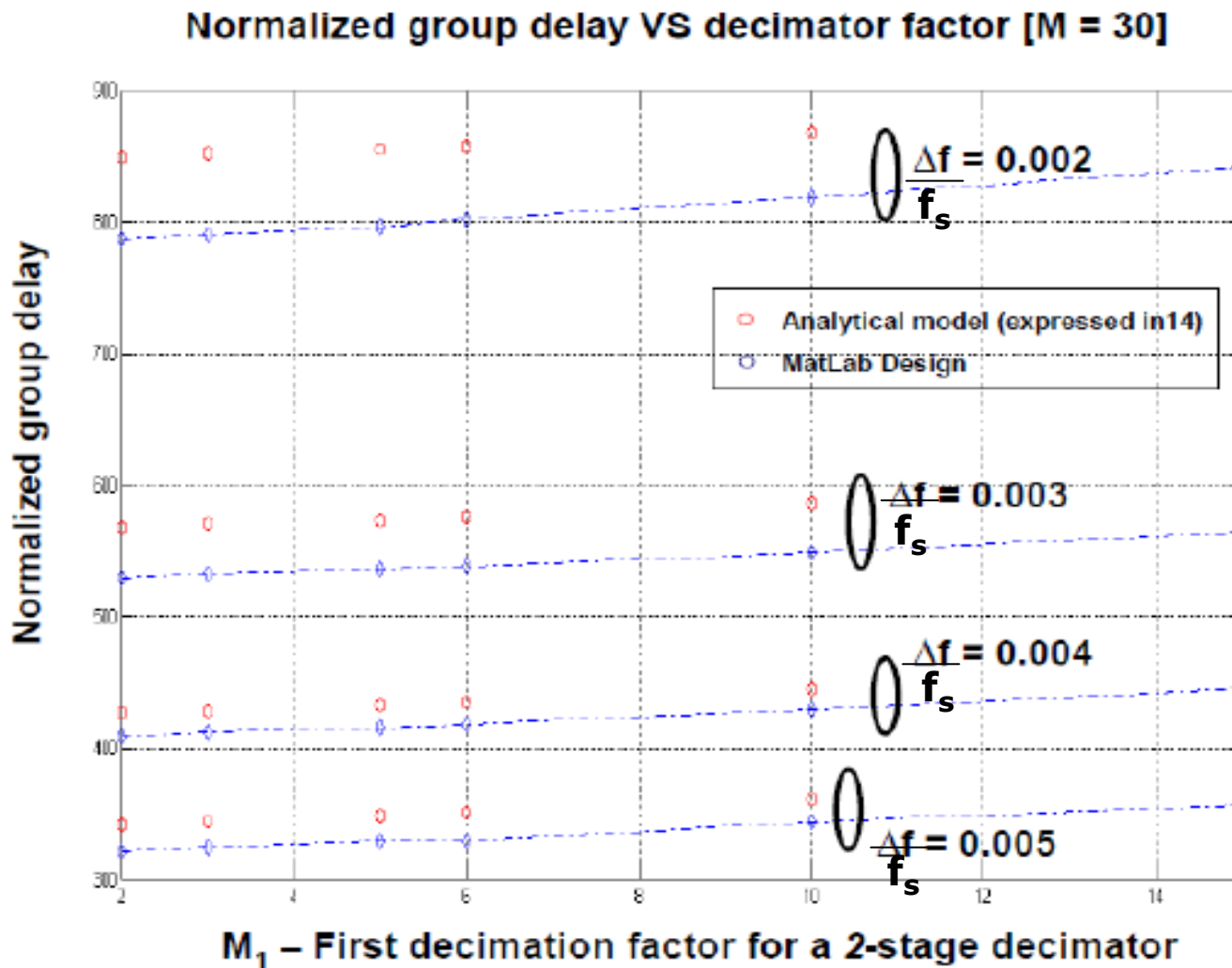
$$M_1^{(min)} \leq M_2^{(min)} \leq \dots \leq M_{I-1}^{(min)} \leq M_I^{(max)}$$

$$M_I = \frac{M}{\prod_{i=1}^{I-1} M_i^{(min)}} = M_I^{(max)}$$

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Normalized Group Delay vs. First Decimation Factor



Normalized Group Delay vs. First and Second Decimation Factor

Decimation Factor $M = 36$

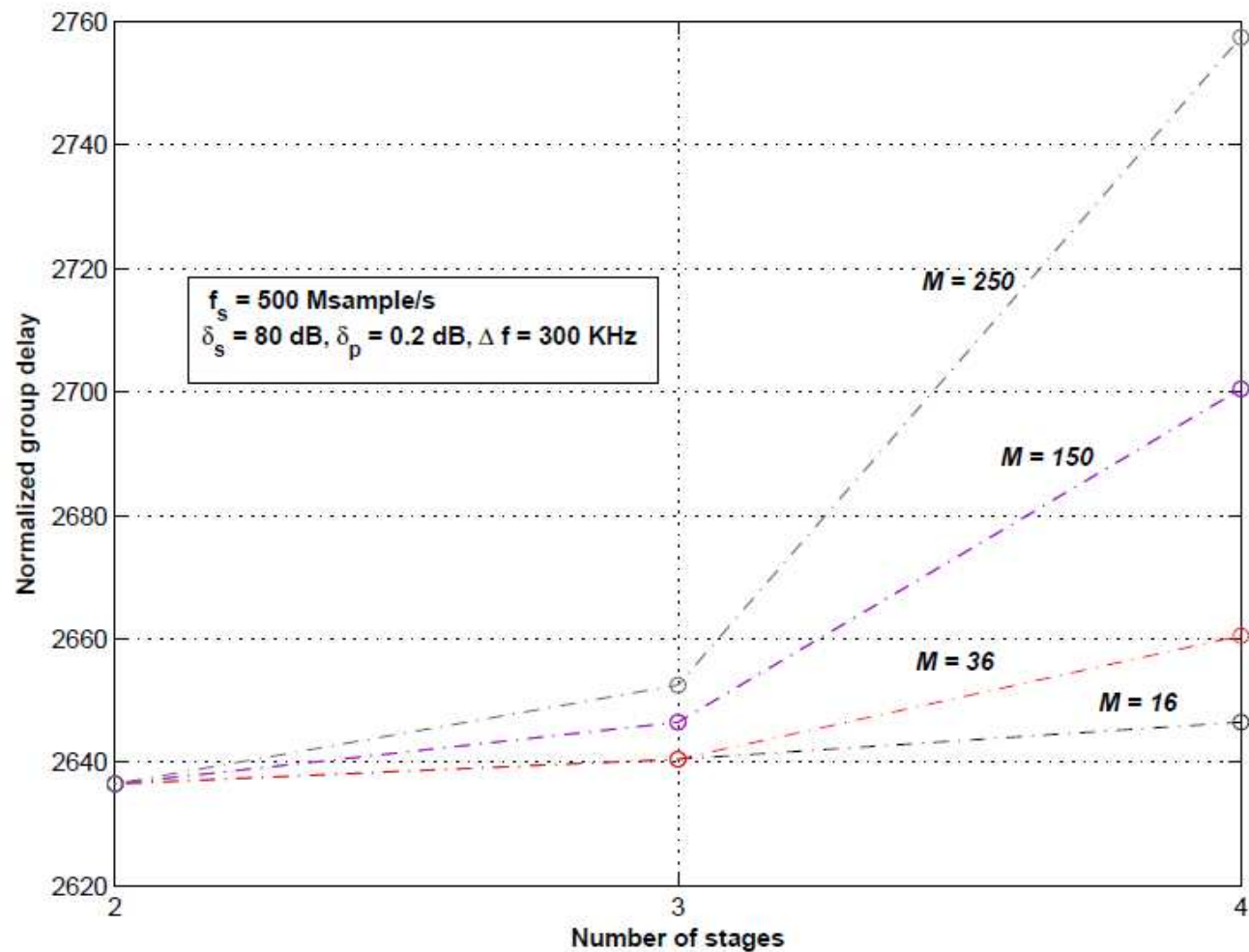
Number of stage I = 3

M_2	M_1								
	1	2	3	4	5	6	7	8	9
1	■	■	■	■	■	■	■	■	■
2	■	458.5	465.5	■	■	482.5	■	■	494.5
3	■	464.0	474.5	483.5	■	495.5	■	■	■
4	■	■	485.0	■	■	■	■	■	■
5	■	■	■	■	■	■	■	■	■
6	■	485.5	500.5	■	■	■	■	■	■
7	■	■	■	■	■	■	■	■	■
8	■	■	■	■	■	■	■	■	■
9	■	503.5	■	■	■	■	■	■	■

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Group Delay vs. Number of stage



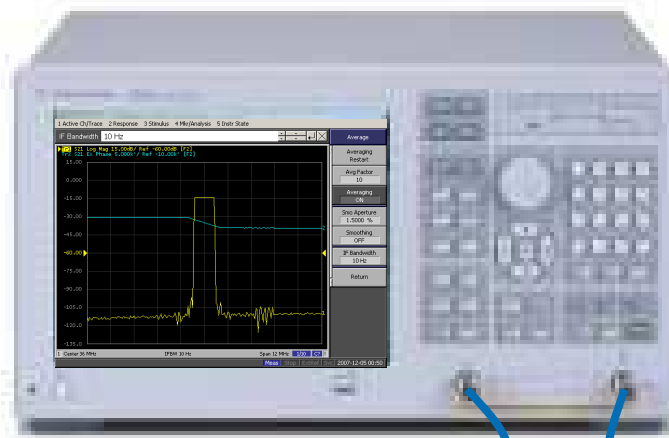
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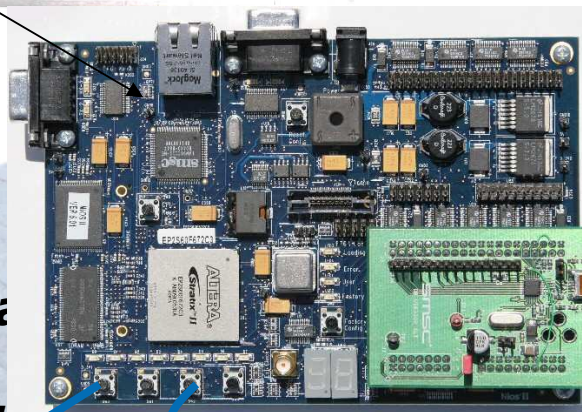
IF Filtering: characterization through network analyzer

Network Analyzer

ENA - Agilent



FPGA - Altera Stratix II

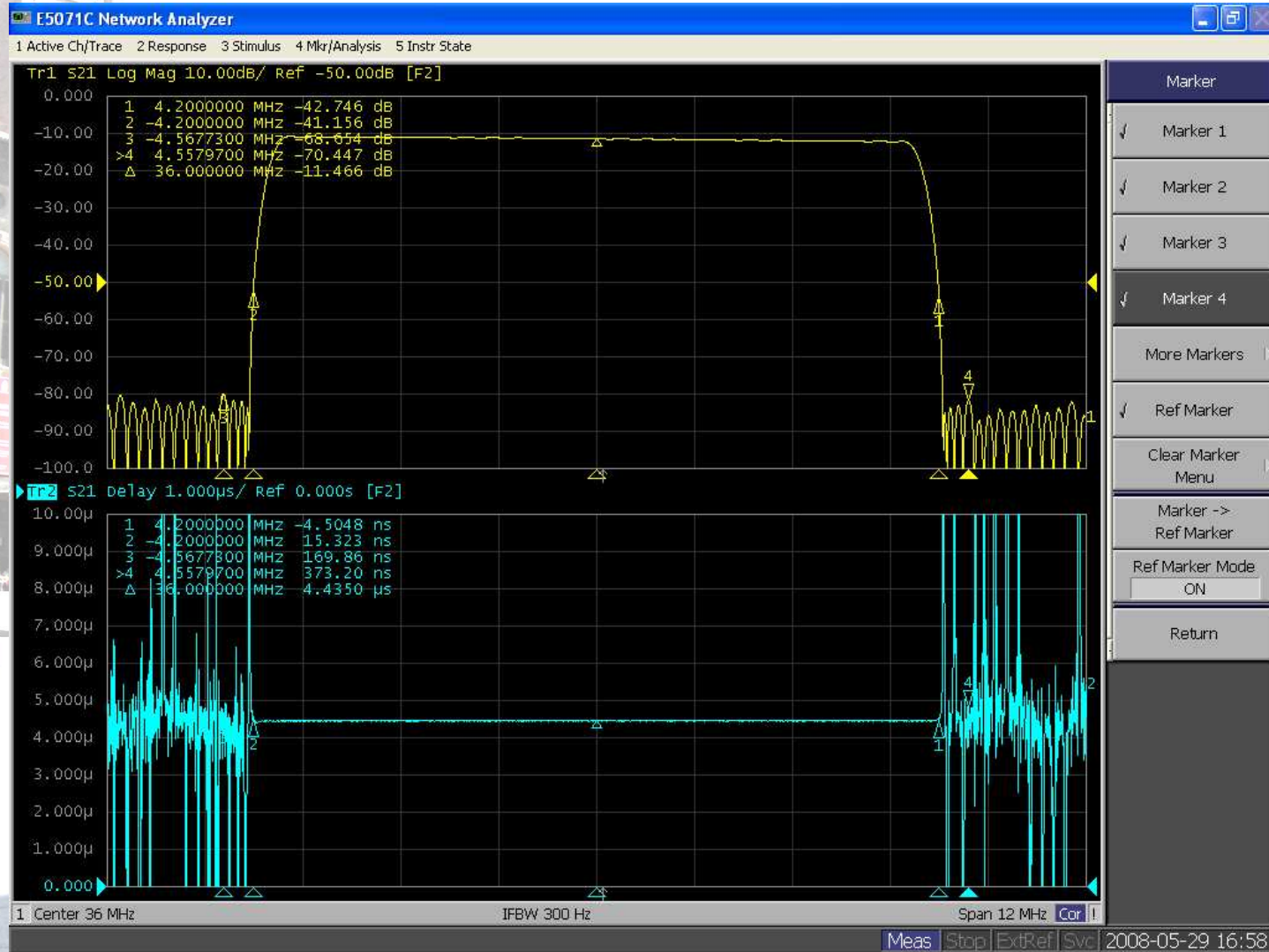


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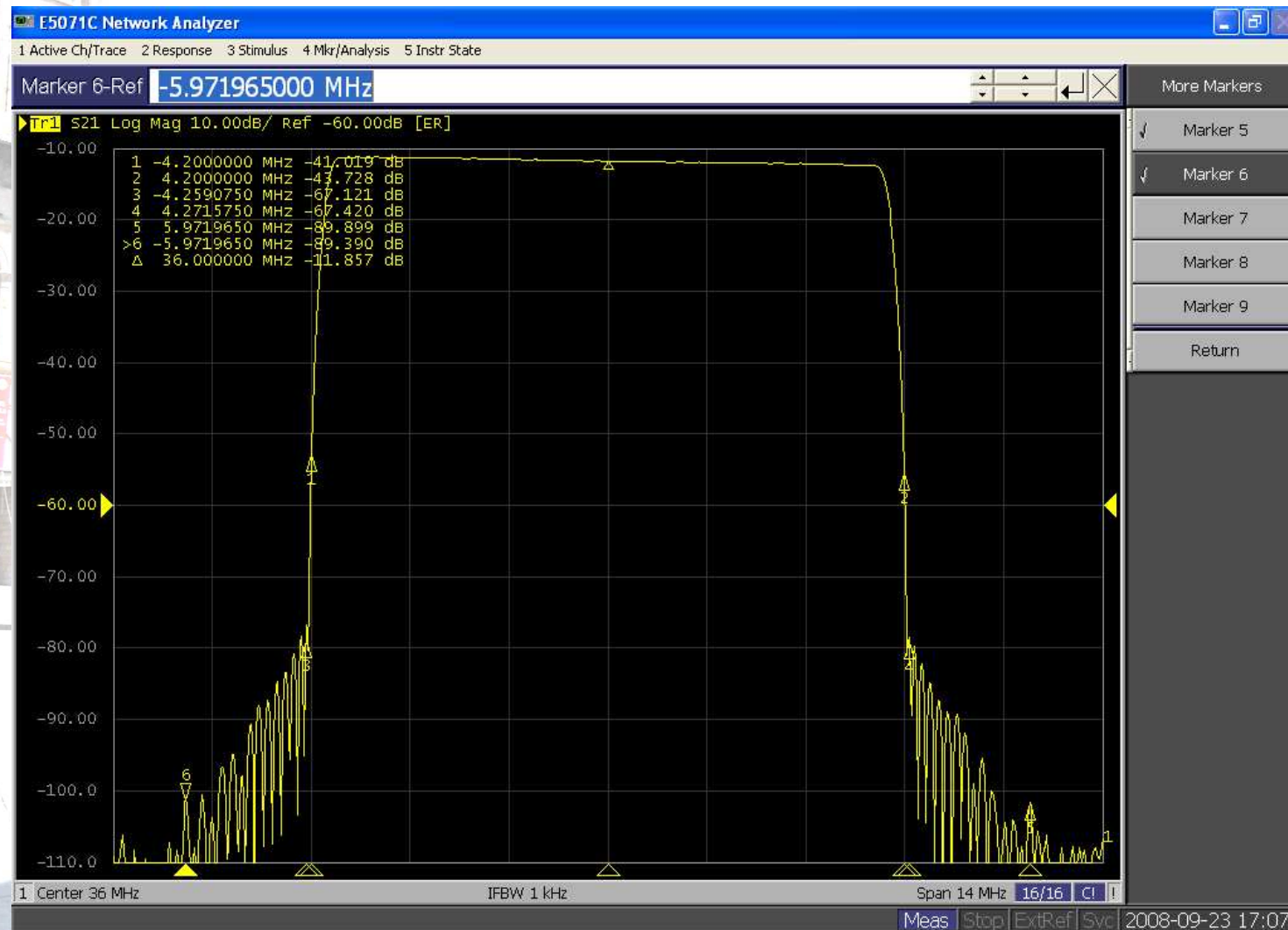
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On network analyzer

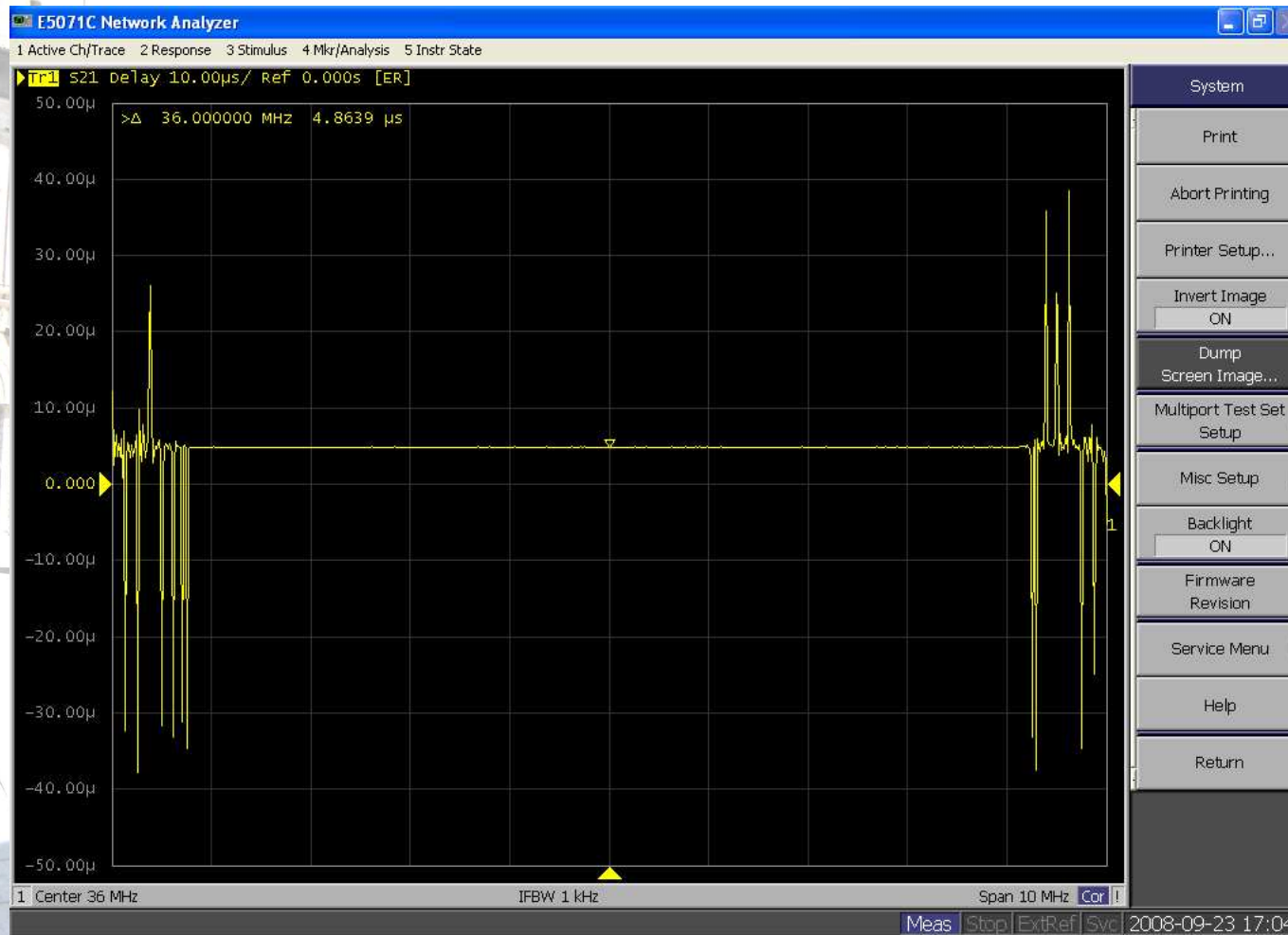


amplitude characteristic



Group delay

Measured group delay = 4.86us



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Conclusions

- Multistage Filters: researches and studies have to be done in order to find best compromise between taps and group delay;
- DVBT2: group delay is a strong requirements?
- Measurements and experiments have to be done to test our criteria on FPGA board.

PAPER:

“On the Design of Multistage Decimators with Minimum Group Delay”, R.Soloperto, G.Pasolini and O.Andrisano, submitted to GLOBECOM2009

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Thank you for your attention!

for questions and discussions,
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