

Curriculum Vitae

Andrea Pietracaprina

Dipartimento di Ingegneria dell'Informazione, Università di Padova
Via Gradenigo 6/B, I35131 Padova, Italy
Tel.: +39 049 827949, Fax: +39 049 8277799
E-mail andrea.pietracaprina@unipd.it
URL <http://www.dei.unipd.it/~capri>

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Personal

Birth: Sassari, Italy, September 17, 1963.

Residence: Via Bassa 6, I-35127 Padova, Italy.

Education

02/87 **Laurea (summa cum laude)** in Computer Science, University of Pisa, Italy. Advisor: Prof. Fabrizio Luccio. Thesis Title: “A Study of Parallel Hashing in VLSI.”

01/91 **M.S.** in Computer Science, University of Illinois at Urbana-Champaign. Advisor: Prof. Franco P. Preparata. Thesis Title: “Analysis of the Unbuffered Butterfly Network.”

05/94 **Ph.D.** in Computer Science, University of Illinois at Urbana-Champaign. Advisor: Prof. Franco P. Preparata. Thesis Title: “Isotropic Graphs with Applications to Parallel Computation.”

Professional Appointments

87–87 **Research Assistant**, Dipartimento di Informatica, Università di Pisa, Italy.

89–92 **Research Assistant**, Coordinated Science Laboratory, University of Illinois at Urbana-Champaign.

91–93 **Research Assistant**, Department of Computer Science, Brown University, Providence.

94–95 **Postdoctoral Fellow**, Dipartimento di Elettronica e Informatica, Università di Padova, Italy.

95–98 **Assistant Professor**, Dipartimento di Matematica Pura e Applicata, Università di Padova, Italy.

98–02 **Associate Professor**, Dipartimento di Ingegneria dell'Informazione, Università di Padova, Italy.

02– **Full Professor**, Dipartimento di Ingegneria dell'Informazione, Università di Padova, Italy.

08– **Vice-Chair**, Dipartimento di Ingegneria dell'Informazione, Università di Padova, Italy.

Other Appointments

87-88 **Officer** in the Italian Army.

Awards

- IBM Italia Award for Laurea Thesis in Computer Science, 1987.
- UNITEAM Award for Laurea Thesis in Computer Science, 1987.
- Best Paper Award 2004 at the International Parallel and Distributed Processing Symposium.

Teaching

Courses

- *Parallel Computation*, Graduate Program in Logics, Mathematics and Theoretical Computer Science, University of Siena, Siena, Italy, (Spring 94 and Spring 96).
- *Parallel Algorithms and Architectures*, Graduate Program in Computer Science, Universities of Bologna, Padova, Venezia, Italy (Spring 95 and Spring 96).
- *Foundations of Computer Science*, Undergraduate Program in Mathematics, University of Padova, Padova, Italy (Spring 97).
- *Programming* (72 h), Undergraduate Program in Mathematics, University of Padova, Padova, Italy (Fall 97).
- *Information Systems* (78 h), Undergraduate Program in Management Engineering, University of Padova, Padova, Italy (1998-2004).
- *Algorithms and Data Structures* (63 h), Undergraduate Program in Computer Engineering (2nd year), University of Padova, Padova, Italy (since 2002).
- *Introduction to Data Mining* (8-12 h), UNESCO Advanced School of Informatics, Damascus, Syria (Spring 2004), Graduate Program in Computer Science, University of Padova (Spring 2002, Fall 2004), Graduate Program in Computer Science and Logics, University of Siena (Fall 2005).
- *Management and Processing of Large Data Sets* (54 h), Undergraduate Program in Computer Engineering (5th year), University of Padova, Padova, Italy (since 2005).

Research

Current Areas of Interest

- High-Performance Computing: Models, Algorithms and Data Structures
- Data Mining
- Interconnection Networks and Routing

Funding

- **Project Coordinator** for CNR Bilateral Projects CNR96-02538-CT07 and CNR-97-03207-CT07 on *Load Balancing and Exhaustive Search Techniques for Parallel Architectures*, in collaboration with University College Cork, Cork, Ir, (1996–1997)
- **Project Coordinator** for the project CDPA-033838: *A Programming Framework for Parallel and Hierarchical Machines: Theory and Implementation*, funded by the University of Padova (2004–2005).
- **Principal Investigator** for NATO Project CRG 961243 on *Bulk Synchronous Computational Geometry*, in collaboration with Texas A&M University, College Station, USA, (1996–1997).
- **Key Researcher** for the following projects: *Foundations of GEneral Purpose Parallel COMputing*, ESPRIT-GEPPCOM No.9072 (1994-1997); *Algorithms, Models of Computations e Information Structures*, MURST 40%, (1995-1997); *Algorithms for Large Data Sets: Science and Engineering*, MURST PRIN (1999-2001); *Center of Excellence: Science and Applications of Advanced Computational Paradigms*, funded by the University of Padova (2001–2004); ALINWEB: *Algorithmics for Internet and for the Web*, MIUR PRIN (2002-2004); ALGONEXT: *Algorithms for the Next Generation Internet and the Web*, MIUR PRIN (2004-2006); MAINSTREAM: *Algorithms for Massive Information Structures and Data Streams*, MIUR PRIN (2007-2009); AEOLUS: *Algorithmic Principles for Building Efficient Overlay Computers*, EU FP6 Integrated Project: (2005-2009)

Program Committees

- *4th International Euro-Par Conference*, Southampton, UK, September 1998.
- *37th Annual AICA Conference*, Abano Terme, Italy, September 1999.
- *ACM SPAA '02: 14th Annual ACM Symposium on Parallel Algorithms and Architectures*, Winnipeg, Canada, August 2002.
- *ICTCS'03: 8th Italian Conference on Theoretical Computer Science*, Bertinoro, Italy, October 2003.
- *IASTED PDCN'04: International Conference on Parallel and Distributed Computing and Networks*, Innsbruck, Austria, February 2004.

- *FUN'04: 3rd International Conference on FUN with Algorithms*, Elba Island, May 2004.
- *10th International Euro-Par Conference*, Pisa, Italy, August 2004.
- *WEA'05: 4th International Workshop on Efficient and Experimental Algorithms*, Santorini, Greece, May 2005.
- *HLPP'05: 3rd International Workshop on High-level Parallel Programming and Applications* Coventry, UK, July 2005.
- *ACM SPAA'05: 17th Annual ACM Symposium on Parallel Algorithms and Architectures*, Las Vegas NV, USA, July 2005.
- *11th International Euro-Par Conference*, Lisbon, Portugal, August/September 2005. (*Global Chair* of Topic 12: “Theory and Algorithms for Parallel Computation”.)
- *I-SPAN'05: 8th International Symposium on Parallel Architectures, Algorithms, and Networks*, Las Vegas NV, USA, December 2005.
- *HPPC'07: Workshop on Highly Parallel Processing on a Chip*, in conjunction with the 13th Euro-Par Conference, Rennes, F, August 2007.
- *PACT'07: Parallel Architectures and Compilation Techniques*, Brasov, Romania, September 2007.
- *IPDPS'08: IEEE International Parallel and Distributed Processing Symposium*, Miami FL, USA, April 2008.
- *ACM SPAA'08: 20th Annual ACM Symposium on Parallel Algorithms and Architectures*, Munich, D, June 2008.
- *15th International Euro-Par Conference*, Delft, The Netherlands, August 2009. (*Global Chair* of Topic 12: “Theory and Algorithms for Parallel Computation”.)

Other Committees

- *Italian-Israeli Workshop on Algorithmic Aspects of Molecular Biology*, Padova, Italy, 1994. Member of the Organizing Committee.
- *Summer School on Architectures and Programming Paradigms for Parallel Computers*, Padova, Italy, 1996. Lecturer and member of the Organizing Committee.
- *ACM SPAA'96: 8th ACM Symposium on Parallel Algorithms and Architectures*, Padova, Italy, 1996. Member of the Organizing Committee.
- *ESA'98: 6th Annual European Symposium on Algorithms*, Venezia, Italy, 1998. Member of the Organizing Committee.
- *Euro-Par Conference*. Member of the Advisory Board from 1999.
- *ICALP'06: 33rd International Colloquium on Automata, Languages and Programming*, Venezia, Italy, 2006. Co-Chair of the Satellite Events Committee.

Editorial Activities

- *IEEE Transactions on Parallel and Distributed Computing*: Associate Editor (since 2004)
- *Theoretical Computer Science*: Guest Co-Editor of Special Issue in honour of F. Preparata

Invited Lectures

- 09/95 *Dagstuhl-Seminar 9537 on Parallel and Distributed Algorithms*, Schloss Dagstuhl, D.
- 12/95 *Heinz Nixdorf Institute*, University of Paderborn, Paderborn, D.
- 06/96 *Summer School on Architectures and Programming Paradigms for Parallel Computers*, Padova, Italy.
- 09/96 *Chinese Academy of Sciences*, Beijing, China.
- 09/97 *Dagstuhl-Seminar 9737 on Parallel and Distributed Algorithms*, Schloss Dagstuhl, D.
- 05/99 *DIMACS Workshop on Distributed Data and Structures*, Computer Science Department, Princeton University, Princeton, NJ, USA.
- 10/01 *Workshop on Advanced MEthods and Tools for Computational Science and Engineering*, Roma, Italy.
- 11/03 *Workshop on Frequent Itemset Mining Implementations (FIMI'03)*, Melbourne FL, USA (panelist).
- 09/04 *Scalable Approaches to High Performance and High Productivity Computing (ScalPerf04)*, Bertinoro, I.
- 10/05 *Scalable Approaches to High Performance and High Productivity Computing (ScalPerf05)*, Bertinoro, I.
- 09/07 *Scalable Approaches to High Performance and High Productivity Computing (ScalPerf07)*, Bertinoro, I.
- 11/08 *Workshop on Random Graphs and Randomized Algorithms (RandomGraals)*, Bertinoro, I.
- 06/09 *Dagstuhl-Seminar on Dynamic Communication Networks*, Schloss Dagstuhl, D.

Refereeing

Journals: *Algorithmica*, *SIAM Journal on Computing*, *Mathematical Systems Theory*, *Theory of Computing Systems*, *Mathematical Structures in Computer Science*, *Networks, Information Processing Letters*, *Parallel Processing Letters*, *Journal on Parallel and Distributed Computing*, *IEEE Transactions on Parallel and Distributed Systems*.

Conferences: ACM Symposium on Theory of Computing (STOC), ACM Symposium on Parallel Algorithms and Architectures (SPAA), International Colloquium on Automata, Languages, and Programming (ICALP), Annual Allerton Conference, European Symposium on Algorithms (ESA), Symposium on Theoretical Aspects of Computer Science (STACS)

Projects: Reviewer for two projects funded within the 5th EU Framework Programme

Publications

Books and Book Chapters

- [1] G. Bilardi, G.F. Italiano, A. Pietracaprina, and G. Pucci, editors. *Proceedings of the 6th Annual European Symposium on Algorithms (ESA'98)*. LNCS 1461. Springer-Verlag, Venice, I, August 1998.
- [2] G. Bilardi, A. Pietracaprina, and G. Pucci. Decomposable BSP: A Bandwidth-Latency Model for Parallel and Hierarchical Computation. In *Handbook of Parallel Computing*, (J. Reif and S. Rajasekaran Eds.), CRC Press 2007. In Print.
- [3] N.M. Amato, D.T. Lee, A. Pietracaprina, R. Tamassia (eds). Excursions in Algorithmics: A Collection of Papers in Honor of Franco P. Preparata. In *Special Issue of Theoretical Computer Science* 408(2-3), 2008.

Journals

- [4] F. Luccio, A. Pietracaprina, and G. Pucci. A probabilistic simulation of PRAMs on a bounded degree network. *Information Processing Letters*, 28:141–147, 1988.
- [5] F. Luccio, A. Pietracaprina, and G. Pucci. A new scheme for the deterministic simulation of PRAMs in VLSI. *Algorithmica*, 5(4):529–544, 1990.
- [6] F. Luccio, A. Pietracaprina, and G. Pucci. Analysis of parallel uniform hashing. *Information Processing Letters*, 37(2):67–69, 1991.
- [7] F. Luccio, A. Pietracaprina, and G. Pucci. Analysis and implementation of parallel uniform hashing. *The International Journal on Foundations of Computer Science*, 3(1):55–63, 1992.
- [8] A. Krishna, A. Pietracaprina, and B. Hajek. Sharper analysis of packet routing on a butterfly. *Networks*, 24(2):91–101, 1994.
- [9] A. Pietracaprina and F.P. Preparata. Practical constructive schemes for deterministic shared-memory access. *Theory of Computing Systems*, 30(1):3–37, Jan/Feb 1997. Special Issue for SPAA'93.
- [10] A. Pietracaprina and G. Pucci. The complexity of deterministic PRAM simulation on Distributed Memory Machines. *Theory of Computing Systems*, 30(3):231–247, May/June 1997.

- [11] A. Bäumer, W. Dittrich, and A. Pietracaprina. The complexity of parallel multisearch on coarse grained machines. *Algoritmica*, 24:209–242, 1999. Special Issue on Coarse Grained Parallel Algorithms.
- [12] G. Bilardi, K.T. Herley, A. Pietracaprina, G. Pucci, and P. Spirakis. BSP vs LogP. *Algoritmica*, 24:405–422, 1999. Special Issue on Coarse Grained Parallel Algorithms.
- [13] K. Herley, A. Pietracaprina, and G. Pucci. Fast deterministic branch-and-bound. *Parallel Processing Letters*, 9(3):325–334, 1999.
- [14] K. Herley, A. Pietracaprina, and G. Pucci. Deterministic branch-and-bound on distributed memory machines. *Intl. Journal of Foundations of Computer Science*, 10(4):391–404, 1999.
- [15] A. Pietracaprina, G. Pucci, and J. Sibeyn. Constructive, deterministic implementation of shared memory on meshes. *SIAM Journal on Computing*, 30(2):625–648, 2000.
- [16] K. Herley, A. Pietracaprina, and G. Pucci. Implementing shared memory on mesh-connected computers and on the fat-tree. *Information and Computation*, 165:123–142, 2001.
- [17] R. Grossi, A. Pietracaprina, and G. Pucci. Optimal deterministic protocols for mobile robots on a grid. *Information and Computation*, 173:132–142, 2002.
- [18] K. Herley, A. Pietracaprina, and G. Pucci. Deterministic parallel backtrack search. *Theoretical Computer Science*, 270(1-2):309–324, 2002.
- [19] C. Fantozzi, A. Pietracaprina, and G. Pucci. A general PRAM simulation scheme for clustered machines. *Intl. Journal of Foundations of Computer Science*, 14(6):1147–1164, 2003.
- [20] G. Bilardi, K.T. Herley, A. Pietracaprina, and G. Pucci. On Stalling in LogP. *Journal of Parallel and Distributed Computing*, 65(3):307–312, 2005.
- [21] A. Pietracaprina and G. Pucci. Optimal many-to-one routing on the mesh with constant queues. *Information Processing Letters*, 96(1):24–29, 2005.
- [22] C. Fantozzi, A. Pietracaprina, and G. Pucci. Translating Submachine Locality into Locality of Reference. *Journal of Parallel and Distributed Computing*, 66(5):633–646, 2006. Special issue on the four Best Papers of IPDPS 2004.
- [23] K.T. Herley, A. Pietracaprina, and G. Pucci. Store-and-forward multicast routing on the mesh. *Theory of Computing Systems*, (42):519–535, 2008.
- [24] P. Bertasi, M. Bianco, A. Pietracaprina, G. Pucci. Obtaining Performance Measures through Microbenchmarking in a Peer-to-Peer Overlay Computer. *International Journal of Computational Intelligence Research*. To appear, 2007.
- [25] N.M. Amato, D.T. Lee, A. Pietracaprina, R. Tamassia (eds). Preface. *Special Issue of Theoretical Computer Science*, 408(2-3):97–98, 2008.

- [26] P. Crescenzi, C. Nocentini, A. Pietracaprina, and G. Pucci. On the Connectivity of Bluetooth-Based Ad Hoc Networks. *Concurrency and Computation: Practice and Experience. Special Issue on EURO-PAR'07*. To appear, 2008.

Conferences

- [27] F. Luccio, A. Pietracaprina, and G. Pucci. Analysis and implementation of parallel uniform hashing. In *Proc. 1st Italian Conference on Algorithms and Complexity*, pages 1–12, Roma, October 1990. World Scientific.
- [28] A. Krishna, A. Pietracaprina, and B. Hajek. Packet routing in optimal time on a butterfly. In *Proc. of the 10th IEEE INFOCOM*, pages 0840–0849, Bal Harbour, FL, April 1991.
- [29] A. Pietracaprina and F.P. Preparata. An $O(\sqrt{n})$ -worst-case-time solution to the granularity problem. In K.W. Wagner P. Enjalbert, A. Finkel, editor, *Proc. 10th Symp. on Theoretical Aspects of Computer Science*, LNCS 665, pages 110–119, Würzburg, Germany, February 1993. Springer-Verlag.
- [30] A. Pietracaprina and F.P. Preparata. A practical constructive scheme for deterministic shared-memory access. In *Proc. 5th ACM Symp. on Parallel Algorithms and Architectures*, pages 100–109, 1993.
- [31] A. Pietracaprina, G. Pucci, and J. Sibeyn. Constructive deterministic PRAM simulation on a mesh-connected computer. In *Proc. 6th ACM Symp. on Parallel Algorithms and Architectures*, pages 248–256, Cape May, NJ, June 1994.
- [32] A. Pietracaprina and G. Pucci. Tight bounds on deterministic PRAM emulations with constant redundancy. In J.V. Leeuwen, editor, *Proc. 2nd European Symposium on Algorithms*, LNCS 855, pages 319–400, Utrecht, NL, September 1994. Springer-Verlag.
- [33] A. Pietracaprina and G. Pucci. Improved deterministic PRAM simulation on the mesh. In *Proc. 22nd Int. Colloquium on Automata, Languages and Programming*, LNCS 1099, pages 598–609, Szeged, H, July 1995. Springer-Verlag.
- [34] K. Herley, A. Pietracaprina, and G. Pucci. Implementing shared memory on multi-dimensional meshes and on the fat-tree. In *Proc. of the 3rd European Symposium on Algorithms*, LNCS 979, pages 60–74, 1995.
- [35] G. Bilardi, K.T. Herley, A. Pietracaprina, G. Pucci, and P. Spirakis. BSP vs LogP. In *Proc. of the 8th ACM Symp. on Parallel Algorithms and Architectures*, pages 25–32, 1996.
- [36] A. Bäumer, W. Dittrich, and A. Pietracaprina. The deterministic complexity of parallel multisearch. In *Proc. of the 5th Scandinavian Workshop on Algorithm Theory*, LNCS 1097, pages 404–415, 1996.
- [37] K. Herley, A. Pietracaprina, and G. Pucci. Fast deterministic backtrack search. In *Proc. of the 23rd Int. Colloquium on Automata, Languages and Programming*, LNCS 1099, pages 598–609, July 1996.

- [38] A. Pietracaprina. Deterministic routing of h -relations on the multibutterfly. In *Proc. of the First Merged IPPS/SPDP Symposium: 12th International Parallel Processing Symposium and 9th Symposium on Parallel and Distributed Processing*, pages 375–379, Orlando, Florida, March-April 1998.
- [39] R. Grossi, A. Pietracaprina, and G. Pucci. Optimal deterministic protocols for mobile robots on a grid. In *Proc. of the 6th Scandinavian Workshop on Algorithm Theory*, LNCS 1432, pages 181–192, Stockholm, Sweden, July 1998.
- [40] K. Herley, A. Pietracaprina, and G. Pucci. Deterministic branch-and-bound on distributed memory machines. In *Proc. of IRREGULAR*, pages 1085–1094, Puerto Rico, USA, April 1999.
- [41] G. Bilardi, A. Pietracaprina, and G. Pucci. A quantitative measure of portability with application to bandwidth-latency models for parallel computing. In *Proc. of EUROPAR 99*, LNCS 1685, pages 543–551, September 1999.
- [42] N.M. Amato, J. Perdue, A. Pietracaprina, G. Pucci, L.K. Dale, and J. Purdue. Predicting performance on smp's. a case study: The sgi power challenge. In *Proc of the Int. Parallel and Distributed Processing Symposium (IPDPS) 2000*, pages 729–737, 2000.
- [43] G. Bilardi, K. Herley, A. Pietracaprina, and G. Pucci. On stalling in LogP. In *Proc. of the Workshop on Advances in Parallel and Distributed Computational Models*, LNCS 1800, pages 109–115, May 2000.
- [44] G. Bilardi, A. Pietracaprina, and P. D'Alberto. On the space and access complexity of computation dags. In *Proc. of the 26th Workshop on Graph-Theoretic Concepts in Computer Science*, LNCS 1928, pages 47–58, Konstanz, D, May 2000.
- [45] C. Fantozzi, A. Pietracaprina, and G. Pucci. Implementing shared memory on clustered machines. In *Proc. of 15th International Parallel and Distributed Processing Symposium*, San Francisco, USA, 2001.
- [46] G. Bilardi, C. Fantozzi, A. Pietracaprina, and G. Pucci. On the effectiveness of D-BSP as a bridging model of parallel computation. In *Proc. of the Int. Conference on Computational Science*, LNCS 2074, pages 579–588, 2001.
- [47] K.T. Herley, A. Pietracaprina, and G. Pucci. One-to-many routing on the mesh. In *Proc. of the 13th ACM Symp. on Parallel Algorithms and Architectures*, pages 31–37, Heraklion, GR, June 2001.
- [48] A. Pietracaprina and G. Pucci. Optimal many-to-one routing on the mesh. In *Proc. of EURO-PAR 2001*, LNCS 2150, pages 645–650, Manchester, UK, August 2001. Springer-Verlag.
- [49] F. Dehne, S. Mardegan, A. Pietracaprina, and G. Prencipe. Distribution sweeping on clustered machines with hierarchical memories. In *Proc. of the 16th International Parallel and Distributed Processing Symposium*, Fort Lauderdale, USA, April 2002.
- [50] C. Fantozzi, A. Pietracaprina, and G. Pucci. Seamless integration of parallelism and memory hierarchy. In *Proc. of 29th Int. Colloquium on Automata, Languages and Programming*, LNCS 2380, pages 856–867, July 2002.

- [51] A. Pietracaprina and D. Zandolin. Mining frequent itemsets using Patricia tries. In *Proc. of the Workshop on Frequent Itemset Mining Implementations (FIMI03)*, Vol. 90, Melbourne, USA, November 2003. CEUR-WS Workshop On-line Proceedings.
- [52] C. Fantozzi, A. Pietracaprina, and G. Pucci. Translating submachine locality into locality of reference. In *Proc. 18th International Parallel and Distributed Processing Symposium*, Santa Fe, USA, April 2004. Best Paper Award.
- [53] G. Bilardi, A. Pietracaprina, G. Pucci, F. Schifano and R. Tripiccion. The potential of on-chip multiprocessing for QCD machines. In *Proc. 12th International Conference on High-Performance Computing*, LNCS Vol. 3769, pages 386-397, 2005.
- [54] A. Pietracaprina, G. Pucci, F. Silvestri. Cache-oblivious simulation of parallel programs. In *Proc. 8th IPDPS Workshop on Advances in Parallel and Distributed Computational Models*, Rhodes Island, GR, April 2006.
- [55] G. Bilardi, A. Pietracaprina, G. Pucci, F. Silvestri. Network-oblivious algorithms. In *Proc. 21st International Parallel and Distributed Processing Symposium*, Long Beach, USA, March 2007.
- [56] A. Pietracaprina, and F. Vandin. Efficient Incremental Mining of Top-K Frequent Closed Itemsets. In *Proc. Discovery Science (DS) 2007*, LNCS 4755, pages 275-280, 2007.
- [57] P. Crescenzi, C. Nocentini, A. Pietracaprina, G. Pucci, and C. Sandri. On the Connectivity of Bluetooth-Based Ad Hoc Networks. In *Proc. EURO-PAR'07 Parallel Processing*, LNCS Vol. 4641, pages 960-969, 2007.
- [58] P. Bertasi, M. Bianco, A. Pietracaprina, and G. Pucci. Obtaining Performance Measures through Microbenchmarking in a Peer-to-Peer Overlay Computer. In *Proc. 1st International Workshop on P2P, Parallel, Grid and Internet Computing, 3PGIC-2007*.

Posters

- [59] N.M. Amato, A. Pietracaprina, G. Pucci, L.K. Dale, and J. Purdue. A cost model for shared memory access on a symmetric multiprocessor. In *10th ACM Symp. on Parallel Algorithms and Architectures*, Puerto Vallarta, Mexico, June/July 1998. Poster.

Theses and Technical Reports

- [60] A. Pietracaprina. Analysis of the unbuffered butterfly network. Master's thesis, Center for Compound Semiconductor Microelectronics, University of Illinois at Urbana-Champaign, November 1990. Tech. Rep. UILU-ENG-90-0401.
- [61] A. Pietracaprina. *Isotropic Graphs with Applications to Parallel Computation*. PhD thesis, Department of Computer Science, University of Illinois at Urbana-Champaign, January 1994. Tech. Rep. UIUCDCS-R-94-1847.
- [62] A. Pietracaprina and F.P. Preparata. Bufferless packet routing in high-speed networks. Technical Report Rapporto Interno N. 4 – 96, Dipartimento di Matematica, Università di Padova, Padova, Italy, May 1996.

- [63] K. Herley, A. Pietracaprina, and G. Pucci. Deterministic parallel algorithms for back-track search and branch-and-bound. Technical Report Rapporto Interno N. 5 – 96, Dipartimento di Matematica, Università di Padova, Padova, Italy, May 1996.