# DESIGN CRITERIA FOR POWER FACTOR PREREGULATORS BASED ON SEPIC AND CUK CONVERTERS IN CONTINUOUS CONDUCTION MODE

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**Abstract - Sepic and Cuk converters used as power factor preregulators in continuous conduction mode are analyzed.**

**The application of the average current mode control technique to obtain sinusoidal input current is investigated. It is shown that, differently from the usual boost topology, the gain of the internal current loop depends strongly on the instantaneous input voltage. Moreover, the presence of undamped complex poles and zeroes makes difficult design of a stable control.**

**The paper shows that stability can be achieved by using a suitable damping network, which properly shapes the current loop transfer function without introducing significant power losses. With this provision, a standard PI controller can be used to ensure the desired phase margin in any operating condition.**

**Detailed design criteria of both power and control stages are given in the paper. Results of a 300W prototype based on the Sepic topology are also reported.**

## I. INTRODUCTION

With the ever-increasing demand for power quality from the utility, power factor correction (PFC) is becoming basic requirement for switching power supplies.

High-quality rectifiers, called Power Factor Preregulators (PFP's), are used to interface ac line and dc load, their goal being to appear to the line as a resistive load, so achieving unity power factor even in presence of distorted line voltage.

The most popular PFP is the boost converter, which is a simple topology from both power and control points of view. However, boost PFP's have some basic limitations, namely output voltage greater than peak input voltage, difficult implementation of high-frequency insulation and lack of current limitation during start-up and overload conditions.

All these limitations can be overcome by using Sepic- and Cuk-type power factor preregulators, which have the additional advantage of input current ripple reduction by means of inductor coupling [1-2]. The analysis of these converters in the Discontinuous Conduction Mode (DCM) has already been carried out [1-3], showing good performances even with simple control. In fact, almost unity power factor is achieved with no need for duty-cycle modulation (voltage follower approach). However, while the Discontinuous Conduction Mode is well suited for low-power applications, Continuous Conduction Mode (CCM) is still the primary choice for many medium- and high-power applications.

In this paper, the application of the average current mode control technique to Sepic and Cuk converters used as PFP's in CCM is investigated.

This control technique, already discussed with reference to the boost topology [4], requires the design of a large-bandwidth internal current loop in order to obtain low-distorted input current. It is shown that, differently from the boost converter, with Sepic and Cuk topologies the gain of the internal current loop depends strongly on instantaneous input voltage, and the presence of undamped complex poles and zeroes makes difficult the design of a stable control.

To overcome these problems, a suitable damping network is proposed, which properly shapes the current loop transfer function without introducing significant losses. With this provision, a standard PI controller in the current loop ensures the desired phase margin in any operating condition.

Design criteria of both power and control stage are also given in the paper.

## II. REVIEW OF AVERAGE CURRENT MODE CONTROL (ACMC) FOR PFC

The recently proposed average current mode control has been widely used in power-factor correction applications. Fig.1 shows the conceptual circuit diagram of the boost PFC circuit with average current mode control.

It includes an inner current loop and an outer voltage loop.

In the current loop, input inductor current $i_g$ is sensed, compared to a sinusoidal reference value $I_{ref}$ and then processed by a suitable current error amplifier $G_i$. Current error amplifier output is compared with a fixed ramp to generate a proper driving signal for the switch.

The outer voltage loop provides the proper current reference signal $I_{REF}$ by multiplying a scaled replica of the rectified voltage by the output of voltage error amplifier $G_v$.

As already shown in [8], the voltage loop must have a very low bandwidth, well below the line frequency, in order to minimize input current distortion.

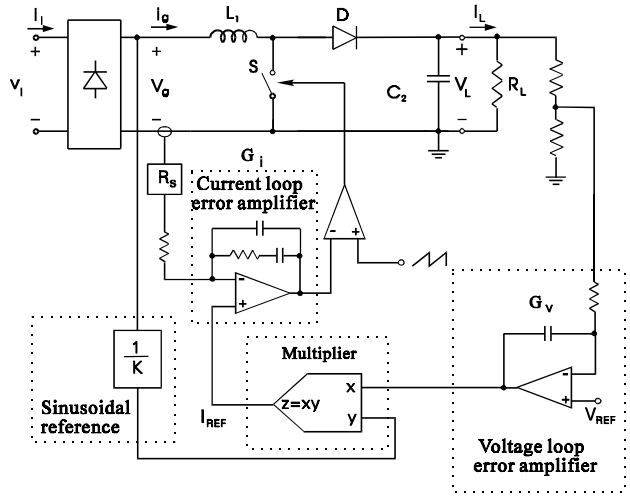


Fig.1. Average current mode control of boost converter.

## III. Application of ACMC to Cuk and Sepic Converters

Fig.2 shows the basic schemes of PFP's based on Sepic and Cuk topologies with high-frequency insulation transformer. The control scheme is the same shown in Fig.1.

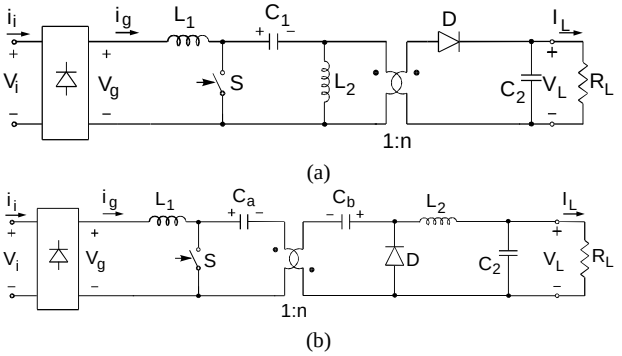


Fig 2. Sepic (a) and Cuk (b) converters for PFP's.

The design of the current error amplifier requires a small-signal analysis of the power stage (transfer function between duty-cycle and input inductor current). For this purpose, we assume a quasi-static condition, i.e., that each operation cycle at line frequency is made up of a sequence of steady-state conditions, each one corresponding to a different value of the input voltage. This is true provided that the switching frequency is much higher than the line frequency.

*A. Power Stage Small Signal Analysis*

The PWM switch approach [5] is used for the small signal analysis of Cuk and Sepic converters. This method relies on the identification of a three-terminal non-linear device (Fig.3a), called the PWM switch, which totally represents the non-linearity of the PWM converter. Substituting the PWM switch with its equivalent small signal model (Fig.3b) in the desired operating condition allows study of the small signal converter characteristics without any need of converter equations linearization (as it is required by the state-space averaging approach).

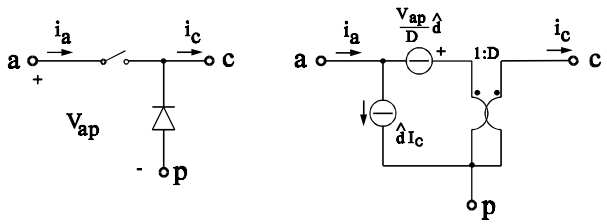

Fig 3. a) PWM switch, b) its equivalent small signal model in CCM in which D is the duty-cycle and $\hat{d}$ is its small signal variation

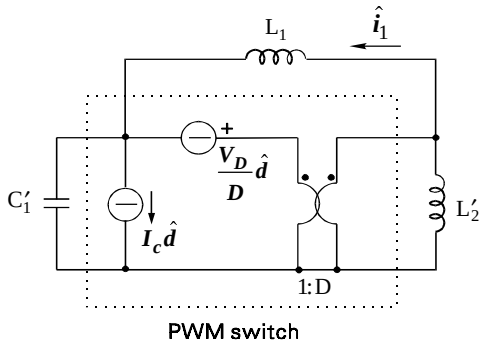


Fig.4 - Simplified small-signal model for Sepic and Cuk converters in CCM.

**Table I. Small-signal model parameters**

| | Sepic | Cuk |
|---|---|---|
| $V_D$ | $V_g + V_L/n$ | $V_g + V_L/n$ |
| $I_c$ | $I_1 + I_2$ | $I_1 + n I_2$ |
| $C_1'$ | $C_1$ | $C_a n^2 C_b / \left(C_a + n^2 C_b\right)$ |
| $L_2'$ | $L_2$ | $L_2 / n^2$ |

The PWM switch model, applied to Sepic and Cuk converters, gives the scheme of Fig.4, the related parameters being given in Table I. The output filter capacitor is considered as a short circuit at high frequency: in fact, it is usually large in order to meet the hold-up-time requirement and to reduce the 100Hz ripple.

The model parameters vary with the converter working point, which continuously changes during the line period. From the model, the desired transfer function $G_{id}(s)$ can be derived as follows:

$$G_{id}(s) = \frac{\hat{i}_1}{\hat{d}} = DV_D \cdot \frac{L'}{L_2' L_1} \cdot \frac{1 + \frac{I_c}{V_D}\frac{D'}{D} L_2' \cdot s + \frac{L_2' C_1'}{D} \cdot s^2}{s \cdot \left(1 + L' C_1' \cdot s^2\right)} \quad (1)$$

where D'=1-D and

$$L' = \frac{L_1 L_2'}{D^2 L_1 + D'^2 L_2'} \qquad (2)$$

The transfer function contains a pole in the origin, a pair of undamped complex poles and a pair of complex zeroes with negative real part. It is important to note that all these quantities are changing within the line period.

*B. Transfer Function Analysis*

Amplitude and phase plots of $G_{id}(s)$, for the Sepic converter whose parameters are listed in the experimental results section are shown in Fig.5.

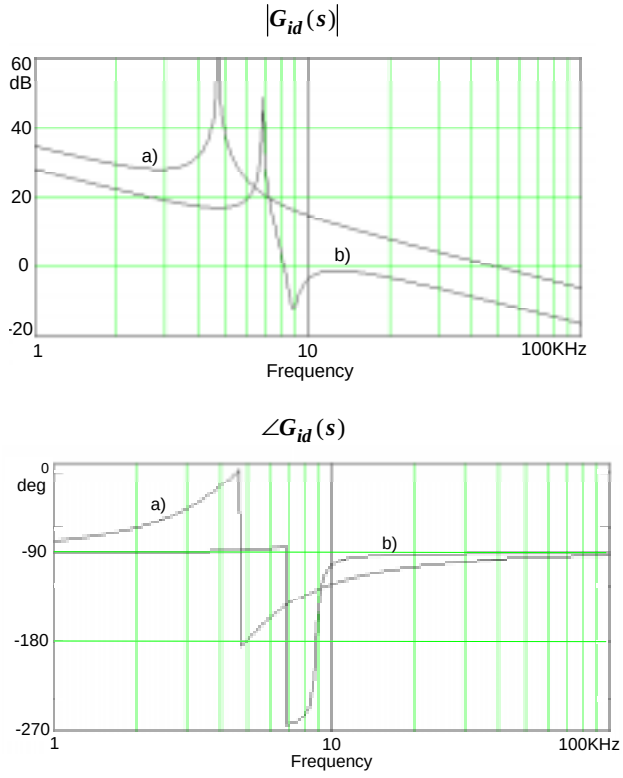


Fig.5 - Amplitude and phase diagrams of $G_{id}(s)$ in two operating points: a) $\theta=\pi/2$, b) $\theta=\pi/18$

Two operating conditions are considered, corresponding to the peak of the sinusoidal line voltage ($\theta=\omega_l t=\pi/2$) and to a point near its zero crossing ($\theta=\pi/18$). As stated above, the gain, as well as the position of poles and zeroes, changes greatly during the line cycle. Moreover, for small values of $\theta$, the phase behavior becomes difficult to compensate. This is because the zeroes pair moves at higher frequencies with respect to the poles pair, and goes close to the imaginary axis, so that the total phase leg exceeds -180deg.

A simple analysis of (1) shows that it is not possible to keep the natural frequency of the zeroes always below that of the poles, even if, for high values of $L_2/L_1$ ratio, the exchange happens at very low values of angle q. Of course, we may expect a better behavior from a real converter, thanks to unavoidable losses which help damping the complex poles, so reducing the total phase leg. Anyway, it is not a good policy to rely on non negligible converter losses to ensure system stability.

It is also interesting to note that, for high values of complex frequency s, the transfer function tends to the value:

$$G_{id}(s) \approx \frac{V_D}{sL_1} \qquad (3)$$

where $V_D$ depends not only on output voltage $V_L$, but also on rectified line voltage $V_g$ (see Table I). Therefore, in Sepic and Cuk converters, a large variation of the current loop bandwidth occurs if a fixed gain feedback circuit is used.

This behavior is significantly different from that of the boost converter, for which $G_{id}(s)$ can be approximated by $V_L/sL_1$, which has a constant gain [4].

## IV. Modification of Basic Converter Structure

In order to properly shape the transfer function, a suitable damping network, i.e. a series $R_d$-$C_d$ in parallel to capacitor $C_1$ for Sepic (or $C_a$ for Cuk) is introduced. With this provision, equation (1) becomes:

$$G_{id}(s) = DV_D \cdot \frac{L'}{L_1 L_2'} \cdot \frac{1 + \left(\frac{I_c}{V_D}\frac{D'}{D}L_2' + \tau_d\right)\cdot s + \left(\frac{L_2'(C_1' + C_d)}{D} + \frac{I_c L'_2}{V_D}\frac{D'}{D}\tau_d\right)\cdot s^2 + \frac{L'_2 C'_1}{D}\tau_d \cdot s^3}{s\cdot\left(1 + \tau_d \cdot s + L'(C_1' + C_d)\cdot s^2 + L'C'_1\tau_d \cdot s^3\right)} \qquad (4)$$

where $t_d = R_d \times C_d$ and the Bode plot of $G_{id}(s)$ becomes that shown in Fig.6.

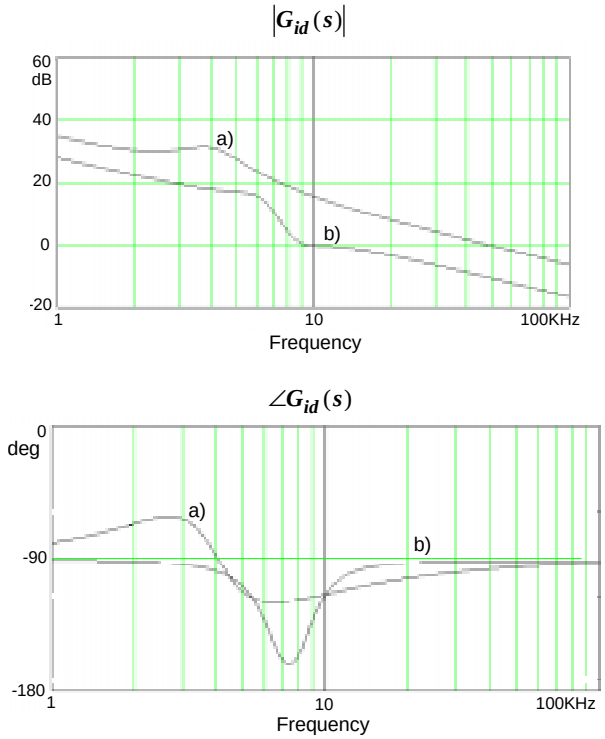


Fig.6 - Amplitude and phase diagrams of $G_{id}(s)$ with damping network in two operating points: a) $\theta=\pi/2$, b) $\theta=\pi/18$

As we can see, the added components introduce a damping factor to the pair of complex poles, so that now it is possible to choose the current error amplifier parameters in order to ensure the desired crossover frequency of the internal current loop with sufficient phase margin in any operating condition.

It is still evident the large gain variation of $G_{id}(s)$ that occurs depending on the instantaneous input voltage and operating condition.

It is important to note that this damping network is placed across a device having a slow varying voltage. Thus, it does not introduce significant power loss.

## V. Converter Design Criteria

This section embodies basic design criteria for Cuk or Sepic PFP's operating in CCM.

### *A. Operation in CCM*

Using the quasi-static approach, PFP's can be considered as dc-dc converters working in very special conditions, since the input voltage $v_g$ is changing continuously during the line cycle, while the output voltage $V_L$ is approximately constant. This situation implies that the dc voltage conversion ratio m and the load $r_L$ "seen" by the converter are changing in each line half-cycle, according to the following equations [3]:

$$m(\theta) = \frac{V_L}{v_g} = \frac{V_L}{V_g \cdot |\sin(\theta)|} = \frac{M}{|\sin(\theta)|} \tag{5}$$

$$r_L(\theta) = \frac{V_L{}^2 / P_L}{2 \cdot |\sin(\theta)|^2} = \frac{R_L}{2 \cdot |\sin(\theta)|^2} \tag{6}$$

where θ is the angular position within the line half-cycle and $P_L$ is the output power. Equation (6) is obtained by averaging the input power during one half-cycle of the line voltage and imposing the power balance condition.

The boundary condition between Continuous Conduction Mode and Discontinuous Conduction Mode can be calculated by equating the dc voltage conversion ratio m(θ) in the two operating conditions.

Defining the adimensional coefficient K as:

$$K = \frac{2L_{eq}}{R_L T} \tag{7}$$

where T is the switching period and:

$$L_{eq} = \frac{L_1 L_2'}{L_1 + L_2'} \tag{8}$$

the CCM operation is verified, for a given angular position θ, when:

$$K > \frac{1}{2 \cdot (M + n \cdot |\sin(\theta)|)^2} \tag{9}$$

where n is the transformer turns ratio $N_2/N_1$.

### *B. Power Stage Design*

Condition (9) can be satisfied only in a limited load range. In fact, increasing $R_L$ produces a consequent decrease of the value of coefficient K until it becomes lower than the second term of (9). Moreover, for a given load resistance, converter operation can change from CCM (near line voltage peak) to DCM (near line voltage zero crossing, see (9)).

Designing the converter to operate always in CCM for a given load calls for an oversize of $L_{eq}$, i.e. of $L_1$ and $L_2$. An alternative approach could be to design the converter to operate in CCM for $\theta_{crit} < \theta < p\text{-}\theta_{crit}$ even at minimum load resistance. The critical angle $\theta_{crit}$ changes as the load $R_L$ changes, and is derived, from (9):

$$\theta_{crit} = \arcsin\left[\frac{1}{n}\left(\sqrt{\frac{R_L T}{4L_{eq}}} - M\right)\right] \tag{10}$$

Operation in DCM is not a problem from device rating point of view, since it occurs near the line voltage zero crossing when few power is transferred. DCM operation causes instead an increase of input current distortion since the dc gain of the power stage transfer function drops significantly; however, it can be shown that stability is always maintained during DCM operation. The choice of $\theta_{crit}$ at full load is therefore a trade-off between size of power stage components and input current distortion in different load conditions.

Once $L_{eq}$ is known, the values of $L_1$ and $L_2$' are calculated from the desired input current ripple and (8).

### *C. Transformer Turns Ratio*

This parameter is selected in order to meet device ratings. For example, Fig.7 shows normalized peak voltage and current stresses in the switch ($v_{spk}$, $i_{spk}$) and in the freewheeling diode ($v_{dpk}$,$i_{dk}$) as a function of n for θ=π/2 (worst condition), for the Sepic converter whose parameter are listed in the experimental results section. Voltages are normalized to input line voltage, while currents are normalized to the output one (at full load).

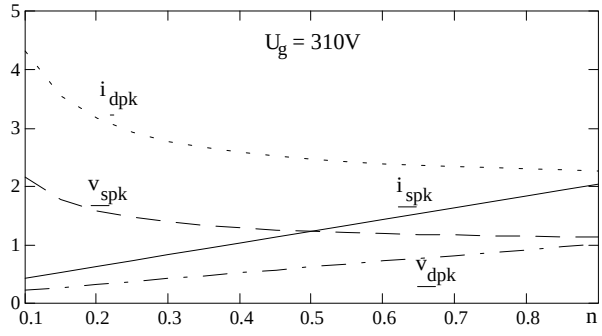


Fig. 7. Normalized switch and diode voltage and current stresses of Sepic converter

For example, looking at the diagram, we see that, in order to use low voltage mosfets, turns ratio n cannot be lower than 0.5. Moreover, the overvoltage due to transformer leakage inductance must be taken into account in the converter design.

### *D. Energy Transfer Capacitor*

The choice of energy transfer capacitor $C_1$ is a trade-off between the needs of low high-frequency voltage ripple and sinusoidal low-frequency behavior. Simulation can be employed for the best choice.

### *E. Damping Network $R_d$-$C_d$*

The network $R_d$-$C_d$ is designed in order to properly damp the pair of complex poles in the transfer function (1). $R_d$ can be selected choosing a suitable value for the merit factor Q corresponding to the L'-C' combination responsible for the pair of complex poles in (1). Therefore:

$$R_d = Q \cdot \sqrt{\frac{C'}{L'}} \qquad (11)$$

The value of capacitor $C_d$ should be chosen in order to have a negligible reactance, with respect to the value of $R_d$, at the natural frequency of L'-C'. This, however, is in contrast with the need of a low capacitance in order to have a sinusoidal voltage across it. In practice, its value must be of the same order of $C_1$'. This constrain limits the choice of Q in (11), and thus limits the effectiveness of the damping network.

*F. Controller Design*

In average current mode control, the current amplifier with a two-pole, one-zero compensation network shown in Fig.1 is normally used. The high-frequency pole is placed after one-half of the switching frequency to filter out the switching ripple of the sensed inductor current. It has little effect on the gain and phase of the current loop in the frequency range of interest.

The position of the compensation zero is selected in order to avoid the phase shift below -180 degrees for whatever operating condition, i.e. to ensure system stability. Placing the zero at higher frequencies results in an increase of the dc gain (and therefore in a decrease of the input distortion), while placing the zero at lower frequencies results in an increase of phase margin. Once again, the choice of the value of the compensation zero is a trade-off between stability and input current distortion.

*G. Line Feedforward for Variable Gain*

As demonstrated by (3), in Cuk and Sepic converters the gain of the internal current loop depends strongly on the instantaneous input voltage. A line feedforward action which compensates for the gain variation can be used to improve the input current waveform. This is achieved by modulating the amplitude of the ramp signal (see Fig.1) proportionally to the input voltage.

## VI. Experimental Results

The performances of a Sepic converter as PFP working in CCM with average current mode control were tested on a prototype having the following parameters:

**Table II. Converter Parameters**

| | | |
|---|---|---|
| $V_g$=90÷260$V_{RMS}$ | $V_L$=36V | $P_L$=300W |
| $L_1$=1.44mH | $C_1$=0.68µF | n=0.5 |
| $L_2$=0.255mH | $C_2$=10mF | $f_s$=70KHz |
| $R_d$=82Ω | $C_d$=1µF | |

The control circuit utilizes the SGS-THOMSON L4981 controller.

Fig.8 reports experimental (continuous lines) and theoretical (dotted lines) transfer function $G_{id}(s)$ in the case of $V_g$=90$V_{rms}$ and 50% of rated power, and considering two positions within the line cycle: q=p/2 and q=p/5; the measure was taken with the converter working (without the damping network) as a dc-dc converter supplied by a voltage Ö2$V_g$×sin(q) and with the load given by (6). The good agreement with the theoretical calculation can be noted; observe also the damping introduced by the converter losses.

The different phase behavior at low frequency is due to the effect of the output capacitor which, in the theoretical analysis, was approximated as a short circuit.

In Fig.9 the measure of $G_{id}(s)$ was done in the same conditions but with damping network $R_d$-$C_d$ included. Once again, a good agreement between theoretical (dotted line) and experimental (continuous line) behaviors can be appreciated.

In Fig.10 the rectified input voltage and filtered input current are reported in the case of $V_g$=220$V_{rms}$ and 100%, 50% and 25% of the rated power. Note that the power factor decreases as the load resistance increases, mainly because of the increase of the time interval where the converter works in DCM in which the power stage dc gain is low.

In Fig.11 the power factor for different load condition and for different input voltages is reported. As expected, increasing the input voltage worsens the power factor, especially at low output power. However, in the nominal condition, it is close to unity.

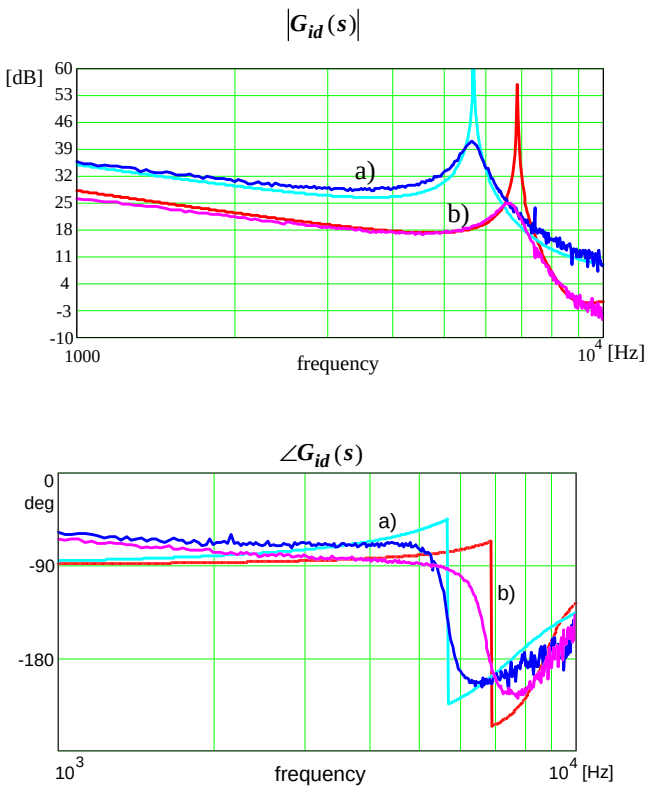


Fig. 8. Comparison between experimental (continuous line) and theoretical (dotted line) amplitude and phase behavior of $G_{id}(s)$ without damping network in different operating conditions: a) q=p/2, b) q=p/5

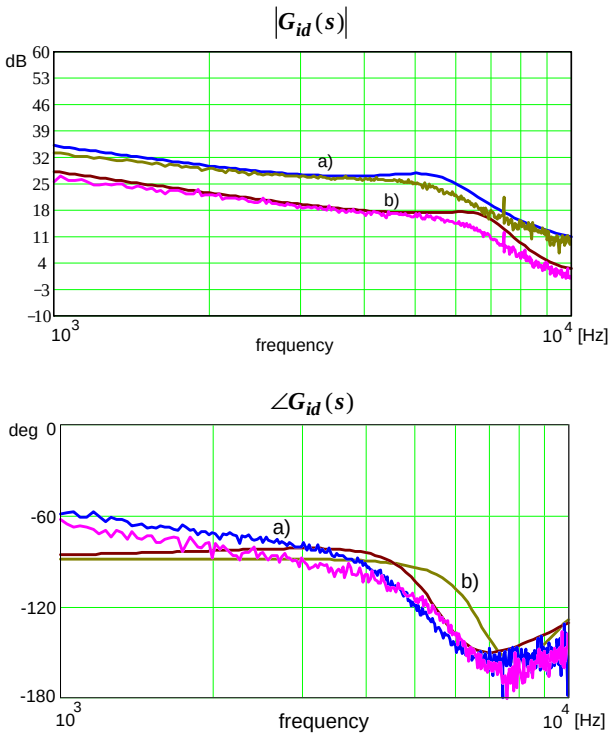


Fig. 9. Comparison between experimental (continuous line) and theoretical (dotted line) amplitude and phase behavior of $G_{id}(s)$ with damping network in different operating conditions: a) q=p/2, b) q=p/5

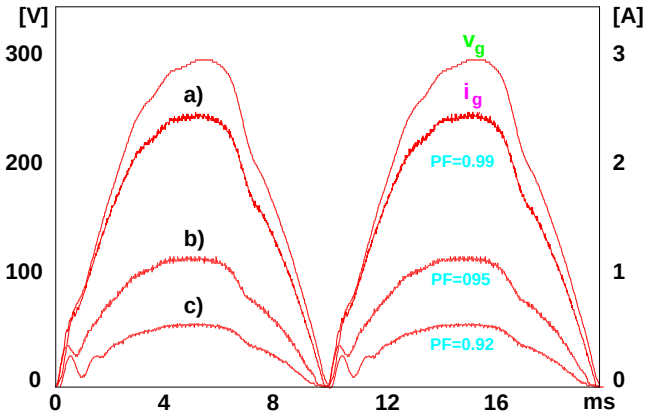


Fig. 10. Rectified input voltage and filtered input current measured at $V_g$=220$V_{rms}$ and different output power: a) 300W, b) 150W, c) 75W. Corresponding power factor is also reported.

## CONCLUSIONS

The application of the average current mode control technique to Sepic and Cuk converters used as power factor preregulators in continuous conduction mode is analyzed.

Since the control-to-output transfer function depends strongly on the instantaneous ac voltage and shows a reduced phase margin, provisions are taken to make possible stabilization in any operating point with a standard PI controller. For this purpose, a suitable damping network is used which, however, does not introduce significant power loss.

Experimental results of a 300W prototype based on Sepic topology confirm the validity of the theoretical approach, and show that almost unity power factor can be achieved with these topologies.

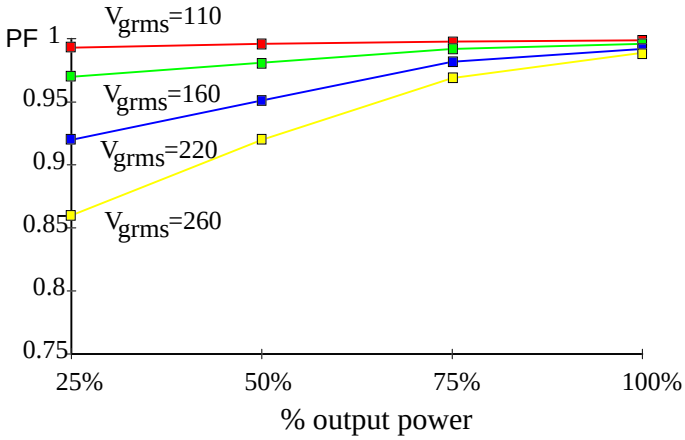


Fig. 11. Converter power factor versus normalized output power for different input voltage values

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