Soft-Commutated Cuk and SEPIC Converters as Power Factor Preregulators

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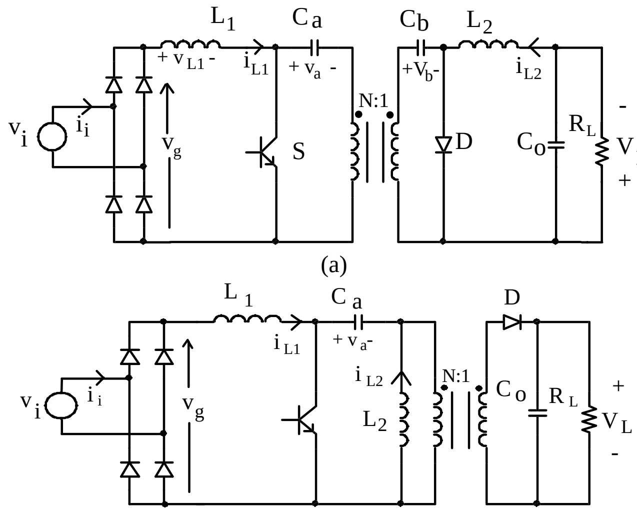
Abstract*[1]*: **Cuk and SEPIC converters operating in Discontinuous Current Mode (DCM), used as Power Factor Preregulators (PFP), present some advantages over other topologies: sinusoidal current shaping using constant frequency and duty-cycle, low input current harmonic content, low input filter requirements, isolation between line and load, etc. The main drawbacks are the voltage and current stresses that devices are submitted to. In this paper, an auxiliary circuit is proposed which limits the overvoltage on the main switch and allows its zero-voltage turn off. Zero-current turn on is provided by the DCM operation. In this way switch commutations are soft, thus improving efficiency and reducing RF noise. Design criteria and experimental results are reported.**

INTRODUCTION

Recently, power converters with high power factor and sinusoidal input current have gained considerable attention, due to international standards regarding the line pollution. Various topologies can be used to perform this task, the most diffused being the boost one. When output isolation is required as well as over-current and start-up protection, Cuk and SEPIC converters are good solutions. Moreover, when operating in Discontinuous Current Mode (DCM) [1-3], they offer other advantages: low harmonic input current without filtering, operation at constant frequency and duty-cycle, no need of current loop, soft turn-on of the main switch. The main drawbacks are the high current and voltage stresses on the switches. Voltage stresses can be further worsened by the effects of transformer leakage inductance, calling for devices with high-voltage capability. IGBTs can be used, which have less forward voltage drop and are cheaper than MOSFETs. But, because of the turn-off tail current, higher commutation losses can be expected, which limit the switching frequency.

In [4], a lossless clamper circuit was used in order to limit the overvoltage due to the transformer leakage inductance. Here, an improved auxiliary circuit is presented, which allows zero-voltage turn-off of the transistor. This means that all commutations are soft, including that of the switches in the auxiliary circuit. The use of soft-switching techniques also limits the RF noise generated, which is a non negligible aspect in preregulators [5].

[1] J. A. Pomilio is doing a post-doctoral research at the University of Padova with a fellowship from the Fundação de Amparo à Pesquisa do Estado de São Paulo, Brazil



(a)

(b)

Figure 1. Cuk (a) and SEPIC (b) converters as Power Factor Preregulators

CUK AND SEPIC CONVERTERS AS POWER FACTOR PREREGULATORS

In the following analysis, a switching frequency much higher than the line frequency is considered, so that the averaged signals over a switching period T can be considered in place of the istantaneous quantities, according to the time-averaging approach. Also, only DCM operation is considered.

Cuk converter

The converter shown in figure 1.a is the insulated version of the Cuk converter driven by a rectified sinusoidal voltage v_g. All the converter components are rated on the switching frequency basis, except the output capacitor C_o which must be big enough to filter the low frequency ripple, at twice the line frequency, caused by the input power variation when operating as PFP [1]. The capacitor voltages are:

$$v_a(\theta) = v_g(\theta) = |v_i| = V_i \cdot |\sin(\theta)|, \theta = \omega_i t \quad (1)$$

$$V_b = V_L \quad (2)$$

When operating in DCM, the current waveforms of both inductors look as shown in figure 2 [6]. The circuit behavior is as follows: when the switch is turned on, the freewheeling diode is reverse biased and the currents rise linearly (assuming small high-frequency voltage ripple across capacitors). During turn-off interval, both inductor currents decrease until their sum becomes zero, causing the freewheeling diode turn off. After that, they remain constant for the rest of the switching period.

The average input current is given by [2]:

$$\bar{i}_{L1}(\theta) = v_g(\theta) \cdot \frac{\delta^2 \cdot T}{2 \cdot L_e} \tag{3}$$

where T is the switching period and

$$L_e = \frac{N^2 \cdot L_1 \cdot L_2}{L_1 + N^2 \cdot L_2} \tag{4}$$

This relation shows that, for constant switching frequency and duty-cycle, the average input current is proportional to the input voltage, ensuring unity power factor.

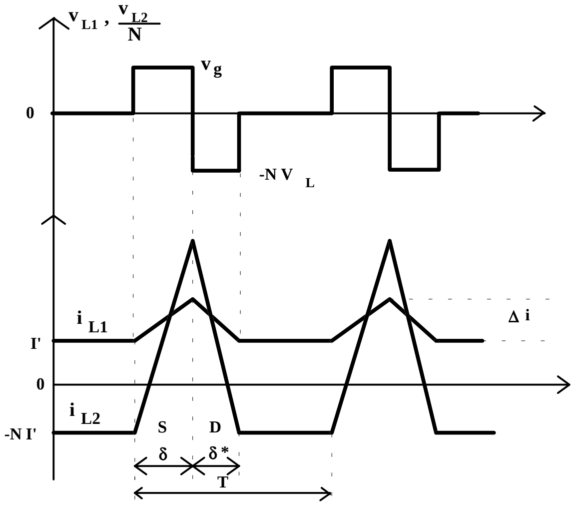


Figure 2. Inductor voltages and currents in DCM for the Cuk converter

Limits for DCM operation. Let us define the following adimensional parameters [1,3,6]:

$$M \equiv \frac{V_L}{V_i} \qquad \textit{Voltage conversion ratio} \tag{5}$$

$$K_e \equiv \frac{2 \cdot L_e}{R_L \cdot T} \tag{6}$$

The converter duty-cycle is given by:

$$\delta = M \cdot \sqrt{2K_e} \tag{7}$$

which shows that, like any other converter operating in DCM, the voltage conversion ratio M depends on the load.

In order to ensure the DCM operation in all conditions, the converter parameters must satisfy the following inequality:

$$K_e < \frac{N^2}{2 \cdot (M \cdot N + 1)^2} \tag{8}$$

Once the value of equivalent inductance L_e is known, from the desired relative input current ripple r_i (peak to peak), the input inductance L_1 is obtained as follows:

$$L_1 = \frac{2L_e}{\delta r_i} \tag{9}$$

With reference to figure 2, it is important to note that current I' must be greater than zero, otherwise the converter operation changes: in fact, current i_{L1} cannot go negative for the presence of the diode bridge. This latter constrain imposes a minimum value for L_1, that is:

$$L_1 > \frac{L_2 \cdot N}{M} \tag{10}$$

SEPIC Converter

For this converter, whose scheme is reported in figure 1.b, the analysis is analogous to the Cuk one, with the difference that the current i_{L2} is not affected by the transformer turns-ratio. The equations are the same except (4), and (10) which become respectively:

$$L_e = \frac{L_1 \cdot L_2}{L_1 + L_2} \tag{11}$$

$$L_1 > \frac{L_2}{M \cdot N} \tag{12}$$

AUXILIARY CIRCUIT FOR SOFT TURN-OFF

In the above PFPs the insulation transformer causes severe voltage spikes and ringing due to its leakage inductance, when the current in the primary side reverses.

Figure 3 shows Cuk and SEPIC converters with the proposed auxiliary circuit, which allows zero-voltage turn-off of the main switch while limiting its overvoltage.

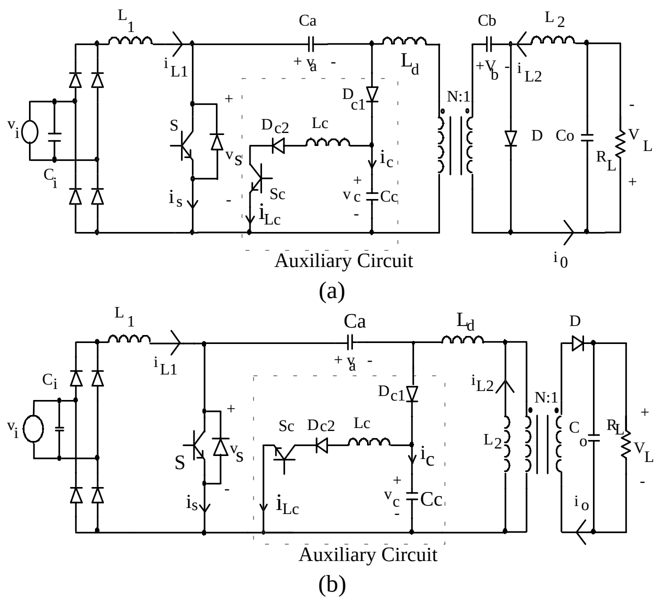


Figure 3. Cuk (a) and SEPIC (b) converters with auxiliary circuit for soft-commutation

Auxiliary circuit behavior

Figure 4 shows the simulated converter waveforms during one switching period. The same driving signal is applied to both switches.

At the end of t_{off} interval, the voltage on C_c is equal to the reflected output voltage plus the overvoltage caused by the transformer leakage inductance. The freewheeling diode D is off. At instant t_0, both switches are turned on under zero-current condition.

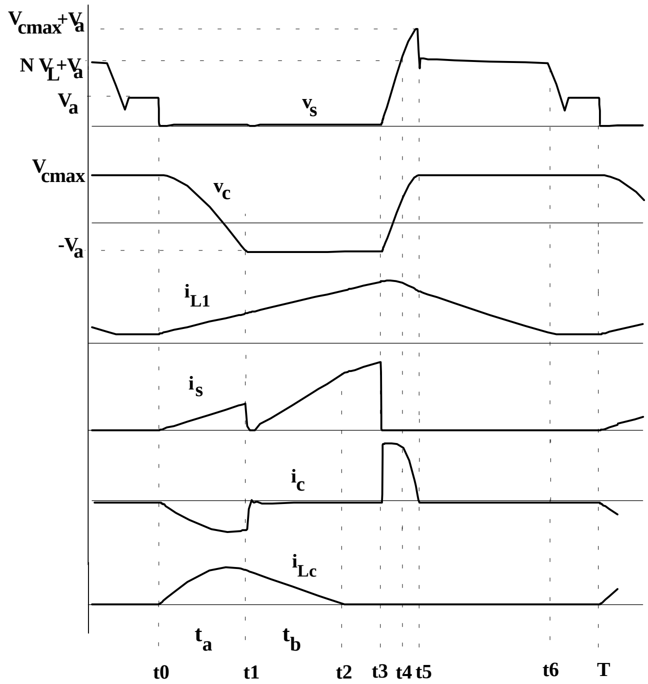


Figure 4. Converter and auxiliary circuit waveforms during a switching period

Interval t_0-t_1. Capacitor C_c starts resonance with inductor L_c. At instant t_1, its voltage reaches the value $-v_a$ and D_{c1} starts conducting.

Interval t_1-t_3. The inductor current i_{Lc} divides between C_a and C_c, flowing almost entirely through S_c, D_{c2}, S, C_a and D_{c1} (C_a>>C_c), and decreases linearly to zero (instant t_2) with a slope equal to $-v_a/L_c$. Note that the auxiliary circuit does not cause increased voltage or current stresses in the main switch. On the contrary, the total current carried by the main switch is lowered.

Interval t_3-t_4. At t_3, the main switch is turned off under zero-voltage condition, and the auxiliary one under zero-current condition. The current flows through D_{c1} to recharge capacitor C_c. As the current during this small interval is almost constant, the voltage varies linearly. When v_c equals the output voltage reflected to the primary side, D starts to conduct (instant t_4).

Interval t_4-t_5. Voltage v_c increases above the reflected output voltage in a resonant manner due to the oscillation between L_d and C_c. The corresponding overvoltage depends on the inductor current value and the characteristic impedance of the resonant circuit. The duration of this interval is one fourth of the resonant period.

Interval t_5-t_6. At t_5, diode D_{c1} stops conduction and current i_{L1} flows through the transformer until the current in the freewheeling diode becomes zero (operation in discontinuous mode).

Interval t_6-T. The output diode opens at zero current. The voltage reflected to the primary becomes zero and the voltage across the main switch drops to v_a.

SELECTION OF AUXILIARY CIRCUIT PARAMETERS

Before to go into detail, let us define the following parameters:

$$\omega_d = \frac{1}{\sqrt{L_d C_c}}, \; Z_d = \sqrt{\frac{L_d}{C_c}}$$

$$\omega_c = \frac{1}{\sqrt{L_c C_c}}, \; Z_c = \sqrt{\frac{L_c}{C_c}}, \; \omega_e = \frac{1}{\sqrt{L_e . C_c}}$$

Capacitor C_c

The value of this capacitor is chosen considering the allowed switch voltage stress. The maximum voltage across C_c, taking into account the effect of transformer leakage inductance, can be estimated as:

$$\hat{V}_c = NV_L + \frac{V_i}{L_e}\delta T \cdot Z_d \qquad (13)$$

Accordingly, the switch voltage stress is:

$$\hat{V}_S \cong V_i + \hat{V}_c \qquad (14)$$

It is important to note that, due to the charging process of C_c, output diode turn on is delayed (interval t_3-t_4). This means an effective increase in the duty-cycle "seen" by the output. The delay increases at light load and near the input voltage zero-crossing. This phenomenon does not affect the converter behavior as power factor preregulator but imposes an upper limit for the value of C_c.

Inductor L_c

Inductance L_c is a critical parameter because it must be chosen in order to allow zeroing of its current during the minimum switches on time, i.e, with reference to figure 4:

$$t_a + t_b < \delta \cdot T \qquad (15)$$

It is not possible to obtain an exact analytical expression for this inductance, but an approximate worst-case result can be obtained. During interval t_a, C_c and L_c resonate until the voltage across C_c reaches $-v_a$. Knowing the voltage $V_{cmax}(\theta)$ across C_c before the switch turn-on, interval t_a is given by:

$$t_a = \frac{1}{\omega_c} \cdot \arccos\left[-\frac{1}{\gamma(\theta)}\right] \qquad (16)$$

where

$$\gamma(\theta) = \frac{V_{c\max}(\theta)}{v_g(\theta)} \qquad (17)$$

At t_1, current i_{Lc} starts to decrease almost linearly to zero under the action of voltage v_a. Thus, we can write:

$$t_b = \frac{L_c \cdot I_o(\theta)}{v_g(\theta)} \qquad (18)$$

where $I_o(\theta)$ is the value of current i_{Lc} in the instant t_1, and is given by:

$$I_o(\theta) = \frac{V_{c\max}(\theta)}{Z_c} \cdot \sin(\omega_c t_1) = \frac{v_g(\theta)}{Z_c} \cdot \sqrt{\gamma(\theta)^2 - 1} \qquad (19)$$

As we can see, in order to find the maximum value of interval t_a+t_b, we must know the behavior of voltage $V_{cmax}(\theta)$. For this purpose note that near the line voltage zero crossing, since both i_{L1} and i_{L2} are low, there is not enough energy to charge C_c to the value NV_L, so no resonance occurs between the transformer leakage inductance and C_c (the output diode does not enter conduction). Thus, we must find the interval, during the line period, in which this situation occurs. The equivalent circuit during interval t_3-t_4 is shown in figure 5.

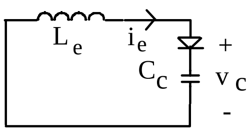


Figure 5. Equivalent circuit at turn off (interval t_3-t_4)

The initial conditions are:

$$i_e(0)=\frac{v_g(\theta)}{L_e}\cdot\delta T,\ \ v_c(0)=-v_g(\theta)$$

Voltage v_c reaches its maximum when i_e zeroes:

$$V_{c\,max}(\theta)=v_g(\theta)\cdot[\delta T\omega_e\cdot\sin(\alpha)-\cos(\alpha)] \quad (20)$$

where $\alpha=\pi+\mathrm{arctg}(-\delta T\omega_e)$.

From the relation

$$V_{c_{MAX}}(\theta_1)=NV_L$$

we find the value of angle θ_1 below which $V_{cmax}(\theta)$ is given by (20):

$$\theta_1=\arcsin\left[\frac{N\cdot V_L}{V_i\cdot[\delta\cdot T\cdot\omega_e\cdot\sin(\alpha)-\cos(\alpha)]}\right] \quad (21)$$

For $\theta_1<\theta<\pi-\theta_1$, the freewheeling diode D starts conduction during the t_{off} interval allowing resonance between L_d and C_c to occur. Note however, that for angles θ slightly greater than θ_1 the overvoltage on C_c is not maximum, since the overshoot is interrupted by the end of turn-off period (interval t_4-t_5 is less then one forth of resonant period). At higher angles, v_c is maximum and is given by:

$$V_{c\,max}(\theta)\cong NV_L+\frac{v_g(\theta)}{L_e}\delta T\cdot Z_d \quad (22)$$

Figure 6 shows typical behavior of voltage V_{cmax}, normalized to the reflected output voltage, versus input voltage angle.

Using these results, the typical variation of interval t_a+t_b, normalized to the duty-cycle, is shown in figure 7. Note that the worst case occurs just after θ_1 (or before $\pi-\theta_1$). This fact suggests a method for estimating L_c, considering that the most critical situation occurs at angle θ_1 and, at this point, there is the total overvoltage across C_c.

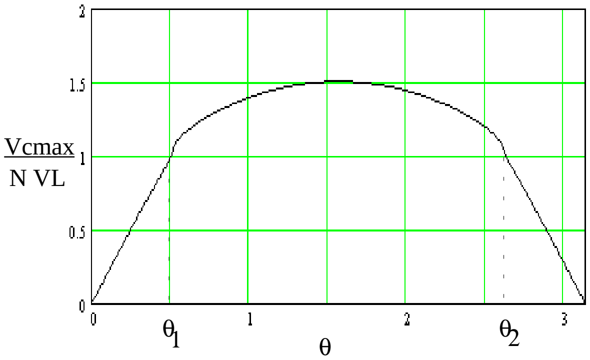


Figure 6. Typical variation of peak voltage across C_c

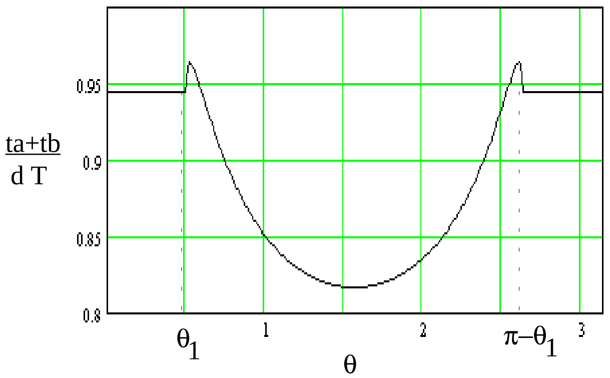


Figure 7. Typical variation of interval t_a+t_b

Thus, using (15÷19) and (22), with the condition $\theta=\theta_1$, the maximum value for the inductance L_c can be approximated by:

$$L_c\cong\frac{\delta^2\cdot T^2}{C_c\cdot\left[\arccos\left(-\frac{1}{\gamma(\theta_1)}\right)+\sqrt{\gamma(\theta_1)^2-1}\right]^2} \quad (23)$$

Note that, there must be a lower limit for the duty-cycle in order to meet condition (15), thus the minimum value of δ must be used in (23).

Zero-Voltage turn-off condition

From the analysis of the auxiliary circuit it is clear that the zero-voltage turn-off condition requires a voltage across C_c always greater than V_a, i.e.:

$$V_{c_{MAX}}\geq v_a(\theta)=v_g(\theta) \quad (24)$$

For $\theta_1<\theta<\pi-\theta_1$ a sufficient condition is that reflected output voltage is higher than maximum input voltage:

$$N\cdot V_L\geq V_i \quad (25)$$

For $\theta<\theta_1$ and $\theta>\pi-\theta_1$, from (20) the condition (24) is satisfied if:

$$\delta T\omega_e\cdot\sin(\alpha)-\cos(\alpha)\geq 1 \quad (26)$$

This condition must be verified once capacitor C_c has been chosen. Taking the equality from (25), we can find the required transformer turns ratio N.

DESIGN PROCEDURE

In the converter design procedure, the following input data are considered:

- peak input voltage V_i
- output voltage V_L
- maximum and minimum load resistance R_{Lmax}, R_{Lmin}
- switching frequency f=1/T
- maximum switch voltage $\hat{V}_S$
- relative input current ripple r_i

Power stage design

In the following, the detailed power stage design procedure is outlined using the results derived in the previous paragraphs.

1) Choose a suitable maximum value for the duty-cycle δ_{max};
2) calculate M from (5);
3) calculate N taking the equality in (25);
4) find the value of K_e from (7) using the minimum load resistance and verify condition (8). If it is not satisfied, a different value for δ_{max} must be chosen;
5) knowing K_e, calculate L_e from (6);
6) calculate L_1 from (9);
7) calculate L_2 from (4);
8) check condition (12); if it is not satisfied, a lower input current ripple must be considered.

Capacitor C_a and C_b are selected taking into account the desired high frequency voltage ripple. As far output capacitor is concerned, it must be rated at line frequency instead of switching frequency. So, given the desired relative voltage ripple r_V (peak to peak), we can write:

$$C_o = \frac{1}{\omega_i r_v R_{L\,min}} \tag{27}$$

Auxiliary circuit design

From the above considerations, the choice of auxiliary circuit parameters can be summarized as follows:

1) from the maximum voltage stress allowed on the switch and (13-14), calculate the value of capacitance C_c and verify inequality (26);
2) calculate the minimum duty-cycle in correspondence of maximum load resistance from (7);
3) calculate θ_1 from (21) at minimum duty-cycle;
4) find the value of parameter $\gamma(\theta_1)$ from (17) and (22);
5) calculate the value of inductance L_c from (23) using the minimum duty-cycle.

EXPERIMENTAL RESULTS

A 250W converter prototype was built according to the following specifications:
$V_i = 120\cdot\sqrt{2}$ V
$V_L = 50$ V
$R_{Lmax} = 62.5\ \Omega$, $R_{Lmin} = 10\ \Omega$,
f = 50kHz (T=20µs)
$\hat{V}_S$ =800V
Input current ripple: 30%

Following the design procedure outlined above, the converter parameters are:

Transformer turns ratio: 5:1
Measured transformer leakage inductance: $L_d = 13\mu H$.
Nominal duty-cycle: $\delta = 0.5$ ($P_o = 250W$)
Minimum duty-cycle: $\delta = 0.2$ ($P_o = 40W$)

$L_1 = 1.9$ mH	$L_2 = 6.2\ \mu H$	$L_c = 30\ \mu H$
$C_a = 500$ nF	$C_b = 50\ \mu F$	
$C_o = 1000\ \mu F$	$C_c = 20$ nF	

Figure 8 shows line current and voltage. The distortion in the current near the zero crossing is due to the limitation imposed by the inductance L_1. As the inductance is relatively high, at low input voltage the current rate of change is limited. Nevertheless a high power factor is obtained. At full power, the measured value is 0.99.

Figure 9 displays the rectifier input current showing its high-frequency components. The expected ripple of 30% is got. The spectrum shows the high-frequency harmonics.

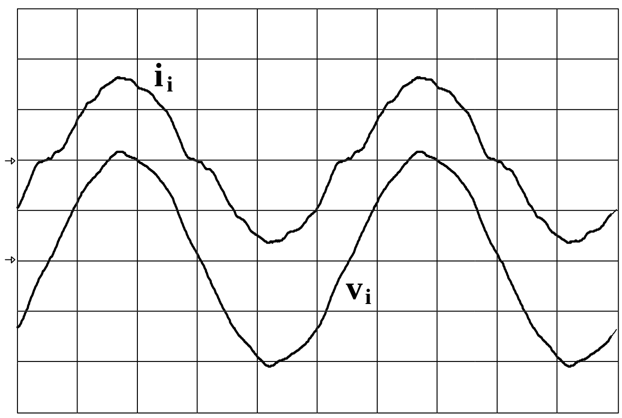


Figure 8. Filtered line current (2A/div) and voltage (100V/div)
Horiz.: 4 ms/div

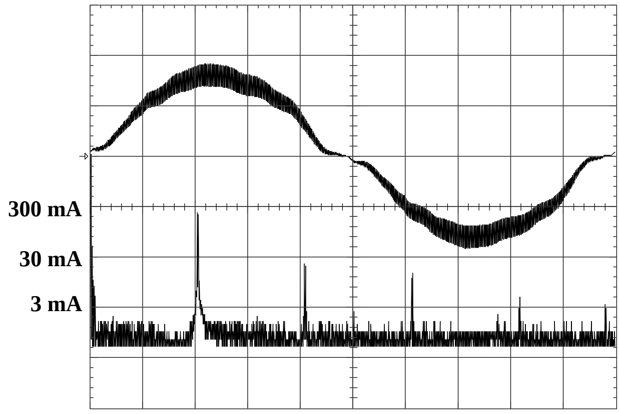


Figure 9. Rectifier input current (2A/div, 2ms/div)) and its spectrum (25 kHz/div)

The next waveforms were taken at the peak of the input voltage, so that they represent the instantaneous highest values of voltage and current through the devices.

Figure 10 shows the behavior of the auxiliary circuit. Note that the charge process happens at constant current and the inversion of the voltage obey a sinusoidal variation.

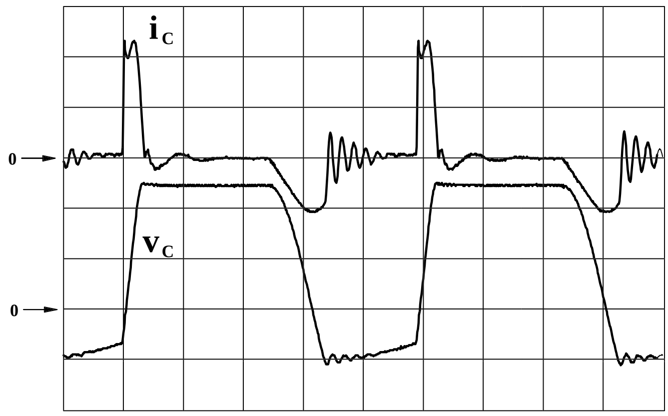


Figure 10. Capacitor C_c current (5 A/div) and voltage (200 V/div).
Horiz.: 4 µs/div

Figure 11 shows the main switch current and voltage waveforms. The zero-current turn-on and zero-voltage turn-off are clear. The IGBT current tail is present and the use of zero-voltage turn-off contributes to reduce the losses [7].

Figure 12 shows the variation of the efficiency and power factor. The measured power factor at minimum load is 0.98 and higher than 0.99 at nominal load. The efficiency is relatively low specially because the high RMS currents present in the secondary side, which increase the resistive losses. Figure 13 reports the calculated converter losses at nominal power: as we can see, the auxiliary circuit losses are 24% of total ones. They weight substantially on the converter efficiency, but it is important to note that they are not proportional to output power. Thus, higher efficiency can be expected at higher power rating

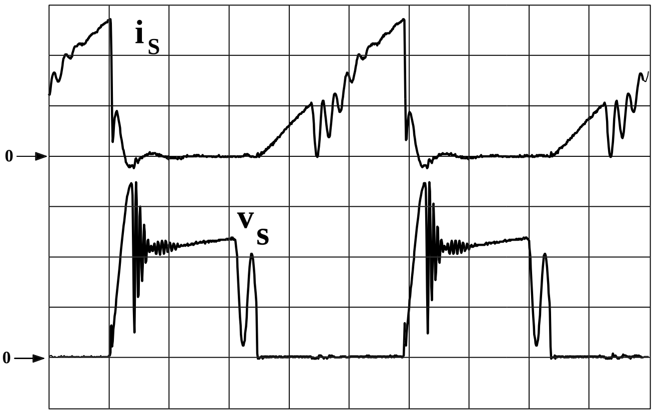


Figure 11. Main switch current (5 A/div) and voltage (200 V/div)
Horiz.: 4µs/div

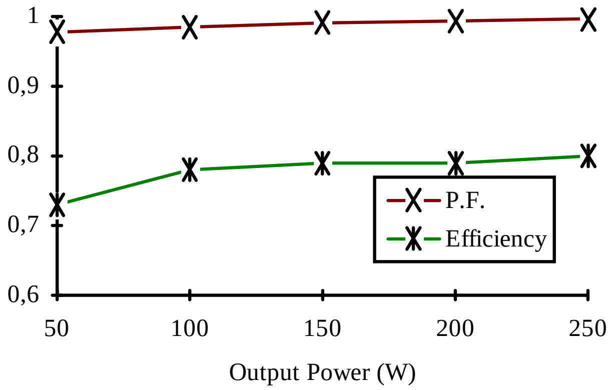


Figure 12. Converter efficiency and power factor vs. output power.

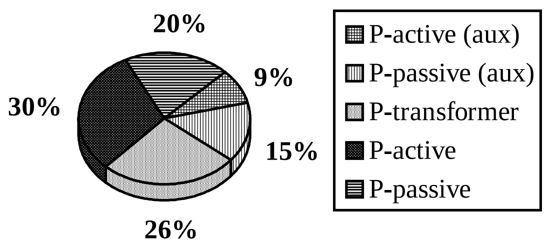


Figure 13. Converter losses distribution

Conclusions

The use of the proposed auxiliary circuit, besides limiting the overvoltage, allows a full soft-commutation converter. A higher switching frequency is therefore possible also with IGBTs, maintaining a reasonably high efficiency. In spite of some low-frequency distortion in the line current, the power factor is next to unity and the current harmonics are small.

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