CONTROL TECHNIQUES FOR POWER FACTOR CORRECTION CONVERTERS

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Abstract. The aspects regarding control strategies for Power Factor Correction (PFC) converters are investigated. The major control techniques to absorb sinusoidal input currents in boost PFC's are reviewed and analyzed.
Their extension to other converter topologies is discussed and some experimental results for a PFC based on the Sepic topology are reported, which allow comparison of converter performance with different control techniques.
Lastly, some considerations regarding dynamic operation are given, together with information about control IC's specifically developed for PFC applications.

Keywords. Power factor correction, control techniques

INTRODUCTION

The attention devoted to the quality of the currents absorbed from the utility line by electronic equipment is increasing due to several reasons. In fact, a low power factor reduces the power available from the utility grid, while a high harmonic distortion of the line current causes EMI problems and cross-interferences, through the line impedance, between different systems connected to the same grid. From this point of view, the standard rectifier employing a diode bridge followed by a filter capacitor gives unacceptable performances. Thus, many efforts are being done to develop interface systems which improve the power factor of standard electronic loads.
An ideal power factor corrector (PFC) should emulate a resistor on the supply side while maintaining a fairly regulated output voltage [1]. In the case of sinusoidal line voltage, this means that the converter must draw a sinusoidal current from the utility; in order to do that, a suitable sinusoidal reference is generally needed and the control objective is to force the input current to follow, as close as possible, this current reference.
The most popular topology in PFC applications is certainly the boost topology, shown in Fig.1 together with a generic controller.

A diode rectifier effects the ac/dc conversion, while the controller operates the switch in such a way to properly shape the input current i_g according to its reference. The output capacitor absorbs the input power pulsation, allowing a small ripple of the output voltage V_L.
The boost topology is very simple and allows low-distorted input currents and almost unity power factor with different control techniques. Moreover, the output capacitor is an efficient energy storage element (due to the high output voltage value) and the ground-connected switch simplifies the drive circuit. The main drawbacks of this topology are: 1) start-up overcurrents, due to the charge of the large output capacitor; 2) lack of current limitation during overload and short circuit conditions, due to the direct connection between line and load; 3) difficult insertion of a high-frequency transformer for insulating the input and output stages; 4) output voltage always greater than peak input voltage.

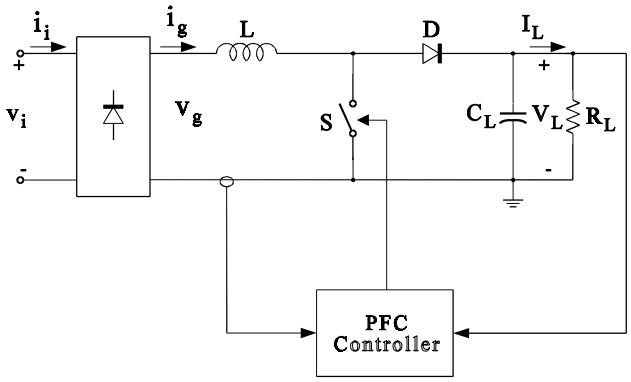

Fig.1 - Principle scheme of a boost PFC

In spite of these limitations, many PFC's based on the boost topology have been proposed in the literature. Various control strategies have also been implemented. In the

following, the most popular control techniques are reviewed and compared, in order to highlight advantages and drawbacks of each solution, also referring to the availability of commercial control IC's.

REVIEW OF PFC CONTROL TECHNIQUES

In the following, we will refer to the boost PFC, even if many of the discussed control techniques can also be used with other topologies.

Peak current control

The basic scheme of the peak current controller is shown in Fig.2, together with a typical input current waveform [2-6].

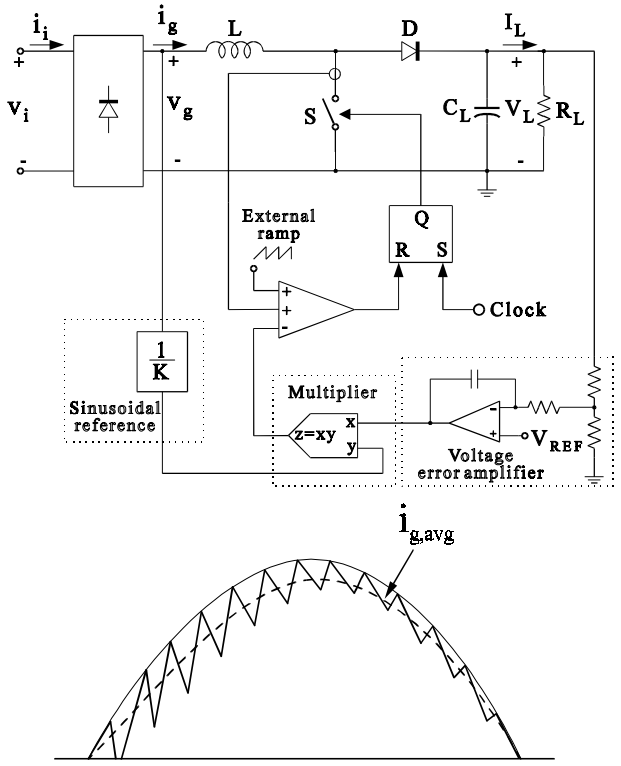

Fig.2 - Peak current control scheme

As we can see, the switch is turned on at constant frequency by a clock signal, and is turned off when the sum of the positive ramp of the inductor current (i.e. the switch current) and an external ramp (compensating ramp) reaches the sinusoidal current reference. This reference is usually obtained by multiplying a scaled replica of the rectified line voltage v_g times the output of the voltage error amplifier, which sets the current reference amplitude. In this way, the reference signal is naturally synchronized and always proportional to the line voltage, which is the condition to obtain unity power factor.

As Fig.2 reveals, the converter operates in Continuous Inductor Current Mode (CICM); this means that devices current stress as well as input filter requirements are reduced. Moreover, with continuous input current, the diodes of the bridge can be slow devices (they operate at line frequency). On the other hand, the hard turn-off of the freewheeling diode increases losses and switching noise, calling for a fast device. Advantages and disadvantages of the solution are summarized hereafter.

Advantages:
- constant switching frequency;
- only the switch current must be sensed and this can be accomplished by a current transformer, thus avoiding the losses due to the sensing resistor;
- no need of current error amplifier and its compensation network;
- possibility of a true switch current limiting.

Disadvantages:
- presence of subharmonic oscillations at duty cycles greater than 50%, so a compensation ramp is needed;
- input current distortion which increases at high line voltages and light load and is worsened by the presence of the compensation ramp [4-5];
- control more sensitive to commutation noises.

The input current distortion can be reduced by changing the current reference waveshape, for example introducing a dc offset, and/or by introducing a soft clamp. These provisions are discussed in [4] and [5]. In [6] it is shown that even with constant current reference, good input current waveforms can be achieved. Moreover, if the PFC is not intended for universal input operation, the duty-cycle can be kept below 50% so avoiding also the compensation ramp.

Available commercial IC's for the peak current control are the ML4812 (Micro Linear) [3] and TK84812 (Toko).

Average current control

Another control method, which allows a better input current waveform, is the average current control represented in Fig.3 [4,7-10]. Here the inductor current is sensed and filtered by a current error amplifier whose output drives a PWM modulator. In this way the inner current loop tends to minimize the error between the average input current i_g and its reference. This latter is obtained in the same way as in the peak current control.

The converter works in CICM, so the same considerations done with regard to the peak current control can be applied.

Advantages:
- constant switching frequency;
- no need of compensation ramp;
- control is less sensitive to commutation noises, due to current filtering;
- better input current waveforms than for the peak current control since, near the zero crossing of the line voltage, the duty cycle is close to one, so reducing the dead angle in the input current [4].

Disadvantages:
- inductor current must be sensed;

- a current error amplifier is needed and its conpensation network design must take into account the different converter operating points during the line cycle.

This control technique is becoming very popular and detailed design criteria can be found in [4,7,8,10]. Many control IC's are available from different manufacturers: UC1854/A/B family (Unitrode) [7,10,12], UC1855 (Unitrode) [11], TK3854A (Toko), ML4821 (Micro Linear), TDA4815, TDA4819 (Siemens), TA8310 (Toshiba), L4981A/B (SGS-Thomson) [13], LT1248 [14], LT1249 [15] (Linear Technology).

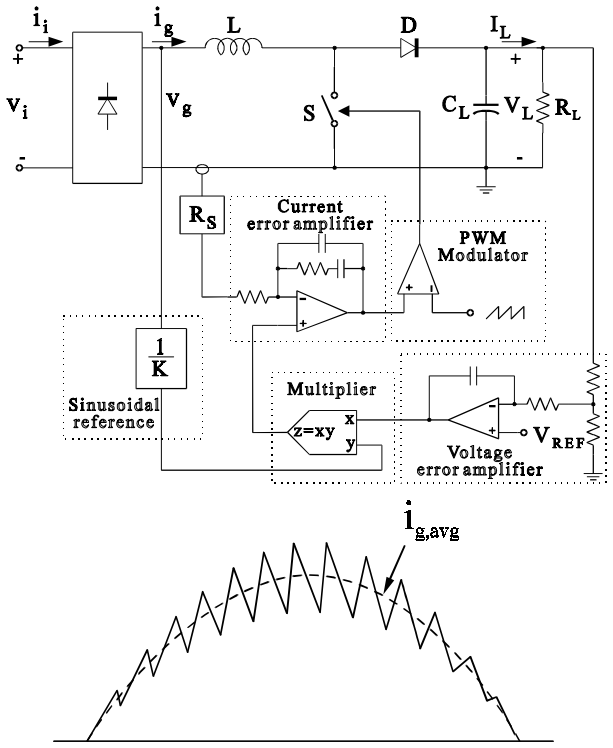

Fig.3 - Average current control scheme

Hysteresis control

Fig.4 shows this type of control in which two sinusoidal current references $I_{P,ref}$, $I_{V,ref}$ are generated, one for the peak and the other for the valley of the inductor current. According to this control technique, the switch is turned on when the inductor current goes below the lower reference $I_{V,ref}$ and is turned off when the inductor current goes above the upper reference $I_{P,ref}$, giving rise to a variable frequency control [16-18].

Also with this control technique the converter works in CICM.

Advantages:

- no need of compensation ramp;
- low distorted input current waveforms.

Disadvantages:

- variable switching frequency;
- inductor current must be sensed;
- control sensitive to commutation noises.

In order to avoid too high switching frequency, the switch can be kept open near the zero crossing of the line voltage so introducing dead times in the line current. An analysis of the power factor as a function of these dead times can be found in [16,17]. A control IC which implements this control technique is the CS3810 (Cherry Semiconductor) [19].

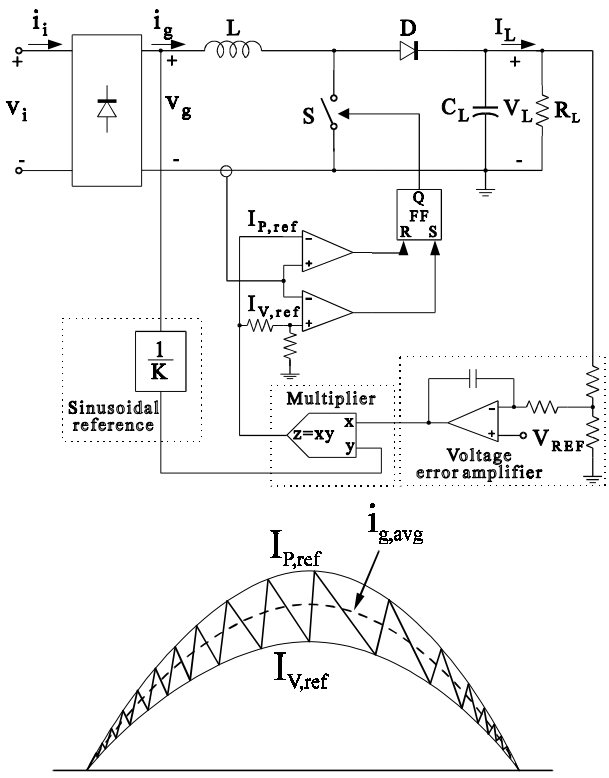

Fig.4 - Hysteresis control scheme

Borderline control

In this control approach the switch on-time is held constant during the line cycle and the switch is turned on when the inductor current falls to zero, so that the converter operates at the boundary between Continuous and Discontinuous Inductor Current Mode (CICM-DICM) [20]. In this way, the freewheeling diode is turned off softly (no recovery losses) and the switch is turned on at zero current, so the commutation losses are reduced. On the other hand the higher current peaks increase device stresses and conduction losses and may call for heavier input filters (for some topologies).

This type of control is a particular case of hysteretic control in which the lower reference $I_{V,ref}$ is zero anywhere.

The principle scheme is shown in Fig.5. The instantaneous input current is constituted by a sequence of triangles whose peaks are proportional to the line voltage. Thus, the average input current becomes proportional to the line voltage without duty-cycle modulation during the line cycle. This characterizes this control as an "*automatic current shaper*" technique.

Note that the same control strategy can be generated, without using a multiplier, by modulating the switch

on-time duration according to the output signal of the voltage error amplifier. In this case switch current sensing can be eliminated.

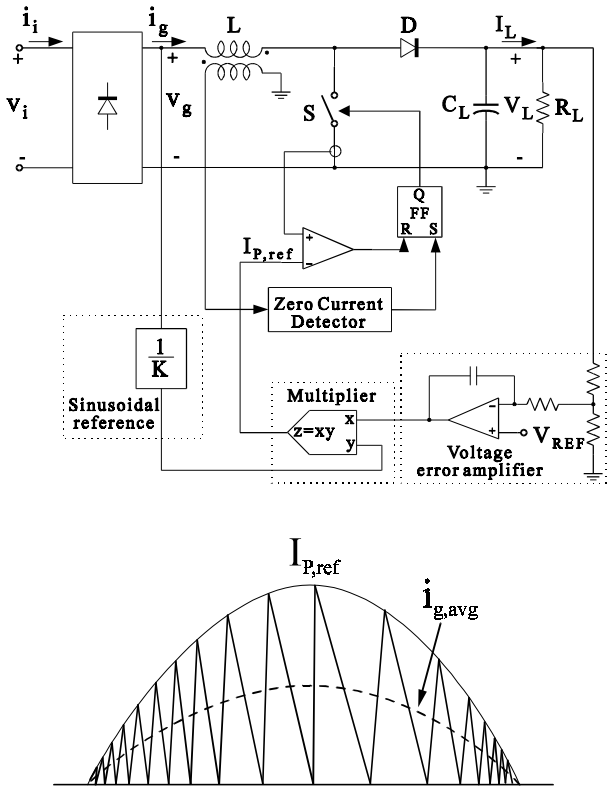

Fig.5 - Borderline control scheme

Advantages:
- no need of a compensation ramp;
- no need of a current error amplifier.
- for controllers using switch current sensing, switch current limitation can be introduced;

Disadvantages:
- variable switching frequency;
- inductor voltage must be sensed in order to detect the zeroing of the inductor current;
- for controllers in which the switch current is sensed, control is sensitive to commutation noises.

Specific control IC's are: TDA4814, TDA4816, TDA4817, TDA4818 (Siemens), SG3561 (Silicon General), UC1852 (Unitrode) [12], MC33261, MC33262 (Motorola), L6560 (SGS-Thomson) [13].

Discontinuous current PWM control

With this approach, the internal current loop is completely eliminated, so that the switch is operated at constant on-time and frequency (see Fig.6) [21-27]. With the converter working in *discontinuous conduction mode* (DCM), this control technique allows unity power factor when used with converter topologies like flyback, Cuk and Sepic. Instead, with the boost PFC this technique causes some harmonic distortion in the line current [24].

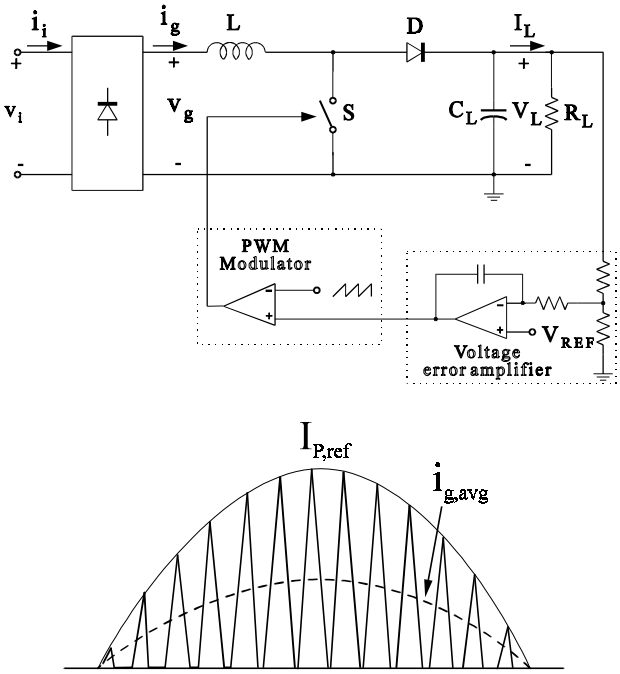

Fig.6 - Discontinuous current PWM control scheme

Advantages:
- constant switching frequency;
- no need of current sensing;
- simple PWM control;

Disadvantages:
- higher devices current stress than for borderline control;
- input current distortion with boost topology.

A control IC specifically developed for this type of control is the ML4813 (Micro Linear) [22]. Note, however, that every PWM controller for dc/dc converters can be used to perform this control.

EXTENSION TO OTHER PFC TOPOLOGIES

Although boost PFC's are the most diffused, other converters like flyback, Cuk and Sepic are well suited for PFC applications. All of these overcome some of the problems encountered with the boost topology: for example, they allow high-frequency insulation, voltage step-up and step-down as well as start-up and overload protection. For these converters, some of the above control techniques have been proposed, with proper modifications to suit the different topology characteristics. We will first analyze the flyback PFC, which is the simplest solution for isolated converters, and then Cuk and Sepic structures.

Flyback PFC

The first control strategy proposed for this converter was the *Discontinuous current PWM control* [21-23]. According to this technique, the converter draws a sinusoidal current with no need of duty-cycle modulation, i.e. at constant on-time and switching frequency. This very

simple approach is convenient for low-power applications, while for medium power levels it is better to operate the converter in *continuous conduction mode* (CCM), thus reducing the current stresses in the switch. For this purpose, the so called *Charge Control* can be used, which is illustrated in Fig.7 [28].

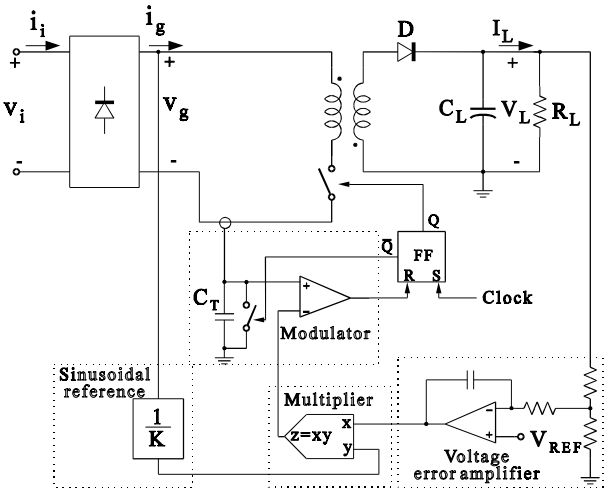

Fig.7 - PFC flyback converter with charge control

With this technique, the switch is turned on at constant frequency by a clock signal. Then, the choppered input current i_g is sensed and integrated by capacitor C_T. When the voltage across C_T, which is proportional to the charge fed by the input generator in a switching period, reaches the sinusoidal reference, the switch is turned off and capacitor C_T is reset in order to be ready for the next commutation cycle. In this way, the average input current is forced to follow the sinusoidal reference even if the converter works in CCM. With this control, subharmonic oscillations can appear, depending on line and load conditions. To get rid of them a suitable compensating ramp must be added, which however increases the input current distortion. In [28] no external ramp was used, but a higher value of the magnetizing inductance was chosen in order to reduce to a negligible value the time interval in which the subharmonic oscillations appear.

Cuk and Sepic PFC

These topologies are less popular as PFC due to their higher complexity as compared to boost or flyback structures. Like the flyback converter, they draw a sinusoidal input current, when working in DCM, with no need of duty-cycle modulation [25-27]. In this case the simple *discontinuous current PWM control* can be profitably applied as shown in Fig.8. With these converters, however, input current can be continuous even in DCM [25], which happens when the freewheeling diode current, which is the sum of the two inductor currents, zeroes. With a proper choice of the two inducance values, the input inductor current can be continuous even if the diode current is discontinuous. This reduces the input filter requirements, but the high current stresses on the devices remain.

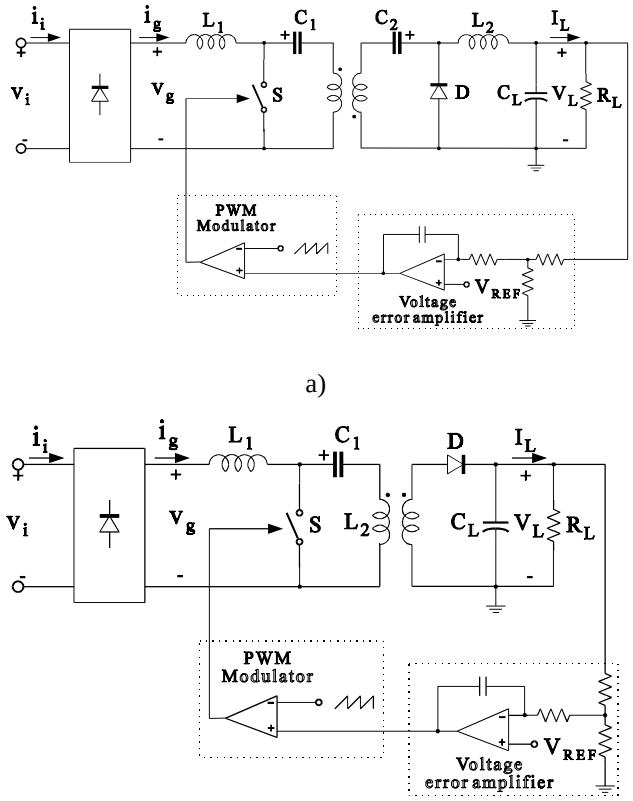

Fig.8 - a) PFC Cuk converter, and b) PFC Sepic converter with discontinuous current PWM control

The input current ripple can be further decreased by exploiting another feature of Cuk and Sepic topologies, i.e. the possibility to magnetically couple the two inductors [26,27]. In this way, the two inductors can be wound on the same magnetic core reducing size and cost and, by a proper choice of the magnetic structure parameters, the high frequency current ripple can be "steered" from one winding to the other.

Observing that the input stages of Cuk and Sepic converters resemble that of a boost one, it seems natural to apply other control techniques initially developed for boost PFC's. In particular, for medium- and high-power applications, CCM is more convenient and the average current control seems attractive for its good performances. The problem is the design of a large-bandwidth internal current loop in order to obtain low-distorted input current. It is shown in [29], that, differently from the boost converter, with Sepic and Cuk topologies the gain of the power stage depends strongly on instantaneous input voltage, and the presence of undamped complex poles and zeroes makes difficult the design of a stable control. To overcome these problems, a suitable damping network is needed, which properly shapes the current loop transfer function without introducing significant losses [29]. With this provision, a standard PI controller in the current loop

ensures the desired phase margin in any operating condition.

CONSIDERATIONS ON PFC DYNAMIC RESPONSE

As previously mentioned, the sinusoidal input waveform of a single-phase PFC causes an input power fluctuation which, in all the mentioned topologies, is absorbed by the output filter capacitor. Consequently, the output voltage contains a ripple term at twice the line frequency, which is going to affect the input current waveform if the output voltage loop has not a band well below the line frequency (typically 20Hz) [30,31]. For this reason, the response of the output voltage to line and load transients is poor. In [32] various modifications of the basic voltage loop are proposed to overcome this problem: in particular the use of notch filters, sampling networks and the so called "regulation band approach" are proposed in order to remove the low frequency output voltage ripple from the feedback signal.

A completely different approach was followed in [33] where a ripple-feedback cancellation scheme was employed to speed up the controller at the expense of a much greater control complexity (need of knowledge of output power and output capacitor value and additional computations).

The response speed to line variations may also be affected by the way in which the current reference is obtained. In fact, when the peak input voltage increases, the peak input current should decrease in order to draw constant power; if the sinusoidal shape is obtained directly from the rectified input voltage as said before, the reference signal moves in the wrong direction when the line voltage changes, calling for a heavy compensating action by the voltage error amplifier. The most common solution to this problem consists in a feedforward action from the input voltage, as shown in Fig.9.

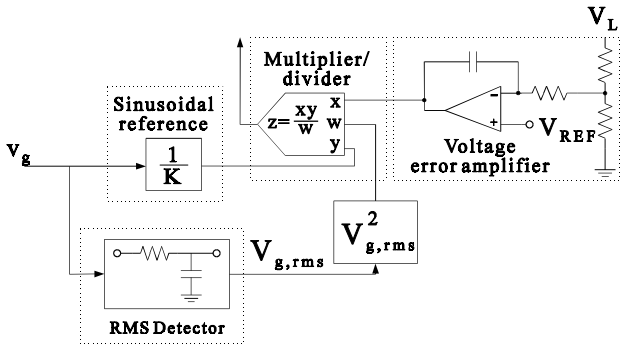

Fig.9 - Line feedforward

Here, a simple low pass filter provides a voltage proportional to the RMS input voltage; this signal is then squared and used in the multiplier to divide the current reference. This compensates for input voltage transients, even if the feedforward action is not instantaneous due to the low pass filtering.

In the same way a feedforward action from the output load can speed up the dynamic behavior during load transients. For this purpose, it is sufficient to multiply the current reference by a signal proportional to the load current.

A valuable approach to improve the converter dynamic performance is given by the sliding-mode control. In [34] this control technique was applied to a high-quality rectifier based on the Cuk topology, resulting in a good trade-off between the needs for increasing response speed and reducing input current distortion and output voltage ripple.

In Fig.10, the principle scheme of the converter is shown. The sliding-mode control, acts in such a way to keep close to zero, by an hysteresis control, a function ψ which is a linear combination of input current and output voltage errors ε_i, ε_u. Thus, the relative value of the two coefficients K_i and K_u determines which variable (input current or output voltage) is more tightly regulated.

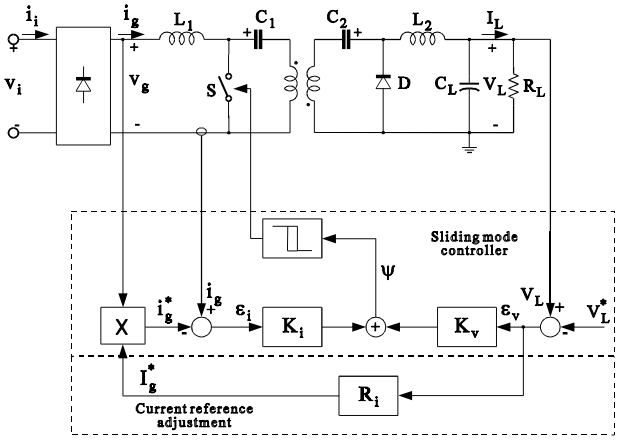

Fig.10 - Scheme of the high-quality rectifier Cuk converter with sliding mode control

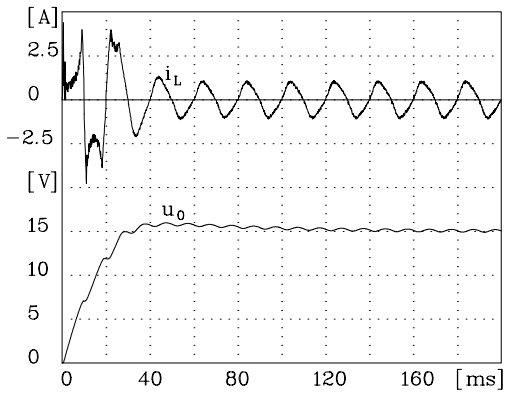

Fig.11 - Line current and output voltage at start-up for the sliding-mode controlled Cuk converter

As an example of converter dynamic behavior, Fig.11 reports line current and output voltage at start-up: the current distortion during the transient, caused by the high error voltage ε_u, is the price for the faster output dynamic, but, in the steady state, a good current waveform is achieved.

CONTROL IC's

In table I commercially available control IC's for PFC applications are summarized [35]. Some of the recent average current control IC's include line voltage feedforward (UC1854/A/B family, UC1855, L4981/A/B) and load feedforward (L4981/A/B).

Tab. 1. Power Factor Controller IC's

Constant frequency peak current control	ML4812 (Micro Linear) TK84812 (Toko)
Constant frequency average current control	UC1854/A/B family (Unitrode) UC1855 (Unitrode) TK3854A (Toko) ML4821 (Micro Linear) TDA4815, TDA4819 (Siemens) TA8310 (Toshiba) L4981A/B (SGS-Thomson) LT1248, LT1249 (Linear Tech.)
Hysteretic control	CS3810 (Cherry Semic.)
Borderline control	TDA4814, TDA4816, TDA4817, TDA4818 (Siemens) SG3561 (Silicon General) UC1852 (Unitrode) MC33261, MC33262(Motorola) L6560 (SGS-Thomson)
Two stage PFC with average-current control	UC1891/2/3/4 family (Unitrode) TK65030 (Toko)
Two stage PFC with peak-current control	ML4819 (Micro Linear) TK84819 (Toko)
Buck-boost constant frequency automatic control	ML4813 (Micro Linear)

As far as the borderline control is concerned, the TDA4816, L6560, MC34261 control IC's employ a multiplier to provide the upper current reference as shown in Fig.5, while the UC1852 has an adjustable switch on-time and therefore does not need switch current detection.

EXPERIMENTAL RESULTS

In the following, experimental results taken on two PFC Sepic converters are reported, one with *discontinuous current PWM control* and the other with *average current control*. The first prototype, rated at 100W, employs the magnetic coupling concept to reduce the input current ripple [27]. Fig.12 reports the waveforms of rectified line voltage and current. In spite of some low frequency oscillation on the input current, due to the resonance between the energy transfer capacitor C_1 and the two inductances, the power factor is close to unity at nominal conditions and decreases for high line voltages and light load currents, as shown in Fig.13.

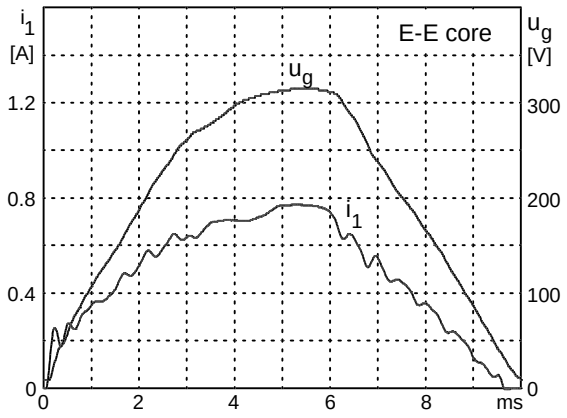

Fig.12 - Rectified input voltage and filtered input current of the PFC Sepic converter in DCM (rated conditions)

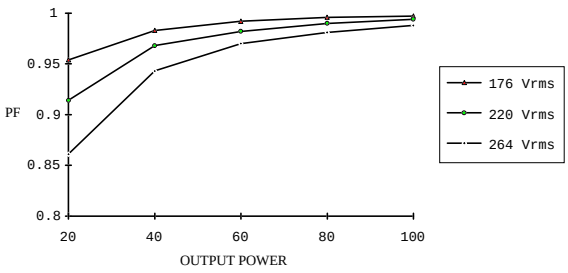

Fig.13 - Power factor vs. output power for different input voltage values

The second prototype, working in CCM with average current control, was rated at 300W [29]. Fig.14 reports the waveforms of rectified line voltage and current, at different load conditions. The input current waveform is less distorted than in the previous case. Accordingly, the power factor increases. This latter, is also reported in Fig.15 as function of output power and input voltage.

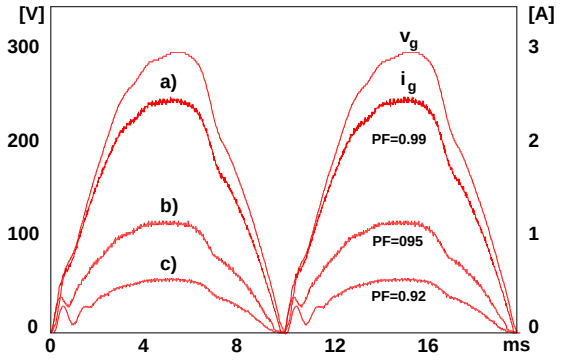

Fig. 14. Rectified input voltage and filtered input current of the PFC Sepic in CCM measured at V_g=220V_{rms} and different output power: a) 300W, b) 150W, c) 75W. (Corresponding power factor is also indicated)

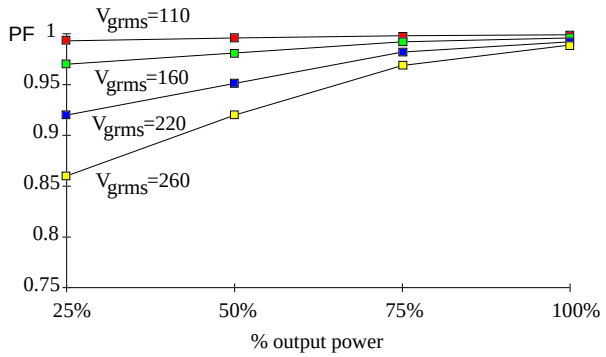

Fig.15. Power factor vs. normalized output power for different input voltage values

CONCLUSIONS

In this paper, several control techniques specifically developed for PFC boost converters are analyzed. For each control strategy advantages and drawbacks are highlighted and information on available commercial IC's is given.
Extension of these control techniques to other PFC topologies are discussed and some experimental results based on a PFC Sepic converter with different control methods are reported.
Lastly, considerations regarding the PFC dynamic response are given.

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