HIGH-QUALITY RECTIFIER BASED ON CUK CONVERTER IN DISCONTINUOUS CAPACITOR VOLTAGE MODE

G. Spiazzi*, L. Rossetto**, P. Mattavelli**, S. Buso*

*Dept. of Electronics and Informatics, **Dept. of Electrical Engineering

University of Padova - ITALY

Abstract. Cuk converters, operating in Discontinuous Capacitor Voltage Mode (DCVM), can achieve unity power factor when used as rectifiers with no need of duty-cycle modulation.
This operating mode causes high voltage stresses across the semiconductors, calling for high-voltage switches like IGBT's. However, zero-voltage turn-off is achieved, resulting in limited power loss even at high frequency.
Both current- and voltage-fed approaches as well as constant- and variable-frequency control are analysed in the paper.
Simulated and experimental results are reported, which demonstrate actual converter performance.

Keywords. Power factor correction, Cuk converter, rectifier.

INTRODUCTION

Several efforts are being done in order to reduce the impact of conventional rectifiers on the grid in terms of power factor and current harmonics. For this purpose, standard topologies like Boost and Flyback are widely used. Other converter topologies, like Cuk and Sepic, are also gaining attention due to their characteristics: high-frequency insulation, inherent short-circuit protection, step-up and step-down regulation, reduction of input current ripple by inductor coupling. These latter structures have different operating modes, some of which are well suited for the use as Power Factor Pre regulators (PFP's) as shown by Simonetti at al. (1), Brkovic and Cuk (2), Spiazzi and Rossetto (3).
In this paper, high-quality rectifiers based on Cuk converters working in Discontinuous Capacitor Voltage Mode (DCVM) are analysed. This operating mode feautures: unity power factor at constant duty cycle and switching frequency; zero-voltage switching at turn-off and reduction of reactive element values.
The converter is first analysed with inductive output filter (current-fed approach, Freeland (4)) and power stage design criteria are given. It is shown that the use of variable frequency control overcomes the problem of limited load range.
Then, the same converter with capacitive output filter (voltage-fed approach (4)) is considered, showing that almost unity power factor can be achieved also in this case.
Due to high voltage stresses and associated reverse recovery of the freewheeling diode this approach is appealing only for low-voltage applications. Note, however, that high voltage devices like IGBT's can be profitably used at high frequency due to the soft commutation.

BASIC CONVERTER OPERATION

Let us consider the dc-dc Cuk converter operating in DCVM shown in figure 1. Its main waveforms are reported in figure 2 and are drawn in the hypothesis of negligible ripples on inductor currents and output capacitor voltage. As we can see looking at voltage U_1 across energy transfer capacitor C_1, this operating mode requires that, at every switching cycle, capacitor C_1 is discharged to zero by the output inductor current. The switching period is divided in three intervals D_1T_s, D_2T_s, D_3T_s. During the first one, the switch is on while the diode is still off and C_1 is discharged by current I_2. During D_2T_s both switch and diode are on and C_1 is short-circuited until the switch is turned off, starting the recharging phase (interval D_3T_s). Note that the switch turn off occurs at zero voltage.
The following relations hold:

$$\begin{aligned} D_1 + D_2 &= D \\ D_3 &= 1 - D \end{aligned} \qquad (1)$$

where D is the duty-cycle.
From the voltage balance across L_2 and the current balance in C_1 we can write respectively:

$$D_1 \hat{U}_1 = 2U_L \qquad (2)$$

$$I_2 D_1 = I_1 D_3 \qquad (3)$$

The peak voltage in C_1 is given by:

$$\hat{U}_1 = \frac{I_1}{C_1} D_3 T_s \qquad (4)$$

Substituting (3) and (4) in (2) and using the power balance condition (efficiency is assumed unity), the voltage conversion ratio M results:

$$M = \frac{U_L}{U_g} = \frac{1}{1-D} \cdot \sqrt{\frac{2C_1 R_L}{T_s}} \qquad (5)$$

As for any converter operating in discontinuous mode, the voltage conversion ratio depends on the load resistance. The square root dependence on R_L allows use of this topology as "automatic current shaper" when employed as a rectifier (see (4)). This means that a sinusoidal input current can be achieved without duty cycle modulation along the line period.

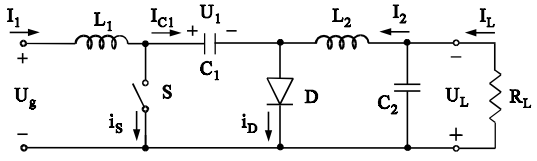

Figure 1: Dc-dc Cuk converter scheme

Using voltage-balance condition across L_1, maximum voltage $\hat{U}_1$ across C_1 can be rewritten as:

$$\hat{U}_1 = \frac{2U_g}{1-D} \tag{6}$$

This equation shows that this operating mode causes high voltage stress across the devices.

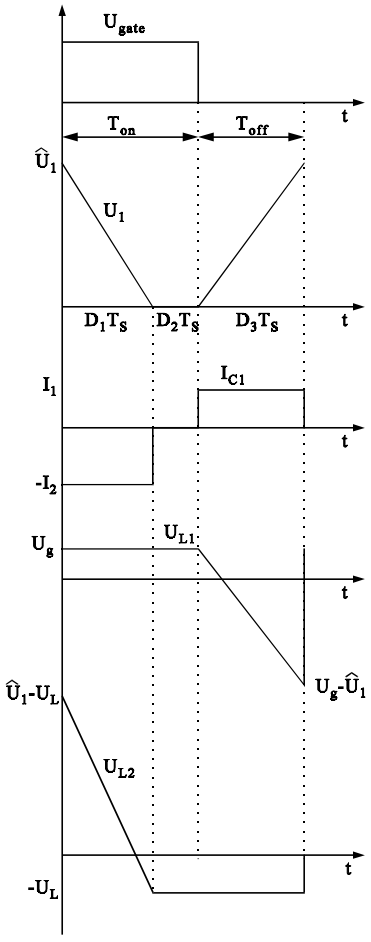

Figure 2: Converter main waveforms in DCVM

DCVM operation is ensured by the condition:

$$D_1 < D \tag{7}$$

which, using (3), (4) and (6) implies:

$$C_1 \le C_{1\lim} = D(1-D)\frac{I_L T_s}{2U_g} \tag{8}$$

This equation reveals that this operating mode can be maintained only for a limited load range.

OPERATION AS PFP: INDUCTIVE FILTER

When operating as a power factor preregulator, the converter is fed by the AC line through a diode bridge rectifier. Moreover, due to the input power pulsating at twice the line frequency, there must be a reactive element capable to filter out this low-frequency fluctuation in order to allow constant output power.

We consider first the case in which the output inductor L_2 is made large enough to maintain a constant output current $I_2=I_L$, as shown in figure 3 (current-fed approach (4)).

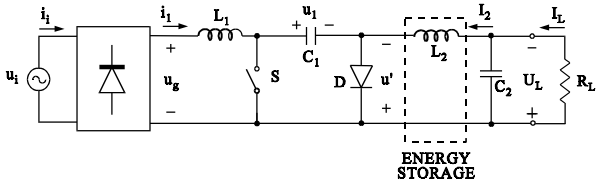

Figure 3: Ac-dc Cuk converter with inductive filter

Assuming unity power factor, the rectified input voltage and current are given by:

$$u_g(\theta) = U_g\left|\sin(\theta)\right| \tag{9.a}$$

$$i_1(\theta) = I_1\sin(\theta) = \frac{2P_L}{U_g}\left|\sin(\theta)\right| \tag{9.b}$$

where $\theta=\omega_l t$ is the angolar line frequency and P_L is the output power. All converter currents and voltages are averaged in a switching period. Under the assumption that the input power fluctuation is fully absorbed by inductor L_2 we can write:

$$u_g(\theta)\cdot i_1(\theta) = u'(\theta)\cdot I_2 \Rightarrow u'(\theta) = 2U_L\sin^2(\theta) \tag{10}$$

Thus the converter operates with an apparent voltage conversion ratio m(θ) given by:

$$m(\theta) = \frac{u'(\theta)}{u_g(\theta)} = \frac{2U_L}{U_g}\left|\sin(\theta)\right| \tag{11}$$

and feds an apparent load r(θ) given by:

$$r(\theta) = \frac{u'(\theta)}{I_2} = 2R_L\sin^2(\theta) \tag{12}$$

The effective voltage conversion ratio $M=U_L/U_g$ can now be derived by substituting in (5) the expressions (11) and (12) in place of M and R_L respectively, obtaining:

$$M = \frac{U_L}{U_g} = \frac{1}{1-D}\cdot\sqrt{\frac{C_1 R_L}{T_s}} \tag{13}$$

Peak voltage stress $\hat{U}_1$ given by (6) and the DCVM condition (8) remain valid provided that U_g represents the peak line voltage.

Power stage design criteria

This section embodies some considerations for a preliminary converter design.

Taking the maximum allowed voltage stress $\hat{U}_{1max}$ as specification the corresponding maximum load variation is derived. For the sake of generality, let us consider that U_g can vary from a minimum value U_{gmin} and a maximum value

U_{gmax}. From (13) it turns out that the maximum duty-cycle corresponds to the situation with minimum input voltage and load resistance and vice-versa. It is also easy to demonstrate that maximum voltage stress $\hat{U}_{1max}$ occurs at the minimum input voltage and hence maximum duty-cycle, while the worst-case condition for C_1 corresponds to the maximum input voltage and load resistance.

Capacitor C_1. Using (6) and (13) we derive the following constraint on C_1 value:

$$C_1 \geq \frac{4T_s}{R_{L\,min}} \cdot \left(\frac{U_L}{\hat{U}_{1max}} \right)^2 = 4T_s \cdot \frac{P_L}{\hat{U}_{1max}^2} \qquad (14)$$

where P_L is the maximum output power.

Maximum load variation. In order to satisfy both constraints (8) and (14) it must be:

$$D_{min} \sqrt{\frac{R_{L\,min}}{R_{L\,max}}} \geq \frac{4U_L}{\hat{U}_{1max}} \qquad (15)$$

An expression for D_{min} can be derived from (13) using the limit value C_{1lim} for C_1. Substituting into (15) we obtain:

$$\frac{R_{L\,max}}{R_{L\,min}} = \left(\frac{\hat{U}_{1max}}{2 \cdot (U_{g\,max} + 2U_L)} \right)^2 \qquad (16)$$

This shows that the maximum voltage stress must satisfy the constraint:

$$\hat{U}_{1max} \geq 2 \cdot (U_{g\,max} + 2U_L) \qquad (17)$$

Inductor L_1. The current waveforms in the input inductor, switch and diode are shown in figure 4. As we can see, the ripple amplitude of i_1 is greater than the value corresponding to the linear ramp during the switch on-time. This occurs due to the oscillation with capacitor C_1 in the off interval. From the equations of inductor current and capacitor voltage we can find:

$$i_1(\theta) = \frac{u_g(\theta)}{Z_1} \cdot \left\{ D\left(\gamma + \frac{\omega_1 D T_s}{2} \right) + \frac{1}{\omega_1 T_s} \left[(1-\alpha) + \beta(\gamma + \omega_1 D T_s) \right] \right\} \qquad (18)$$

which gives the average input current (over a switching cycle), and peak-to-peak input current ripple:

$$\Delta i_{1_{pk-pk}}(\theta) = \frac{u_g(\theta)}{Z_1}(\xi - \gamma) \qquad (19)$$

where the parameters are:

$$Z_1 = \sqrt{\frac{L_1}{C_1}}, \qquad \omega_1 = \frac{1}{\sqrt{L_1 C_1}} \qquad (20.a)$$

$$\alpha = \cos(\omega_1 (1-D) T_s), \beta = \sin(\omega_1 (1-D) T_s) \qquad (20.b)$$

$$\gamma = \frac{\alpha}{1-\alpha}\left(\omega_1 D T_s + \frac{\beta}{\alpha} \right), \xi = \sqrt{1 + (\gamma + \omega_1 D T_s)^2} \qquad (20.c)$$

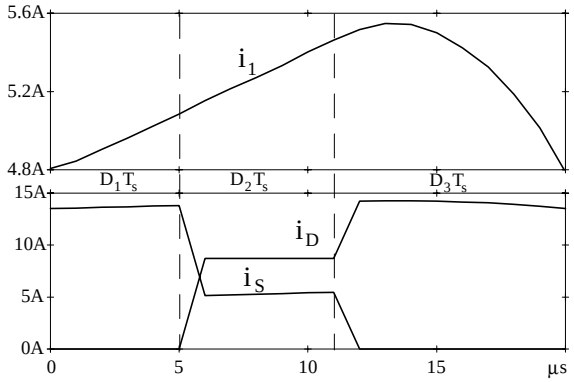

Figure 4: Input inductor, switch and diode current waveforms during a switching period

It is worthy to note that (18) confirms the property of this circuit to operate at unity power factor without duty cycle modulation since, the average input current results proportional to the line voltage when duty cycle D is fixed. Eqs. (18) to (20) can be used for choosing inductor L_1 so as to meet the input current ripple specification.

Inductor L_2. As stated above, L_2 must filter out the low-frequency component of voltage u'(θ) given by (10). Thus, the inductor value is given by:

$$L_2 = \frac{R_L}{\omega_i r_i} \qquad (21)$$

where r_i is the allowed relative low-frequency current ripple (peak-to-peak).
The corresponding stored energy is quite high, but can be considerably reduced by using a tuned L-C filter in place of L_2, as reported in King (5).

Capacitor C_2. Its aim is to further reduce the low-frequency ripple on the output voltage. Thus, if r_u is the allowed relative low-frequency voltage ripple (peak-to-peak), the capacitor C_2 value can be calculated as:

$$C_2 = \frac{r_i}{2\,\omega_i R_L r_u} \qquad (22)$$

Switch and diode current stress. As we can see from figure 4, during interval $D_1 T_s$ the switch carries the sum of the two inductor currents, while during interval $D_2 T_s$ its current reduces to the input inductor current only. Similarly, freewheeling diode D carries the output current during $D_2 T_s$ and the sum of the two inductor currents during $D_3 T_s$. Consequently, the current stresses are respectively:

$$i_{S_{pk}} = I_L \cdot \left[2M + \frac{U_g \quad D \quad T_s}{2 L_1 I_L} + 1 \right] \qquad (23)$$

$$i_{D_{pk}} = I_L \cdot \left[2M + \frac{\Delta i_{1_{pk-pk}}}{2 I_L} + 1 \right] \qquad (24)$$

Switch and diode voltage stress. The voltage stress is the same for both diode and switch and is equal to the maximum voltage $\hat{U}_{1max}$ across capacitor C_1.

Modified control strategy

As already asserted, the converter of figure 3 achieves unity power factor at constant duty-cycle and switching frequency, thus simplifying the control. Unfortunately, condition (16) poses a severe limit on the allowed load range due to the high voltage stress corresponding to wide load variations.

In order to overcome this limitation, a variable switching frequency control can be used. In fact, from (13) we see that if the switching frequency is kept proportional to the load current the voltage conversion ratio M becomes independent of the load. Thus, both duty-cycle and voltage stress remain constant.

For example, selecting C_1 equal to C_{1lim} for the maximum load current and substituting into (13) we obtain:

$$M = \frac{U_L}{U_g} = \frac{1}{2}\cdot\frac{D}{1-D} \tag{25}$$

Note that a minimum load current limitation must still exist in order to avoid the switching frequency to go near zero.

OPERATION AS PFP: CAPACITIVE FILTER

In the scheme of figure 3, the output inductor is the energy storage element which accounts for the low frequency input power fluctuation. As a consequence it results bulky and expensive.

However, we can observe that, in order to have unity power factor, we only need to discharge capacitor C_1 at every switching cycle. To do this, we need a high output inductor current i_2 only near the peak of the line voltage. This means that the output inductor can be designed to have a high low-frequency ripple, thus saving cost and size, without affecting the converter performances. This, of course, results in higher current stresses in the power semiconductors.

An alternative approach is to use the output capacitor as a storage element, as shown in figure 5 (voltage-fed approach (4)).

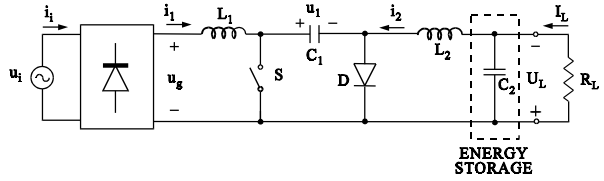

Figure 5: Ac-dc Cuk converter with capacitive filter

In this case, following the same approach outlined for the inductive filter we find that the converter operates with an apparent voltage conversion ratio m(θ) and an apparent load r(θ) given by:

$$m(\theta) = \frac{U_L}{u_g(\theta)} = \frac{U_L}{U_g|\sin(\theta)|} \tag{26}$$

$$r(\theta) = \frac{U_L}{i_2(\theta)} = \frac{R_L}{2\sin^2(\theta)} \tag{27}$$

Substituting into (5) the expressions (26) and (27) in place of M and R_L, respectively, we obtain again the voltage conversion ratio (13). Also peak voltage stress $\hat{U}_1$ remains unchanged, while the DCVM condition (8) becomes:

$$C_1 \le C_{1lim}(\theta) = D(1-D)\frac{I_L T_s}{U_g}\cdot|\sin(\theta)| \tag{28}$$

It is clear, from the above equation, that DCVM condition cannot be maintained during the whole line period, even at maximum load current. Thus, it becomes interesting to determine θ_{lim}, i.e the angle which separates DCVM from CCVM operation for a given voltage stress and load range. From (6), (14) and (28) we can derive:

$$\theta_{lim} = \sin^{-1}\left(\frac{2U_L}{\hat{U}_{1max}\sqrt{\frac{R_{L\,min}}{R_{L\,max}} - 2U_{g\,max}}}\right) \tag{29}$$

Equation (29) shows that in order to reduce the input current distortion a higher voltage stress than predicted by (16) must be tolerated. For example, considering a constant load resistance, using the value given by (17) for $\hat{U}_{1max}$ in the previous expression it yields $\theta_{lim} = \pi/6$.

SIMULATION AND EXPERIMENTAL RESULTS

In order to verify the theoretical forecasts a converter having the following specifications was simulated:

Input voltage .....U_g=110V_{rms}+/- 20%
Output voltage.....U_L=36V
Output power .....P_L=300W
Switching frequency .....f_s=50kHz

Converter with inductive filter

Considering a constant load resistance, the maximum voltage stress must satisfy inequality (17), which gives a value of 518V. Choosing $\hat{U}_{1max} = 550V$ so that DCVM condition is always satisfied, we find C_1=80nF from (14). The other parameter values follow from (18-22) and are listed in table 1.

TABLE 1 - Converter parameter values (inductive filter)

L_1=2mH	L_2=68mH	C_1=80nF	C_2=2.2mF
$\hat{U}_{1max} = 550V$	$\Delta i_{1_{pk-pk}} = 0.81A$	r_v=0.034	r_i=0.2

The simulated input current waveform is reported in figure 6 in the case of minimum input voltage. As we can see the converter draws a sinusoidal current in phase with the line voltage, thus achieving unity power factor.

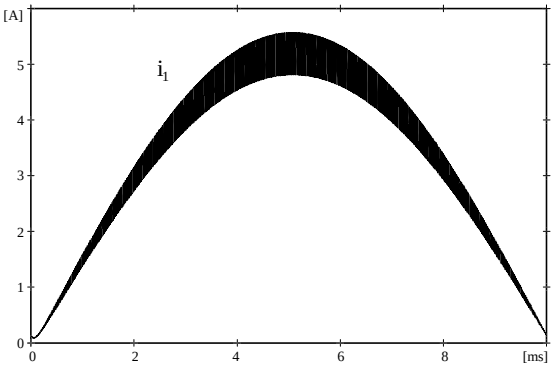

Figure 6: Simulated input current waveform at minimum line voltage

Converter with capacitive filter

Imposing that the value of θ_{lim} given by (29) with $R_{Lmax}=R_{Lmin}$ is lower than 10° results in a maximum voltage stress of 800V. Thus from (14) we find $C_1>37.5$nF. The other parameter values are reported in table 2. Note that, inductor L_2 was selected by imposing a constraint on its high frequency current ripple instead of using (21), while capacitor C_2 must now reject the whole low-frequency ripple and can be calculated using (22) with $r_i=2$.

TABLE 2 - Converter parameter values (capacitive filter)

L_1=2mH	L_2=0.4mH
C_1=40nF	C_2=20mF
$\hat{U}_{1max} = 800V$	$\Delta i_{1_{pk-pk}} = 1.35A$
$\Delta i_{2_{pk-pk}} = 1.3A$	r_v=0.037

A prototype was built with the given specifications. An IGBT (1000V, 34A) was employed. All the following measurements were taken at a reduced input voltage due to the dissipation problems caused by the reverse recovery of the freewheeling diode.

Figure 7 shows input voltage and current waveforms. Since at nominal conditions the value of the limit angle θ_{lim} is low, almost unity power factor is achieved.

The waveform of voltage u_1 during two switching periods is shown in figure 8, revealing the discontinuous operating mode and, above all, the zero-voltage turn off of the switch. This behaviour reveals a poor converter exploitation since capacitor C_1 is discharged in a small fraction of the available switch on-time. This is caused by constraint (29) which, in order to reduce the input current distortion, obliges to select a higher voltage stress as compared to the converter with inductive filter, with a consequent lower value of capacitor C_1. Moreover, differently from the converter of figure 3, current i_2 is not constant during the line period, but varies from zero to twice the load current (see eq. (27)). This means that at the peak of the line voltage, inductor L_2 has more than the energy necessary to discharge C_1.

This fact has another consequence: at the peak of the line voltage, the freewheeling diode carries a current higher than thet given by (24) (in practice, the same formula can be used providing that the unity term into parentheses is substituted by a factor 2), and, at the same time, it must sustain the maximum voltage stress. Thus, the losses due to the reverse recovery of the diode increase, as revealed by figure 9 which reports the switch current during a switching period: the high current spike at turn on is clearly visible. This phenomenon caused an efficiency of 66% at 45W output power. However, the high current spike can be reduced by using a faster diode.

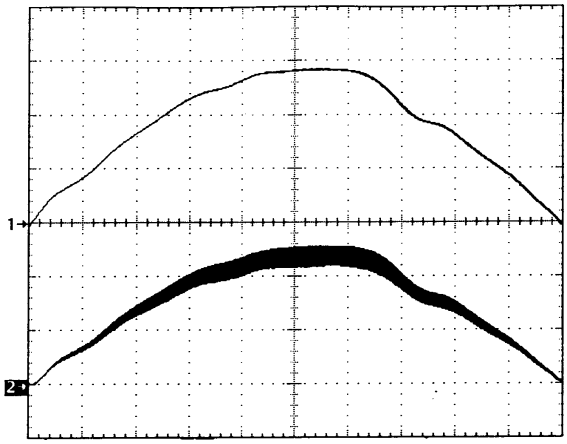

Figure 7: Measured input voltage (upper trace - 20V/div) and current (lower trace - 1A/div) waveforms. (Horz. 1ms/div)

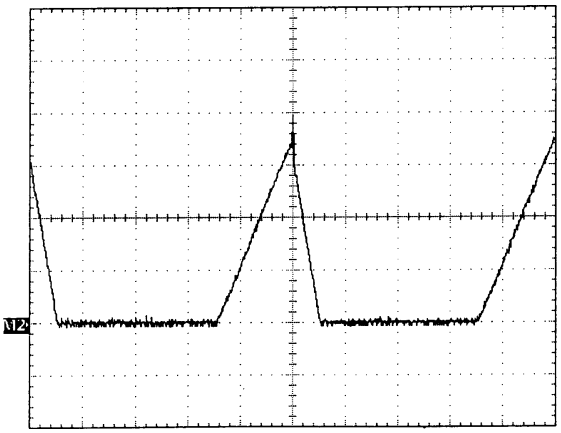

Figure 8: Detail of voltage u_1 waveform during two switching periods taken at the peak of the line voltage (Vert. 100V/div - Horz. 4µs/div)

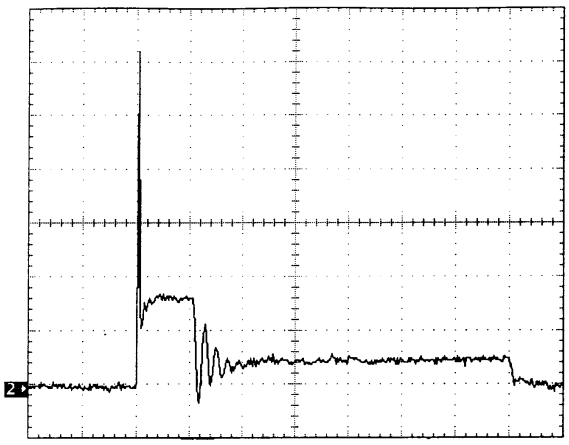

Figure 9: Detail of switch current waveform during a switching period taken at the peak of the line voltage (Vert. 5A/div - Horz. 2µs/div)

From the above considerations, we can expect a better behaviour from the converter with inductive filter.

CONCLUSIONS

A high-quality rectifier employing a Cuk converter operating in Discontinuous Capacitor Voltage Mode (DCVM) is analysed. A unity power factor is achieved with no need of duty-cycle modulation, also with capacitive output filter.
This solution allows a reduction of the reactive elements at the expense of higher voltage stresses on the power semiconductors. However, IGBT's can be profitably used at high frequency due to the zero voltage turn-off which reduces the losses caused by the tail current.
The proposed approach is suitable for smart-power integration and it is competitive in the low-voltage environment.
Simulated and experimental results are reported showing actual converter performances.

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References

1. Simonetti, D.S.L., Sebastian, J., Dos Reis, F.S., and Uceda, J., 1992, IECON Conf. Proc., pp. 283-288.
2. Brkovic, M., and Cuk, S., 1992, INTELEC Conf. Proc., pp. 532-539.
3. Spiazzi, G., Rossetto, L., 1994, PESC Conf. Proc., pp.336-341.
4. Freeland, S.D., 1988, Phd Thesis, Part II, CalTech.
5. King,, R.J., 1991, IEEE Trans. on Industrial Electronics., Vol.38, NO.2, April, pp.126-134.

Addresses of the authors

G.Spiazzi, L.Rossetto, P.Mattavelli, S.Buso: University of Padova, via Gradenigo 6/a, 35131, Padova, ITALY