METHODS TO IMPROVE DYNAMIC RESPONSE OF POWER FACTOR PREREGULATORS: AN OVERVIEW

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Abstract. In standard Power Factor Preregulators (PFP's), there is a trade-off between output voltage dynamic and input current distortion. In this paper, several control techniques aimed to improve the output voltage transient response of Power Factor Preregulators (PFP's) while maintaining a high power factor are reviewed and compared.
These methods do not require additional sensing, but only simple analog circuitry, and work with wide input voltage range.
Simulation tests on a Boost converter with average current control highlight merits and drawbacks of each solution.

Keywords. Power factor correction, rectifier, Control Techniques.

INTRODUCTION

In ac/dc rectifiers with unity power factor, the main effort is devoted to the quality of the input current waveform while, especially with simple single-switch topologies like the Boost one, the dynamic response of the output voltage is sacrificed [1]. In fact, due to the input power fluctuation, the output voltage contains a low-frequency ripple at twice the line frequency which affects the input current waveform unless the loop bandwidth is kept well below the line frequency (typically 10-20 Hz). The result is a poor transient response of the output voltage during line and load variations.
Many techniques aimed to improve the output voltage response while maintaining a high power factor have been proposed in the literature [2-7]. Between these control approaches those which do not require additional sensing (i.e load current sensing) and/or significant increase of control complexity are likely to be used, since they do not modify the basic control scheme and, on the contrary, can be integrated with it.
Almost all the proposed control techniques are aimed to remove the low-frequency ripple from the feedback signal, so as to allow a higher voltage loop bandwidth. In [2], the use of a notch filter tuned at twice the line frequency was analysed, while a sampling network was employed in [2] and [3]. Both these approaches are simple and effective, but the dynamic improvement achievable is limited due to stability problems.
Better performances can be obtained by using ripple compensation techniques like those proposed in [4,6]. While in [4,5] the presented solutions had the drawback of the need of a precise load power estimation, which requires sensing of the load current and increased control complexity, in [6] a compensation technique was proposed which allows a good compromise between dynamic response and control complexity without need of additional sensing.
A different approach was proposed in [2] in which a non linear output voltage regulator is employed: the current reference amplitude is kept constant when the output voltage is inside a suitable band (which is wide enough to contain the low frequency ripple) while when the output voltage goes outside of this "regulation band" a high gain error amplifier acts so that to bring the output voltage back inside the band as fast as possible. A modification of this regulation band approach is also presented in this paper.
Instead, the solution proposed in [7] employs the sliding mode control to reduce the output voltage deviation from the reference value during transient conditions at the expense of a higher input current distortion
In this paper, all these methods are reviewed and compared by simulation of a boost power factor preregulator: advantages and drawbacks of each solution in terms of hardware implementation and effectiveness are highlighted.

BASIC PFP SCHEME

A boost PFP with average current control is shown in figure 1 [1]. The large bandwidth current error amplifier $G_i(s)$ forces the input current, sensed by resistor R_S, to follow as close as possible a suitable sinusoidal reference signal. This latter is generated by multiplying a scaled version of rectified voltage v_g by the output of the voltage error amplifier. Thus, the voltage loop adjusts the current reference amplitude to keep the output voltage constant and equal to V_{REF}.
The third input of multiplier M1 is fed by a signal proportional to the line voltage RMS value obtained from v_g by using a low-pass filter. This feedforward action helps the system response to line variations: in fact, with constant output power, an increase of the input voltage must correspond to a proportional decrease of the input current, which is provided by the feedforward path without need of voltage loop intervention.
In the assumption of unity power factor and negligible input inductor energy, the fluctuating input power causes a low-frequency voltage ripple Δv_o across C_o which depends only on the load current and is given by:

$$|\Delta v_o(t)| = \frac{I_o}{2\omega_i C_o}\cdot\sin(2\omega_i t) = \frac{P_o}{2\omega_i C_o V_o}\cdot\sin(2\omega_i t) \quad (1)$$

where ω_i is the line angular frequency (rad/s) and P_O the output power. This holds provided that the voltage loop has a bandwidth well below the line frequency, in order to avoid variation of $I_{REF}(t)$ within the line cycle, which would cause input current distortion. To this purpose, a standard controller has a voltage loop bandwidth in the range 10-20Hz. This fact, gives a poor dynamic response to load variations.

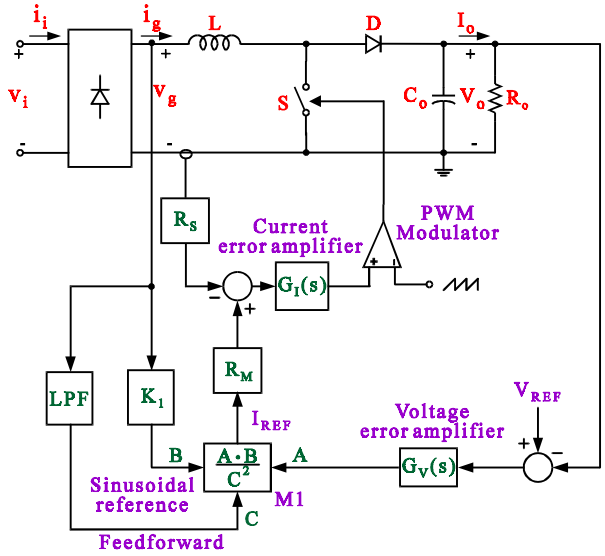

Figure 1: Basic scheme of the boost PFP with average current mode control

In the following, several modification of the basic control scheme of figure 1 aimed to eliminate the low-frequency ripple from the feedback signal are reviewed.

CONTROL SCHEME WITH NOTCH FILTER

A natural way to remove the output-voltage low-frequency ripple is to add a notch filter tuned at twice the line frequency in the voltage loop, as shown in figure 2 [2].

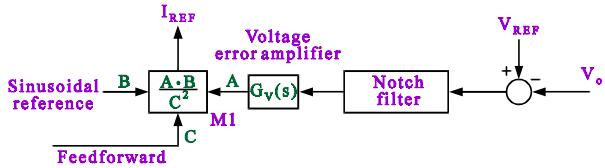

Figure 2: Control scheme with notch filter.

This solution is very simple, requiring only few added components, and effective if the filter is well tuned and has a high quality factor. The main limitation of this solution is represented by the limited improvement achievable on the output voltage dynamic. In fact, the notch filter transfer function

(2)

$$G_{NOTCH}(s) = \frac{s^2 + (2\omega_i)^2}{s^2 + \frac{2\omega_i}{Q}s + (2\omega_i)^2}$$

causes a deep notch in the magnitude plot of the voltage loop gain associated with a phase rotation between $-\pi/2$ and $\pi/2$ which is going to affect the system stability unless a lower crossover frequency is selected. Thus, the output voltage loop bandwidth is limited to a value below twice the line frequency.

CONTROL SCHEME WITH SAMPLE & HOLD

A ripple free feedback signal can be obtained by using discrete-time domain techniques. In particular, by sampling the output voltage error signal at a rate equal to the voltage ripple (1) during the zero crossing point of the line voltage, the average output voltage can be sensed [2-3]. This solution does not significantly increase the controller complexity requiring just few analog devices as shown in figure 3.
One advantage given by the discrete-time approach is that the current command signal A is not allowed to vary during a half-line cycle and is updated only at the beginning of each half cycle. This means that a high power factor can be maintained in both transient and steady-state conditions.
Like the notch filter approach, the use of a sampling network limits the maximum voltage loop bandwidth achievable to a value lower that twice the line frequency, due to the phase shift introduced by the sample & hold action [3].

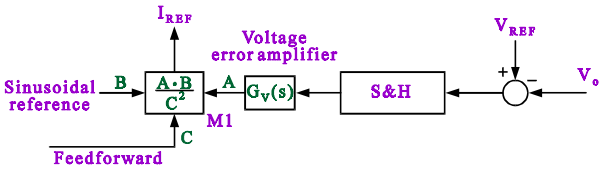

Figure 3: Control scheme with sample & hold network.

CONTROL SCHEME WITH RIPPLE COMPENSATION

This technique is based on the principle of output voltage ripple cancellation [4-6]. This means that ripple $\Delta v_O(t)$ is estimated and subtracted to $v_O(t)$, so that the voltage error amplifier processes a ripple-free signal.
According to (1), estimation of $\Delta v_O(t)$ requires a sinusoidal waveform at twice the line frequency with an amplitude proportional to the output power. In the literature [4,5] signal $\Delta v_O(t)$ is generated by using a PLL, which gives the waveform $\sin(2\omega_i t)$ and by sensing the load current to produce a signal proportional to the load power. Besides the use of an additional sensing, the drawback of this approach is that it works well only with a pure sinusoidal line voltage, since the presence of harmonics in the input voltage causes the ripple signal to deviate from (1).
The ripple cancellation scheme shown in figure 4, was proposed in [6]. Here, voltage ripple $\Delta v_O(t)$ is estimated in the following way: under unity power factor assumption, the input power is given by:

$$p_{in}(t) = v_g(t)\cdot i_g(t) = P_{in} - \frac{\eta P_o}{2}\cdot\cos(2\omega_i t) \quad (3)$$

where η is converter efficiency and $P_{in}=\eta P_o$ is average input power. Comparison between (1) and (3) shows that $\Delta v_o(t)$ can be estimated from the signal $p_{in}(t)$ by eliminating the DC component P_{in}, multiplying the result by a proper gain and phase shifting by ninety degree.

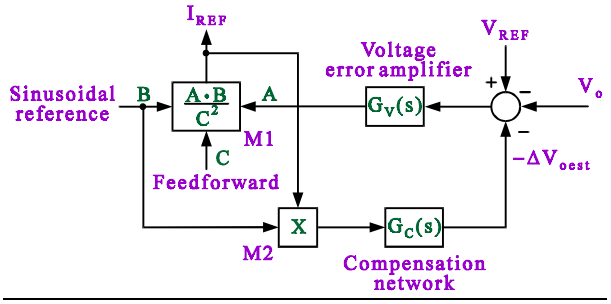

Figure 4: Control scheme with ripple compensation network.

In figure 4, the input power signal (3) is obtained by multiplying (M2) a signal proportional to rectified input voltage v_g by reference current I_{REF}. This latter is used instead of i_g in the assumption of a large current loop bandwidth. Then, block G_C provides the estimated ripple signal $\Delta v_{oest}(t)$ which is finally subtracted to $v_o(t)$, thus providing a ripple free signal for the voltage error amplifier.
Since the reconstructed ripple signal is proportional to the power, as requested by (1), its action is not affected by load and/or input voltage variations; the PFP can therefore be used with wide input voltage range.

In theory, the correct ripple estimation can be provided by the simple compensation network:

$$K_C = \frac{K_2}{2\eta\omega_i^{\,2} C_o V_o} \qquad (4a)$$

where K_C is given by:

$$K_C = \frac{K_2}{2\eta\,\omega_i^{\,2} C_o V_o} \qquad (4.b)$$

$K_2=R_M/(K_1R_S)$ takes into account the various scaling factors.
In practice, it is worthwhile to observe that network $G_C(s)$ may cause errors in the estimation of $\Delta v_o(t)$ due to the presence of the derivative action, especially in the case of a significant harmonic content in the input voltage. In fact while the power stage output filter R_o-C_o attenuates higher harmonics in the output voltage ripple, network G_C performs an opposite action, thus increasing the harmonic content in the estimated signal.
In order to overcome this problem the compensation network $G_C(s)$ must provide:

a) ninety degrees phase shift
b) elimination of the DC term
c) first-order attenuation of higher harmonics (similarly to the R_o-C_o filter).

These goals can be accomplished by using a band-pass filter tuned at twice the line frequency (which satisfies points b) and c)) followed by a phase shifting network to satisfy point a) (this latter can be implemented by means of a couple negative real pole-positive real zero at the same frequency $2\omega_i$).
In [6] was demonstrated that, since a perfect ripple compensation cannot be achieved, a reasonable trade-off between input current distortion and speed of response yields to a 100-200Hz voltage loop bandwidth range, which represents a considerable improvement respect to previously mentioned control techniques.

CONTROL SCHEME WITH "REGULATION BAND"

In this control technique, different actions are done depending if the voltage error signal is inside or outside a suitable regulation band, which is made large enough to include the maximum expected voltage ripple. Two different approaches are reported hereafter.

Regulation Band Approach TYPE 1

According to the control technique proposed in [2], the current reference amplitude is kept constant as long as the output voltage remains within a defined regulation band. When the output voltage goes outside of this band a high gain controller changes rapidly the current reference amplitude so as to bring the output voltage back into the regulation band. A simplified scheme of this control technique is shown in figure 5. Note the local feedback through block K_b which makes the global transfer function between V_o and I_{REF} constant and equal to K_a/K_b (assuming the transconductance amplifier has high gain).
As demonstrated in [2], in order to ensure system stability, the gain must be chosen according to the equation:

$$\frac{K_a}{K_b} = \alpha \cdot \frac{V_o C}{L I_{g\max}} \qquad (5)$$

where α is a parameter whose value is lower than one, while error amplifier $G_V(s)$ is a simple PI regulator whose zero should have a time constant close to the line period.
With this control technique, a good output voltage dynamic response is achieved while the input current dynamic results slower, even if the correct current waveform is recovered in few line cycles.
One drawback of this control scheme is that, since the current reference amplitude does not change as long as the output voltage is inside the regulation band, the correct average output voltage is obtained only at nominal condition (i.e. maximum load current), where the band amplitude coincides exactly with the voltage ripple amplitude. Instead, when the ripple is smaller than the band (i.e. at different line and/or load conditions), we have an average output voltage error.

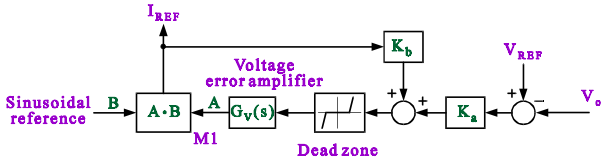

Figure 5: Control scheme with regulation band approach (TYPE 1).

Regulation Band Approach #2

In order to overcome the problem represented by the steady-state error on the output voltage of the previous control technique, a low-bandwidth PI controller can be used which ensures stability and no DC errors. When the output voltage goes outside the band, the gain of the voltage error amplifier is

increased in order to enhance the corrective action. The block scheme of figure 6 describes this control technique.

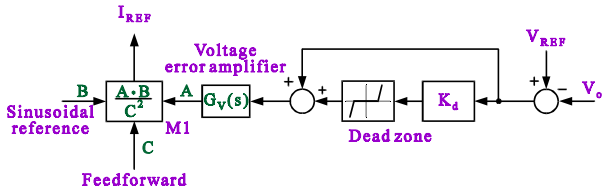

Figure 6: Control scheme with regulation band approach (TYPE 2).

SLIDING MODE CONTROL

Differently from the previous control techniques, the sliding mode control approach presented in [7], keeps the low-frequency output voltage loop. However, as shown in figure 7, a faster inner loop, represented by gain K_V, was added to the current error signal (multiplied by gain K_i) to form the sliding function ψ. Then, a hysteretic block drives the switch so as to maintain the sliding function close to zero. The relative value of the two coefficients K_i and K_V determines which variable (input current or output voltage) is more tightly regulated, thus allowing a trade-off between input current distortion and dynamic response speed.

Note that the action of the faster voltage inner loop is to reduce the output voltage overshoot and undershoot during transient conditions, while the settling time is still dominated by the slower outer voltage loop.

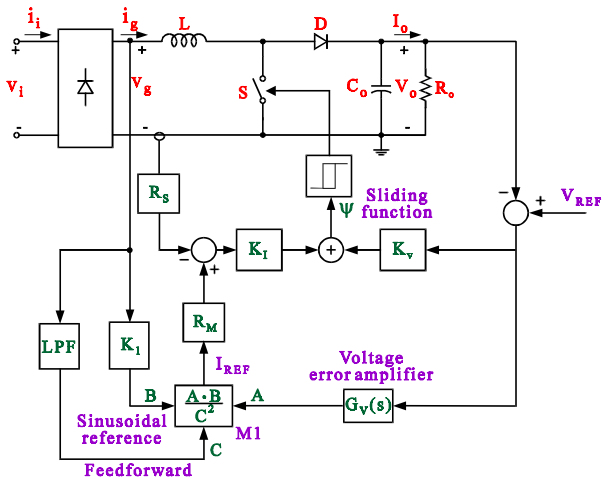

Figure 7: Sliding mode control scheme of boost PFP.

COMPARISON OF CONTROL STRATEGIES

All these control techniques were simulated with a boost PFP whose parameter values are reported in Table 1, except the sliding mode control because, in this latter, the converter dynamic improvement is related to the allowed input current distortion. However, experimental results of a Cuk PFP with sliding mode control can be found in [2].

The converter response in terms of output voltage error and rectified input current waveforms was analysed for a load step change from 100% to 10% of rated power and vice versa. The results are reported in figure 8 through 13 with the following sequence: standard control (S.C.), notch filter (N.F.), sample & hold (S.H.), regulation band type 1 (R.#1), regulation band type 2 (R.#2) and ripple compensation (R.C.).

The error voltage amplifier is a PI regulator for all the presented solutions

$$G_v(s) = \frac{K_I}{s}\left(1 + \frac{s}{\omega_z}\right) \qquad (6)$$

and its parameter values are reported in table 2.

TABLE 1 - Converter parameters

V_g=220V_{RMS}	V_o=380V	f_s=50kHz
L=2mH	C_o=470µF	P_o=600W

TABLE 2 - Error voltage amplifier parameter values

	S.C.	N.F.	S.H.	B.#1	B.#2	R.C.
K_I	8.8	73.4	8.7	100·K_a	8.8·K_d	223
ω_z	69.2	188.5	62.8	166.7	69.2	354.4

(K_a=13.8, K_h=1, K_d=21.4)

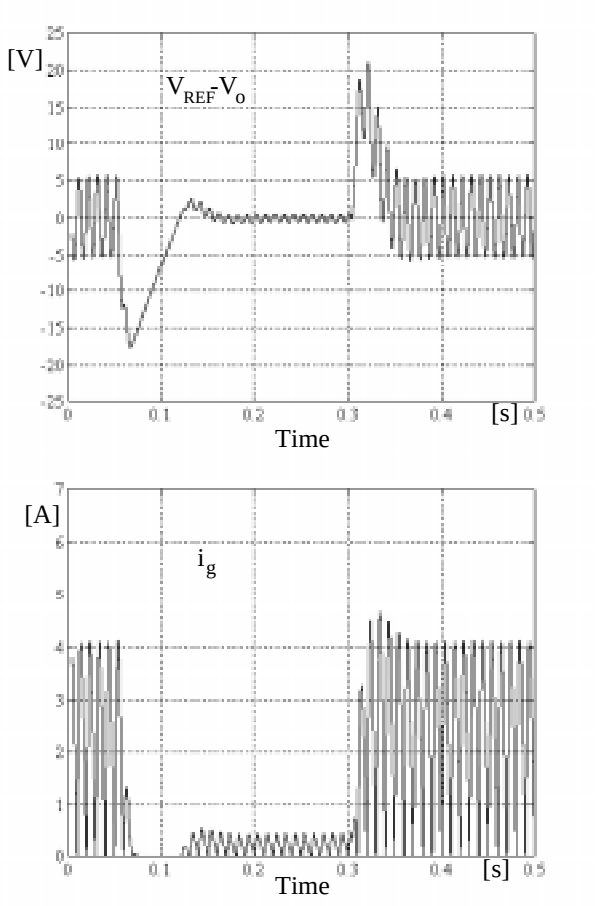

Figure 8: Output voltage error (top trace) and rectified input current waveforms (bottom trace) during a load step change from 100% to 10% of rated power and vice versa, for a standard boost PFP.

As far as the standard control is concerned, a voltage loop bandwidth of 20 Hz was selected, thus achieving a not too bad dynamic response. However, the third harmonic in the input current is already about 10% of the fundamental one.

From the analysis of the shown waveforms, we can do the following considerations:

- the sample & hold network exibits a dynamic response similar to that of the standard solution. However, we obtain a unity power factor both in steady state and transient conditions. To achieve the same results with standard control, the loop bandwidth must be further reduced to some Hertz, slowering its dynamic response.
- Both regulation band approaches work satisfactorily limiting the output voltage deviation from the steady state. Note that regulation band TYPE 1 suffers from a steady state error in the output voltage which disappears using the regulation band TYPE 2 technique. On the other hand, it provides unity power factor when the output voltage is inside the regulation band, while the second solution behaves like a standard approach. Observe the input current distortion during transient conditions: it takes some line cycles before to recover the undistorted sinusoidal waveform.
- The two solutions which give better results both in terms of voltage overshoot/undershoot and settling time are the notch filter and the ripple compensation schemes. Table 3 reports also the normalised value of input current harmonics obtained from these control techniques for two different situations: A) pure sinusoidal line voltage and B) line voltage with 10% of third harmonic. As we can see, even if, in the presence of the third harmonic in the line voltage, the harmonic content of the ripple compensation scheme is higher than that of the notch filter, the power factor is 99.75% for the R.C. compared to 99.47% of the N.F..

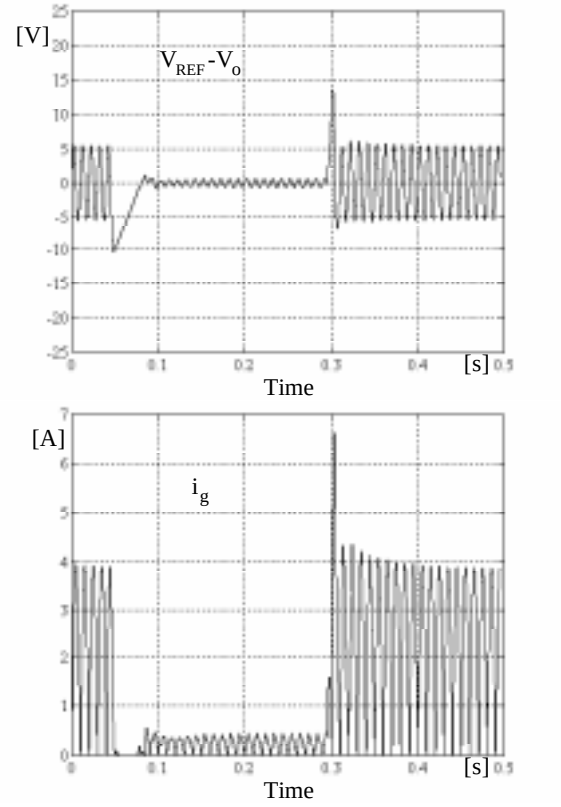

Figure 9: Output voltage error (top trace) and rectified input current waveforms (bottom trace) during a load step change from 100% to 10% of rated power and vice versa, for the notch filter approach.

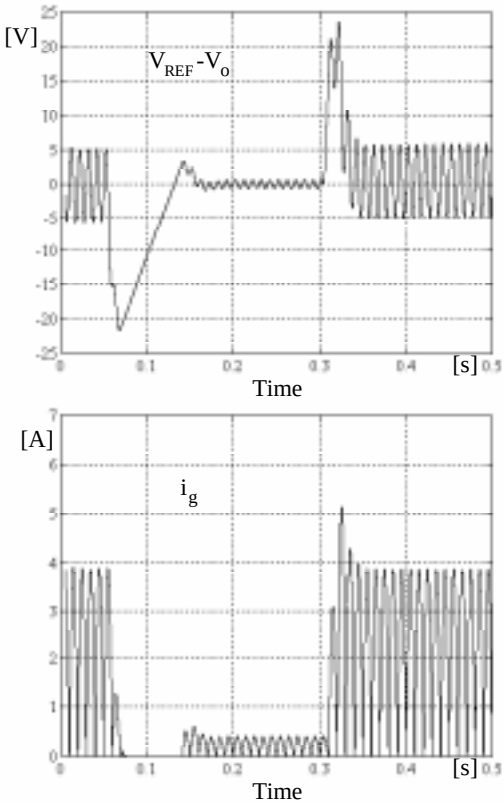

Figure 10: Output voltage error (top trace) and rectified input current waveforms (bottom trace) during a load step change from 100% to 10% of rated power and vice versa, for the sample & hold approach.

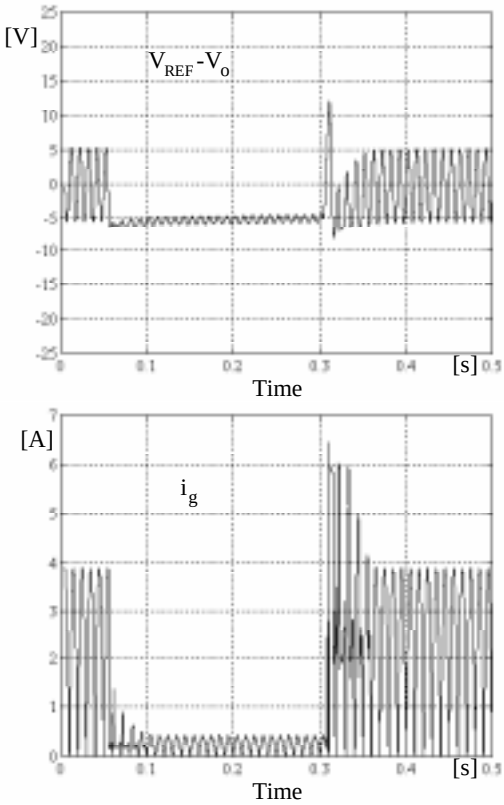

Figure 11: Output voltage error (top trace) and rectified input current waveforms (bottom trace) during a load step change from 100% to 10% of rated power and vice versa, for the regulation band TYPE 1 approach.

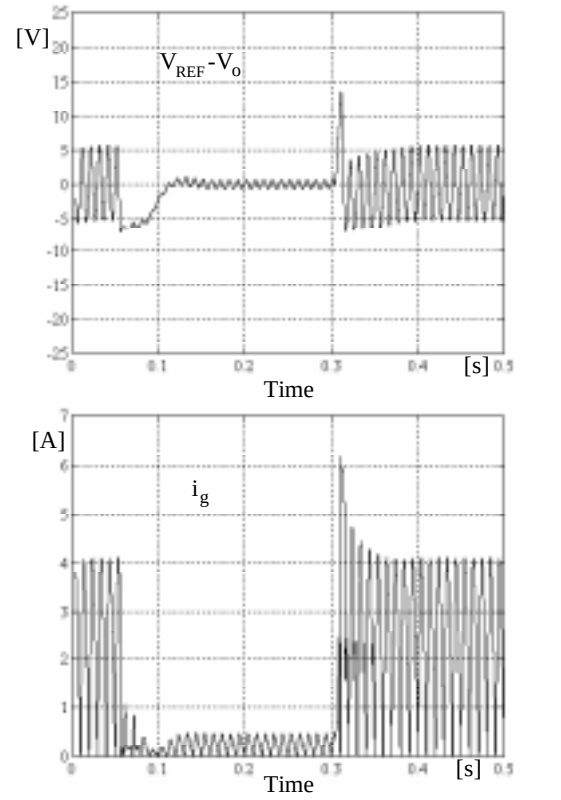

Figure 12: Output voltage error (top trace) and rectified input current waveforms (bottom trace) during a load step change from 100% to 10% of rated power and vice versa, for the regulation band TYPE 2 approach.

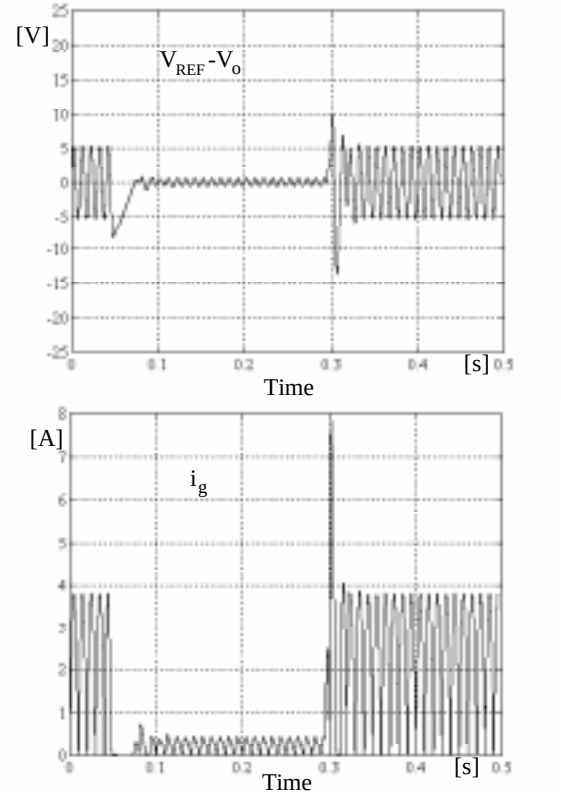

Figure 13: Output voltage error (top trace) and rectified input current waveforms (bottom trace) during a load step change from 100% to 10% of rated power and vice versa, for the ripple compensation scheme.

TABLE 3 - Normalised input current harmonics for two different situations: A) pure sinusoidal line voltage and B) line voltage with 10% of third harmonic.
(R.C = ripple compensation, N.F. = notch filter)

v_i		3^{th}	5^{th}	7^{th}	9^{th}	11^{th}
A)	R.C	-31.6	-38.5	-42.1	-43.3	-43.3
A)	N.F	-42.4	-44.0	-44.8	-44.4	-44.2
B)	R.C.	-21.3	-25.8	-33.8	-38.5	-40.9
B)	N.F.	-34.8	-34.2	-45.2	-45.5	-45.4

CONCLUSIONS

Different control techniques aimed to improve the transient response of power factor preregulators, without affecting the quality of the input current waveform, are reviewed. These methods do not require additional sensing, and work with wide input voltage range.
Their performance are compared by simulation done for a Boost PFP with average current control.

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