HIGH-QUALITY RECTIFIERS WITH HIGH-FREQUENCY INSULATION - AN OVERVIEW

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Abstract. This paper presents an overview of single-phase topologies for active power factor correction with high-frequency insulation.

Solutions for low- and medium-power applications are investigated, with particular attention to solutions capable to provide fast output voltage regulation.

A brief review of control techniques suitable for power factor correction (PFC) circuits is also reported.

1. INTRODUCTION

Since January 1996, the IEC 555-2 standard, limiting harmonic current absorption of household appliances up to 16 A per phase, will take effect. Accordingly, loads connected to the low-voltage distribution grid will be required for compensation on individual basis. Something similar is coming on also for larger power and voltage levels, due to the increasing application of IEEE 519 recommended practice. The impact of such standards on cost and size of the power supplies can be considerable: for IEC 555-2, an average increase of about 20% has already been estimated.

Solutions mainly depend on the power level. Passive solutions are widely used both at high power level (above 10kW) and at very low power level (below 200W). At high power, passive solutions are justified by the lack of stringent harmonic regulations and the difficult application of high-frequency switching techniques. At low power, passive solutions are justified by cost saving (mostly on EMI filters and semiconductors). For intermediate power levels, active solutions based on electronic switched-mode Power Factor Correctors (PFC's) can be cost effective, but EMI/EMC limits must carefully be taken into account.

After a presentation of IEC 555-2 standard, this paper comments today's available single-phase topologies for active power factor correction complying with standard requirements and capable of high-frequency insulation. Particular attention is devoted to solutions providing fast output voltage regulation. A brief review of PFC control techniques is also presented.

2. IEC 555-2 STANDARD

There are many good reasons to limit harmonic current absorption from the grid. In fact, current harmonics cause: improper operation of protection relays and circuit breakers; voltage distortion due to voltage drop on series line impedances; possible amplification of voltage distortion due to resonance phenomena; increased losses in series components of power distribution; decreased accuracy of measuring instruments.

Limiting the current distortion is advantageous on load side too. In fact, increasing the power factor makes more power available. Moreover, the current in neutral wires is greatly reduced.

Obviously, the impact of harmonic-limiting standards on complexity and cost of electronic power supplies will be considerable, taking also into account that active compensators based on switching converters produce radio-frequency noises, which need to be compensated too.

The IEC 555 standard [1] applies to single-phase and three-phase equipment drawing less than 16 A per phase and divides the loads into four categories: *Class A* includes balanced 3-phase equipment and all other equipment, except those in one of the remaining classes; *Class B* includes portable tools; *Class C* includes lighting equipment and dimming devices with active power above 25W; *Class D* includes equipment having an input current within the mask shown in Fig.1 and a fundamental active power between 75W and 600W. Whatever the waveform of their input current, class B, class C, and provisionally motor-driven equipment are not considered as class D equipment.

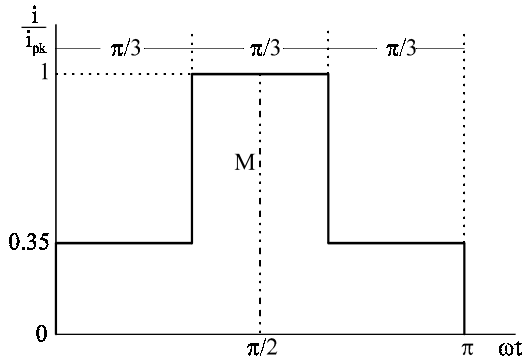


Fig.1 - Limit waveshape for *Class D* equipment

Absolute or relative harmonic current limits are set from the standard for each class, see Tables 1, 2, 3.

In general, we can say that:

- standard requires equipment-level compliance, and cost is directly borne by the end user;
- high crest-factor waveforms are penalized (class D), in order to reduce the peak-clipping effect;
- odd harmonics are penalized, in order to reduce asymmetry;

- requirements for lamps above 25W are quite severe, but below 25W (i.e., for most fluorescent lamp ballast) there are no limits;
- below 600W, class A requirements are less stringent than for class D, so that changing the input current waveform to exit class D can be convenient;
- it is easy to check that diode-capacitor rectifiers do not fulfil the standard, except in case of a very high dc voltage ripple.

Table 1 - Harmonic current limits for Class A and Class B equipment

	Class A	Class B
Harmonic order n	max permissible harmonic current	max permissible harmonic current
odd	A	A
3	2.30	3.45
5	1.14	1.71
7	0.77	1.155
9	0.40	0.60
11	0.33	0.495
13	0.21	0.315
15 <= n <= 39	2.25/n	3.375/n
Even		
2	1.08	1.62
4	0.43	0.645
6	0.30	0.45
8 <= n <= 40	1.84/n	2.76/n

Table 2 - Harmonic current limits for Class C equipment (>25W)

Harmonic order n	Maximum value expressed as a percentage of the fundamental input current of the luminaries
2	2
3	30 λ^*
5	10
7	7
9	5
11 <= n <= 39	3

*λ is the power factor

Table 3 - Harmonic current limits for Class D equipment

Maximum permissible harmonic current	
Harmonic order n	75 W < P < 600 W mA/W
3	3.4
5	1.9
7	1.0
9	0.5
11	0.35
13	0.296
15 <= n <= 39	3.85/n

No limits apply for equipment below 75 W input power

3. HIGH-QUALITY RECTIFIERS

A common approach to achieve almost unity power factor is to use a power factor preregulator followed by a dc/dc stage, which provides high-frequency insulation as well as tight output voltage regulation [2].

Such a configuration is shown in Fig.2. Capacitor C_B stores and returns the energy associated to the input power fluctuation due to sinusoidal current absorption. Consequently, the voltage across C_B has a considerable ripple at twice the line frequency, which does not allow a fast output voltage regulation of the PFC. In fact, compensation of this voltage ripple would involve a distortion of the line current, so that the voltage loop must have a bandwidth lower than the line frequency [2-3].

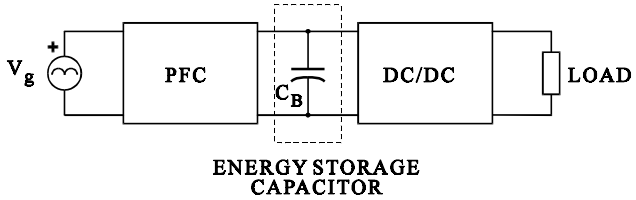


Fig.2 - Two-stage power factor controller

Output voltage accuracy is ensured by the dc/dc converter stage, which easily includes high-frequency insulation too. This configuration, however, has a low efficiency, since the same power is processed twice. Moreover, it is expensive due to high number of components and circuit complexity.

In order to overcome these limitations single-stage topologies offering performances similar to the two-stage scheme and reduced circuit complexity have been identified and will be discussed hereafter.

4. LOW-POWER PFC TOPOLOGIES

In this section, high-quality rectifiers suited for low-power applications are reviewed. All of them are characterized by discontinuous operation, which generally involves the following effects:

- component stresses and conduction losses are high as compared to useful voltage and current;
- voltage and current ringings may appear as a consequence of resonances between converter inductances and device parasitic capacitances (increased EMI);
- if input current is discontinuous, rectifier diodes must be fast devices, unless the input filter is located after the bridge;
- if input current is discontinuous, the input filter for differential-mode noise attenuation must be sized taking into account the high-frequency harmonic content of the current;
- diodes' reverse recovery is soft;
- switches turn on at zero current.

Except for the simple flyback PFC, all topologies described hereafter provide a fast output voltage

regulation, by moving the low-frequency filter capacitor C_B from the converter output into the converter itself.

a) Flyback converter

The simplest PFC with high-frequency insulation is the flyback converter shown in Fig.3 [4-7]. This converter can operate both in the continuous and discontinuous conduction mode. In the discontinuous conduction mode (DCM), input current is made up of saw-tooth pulses at the switching frequency. In this case, the line current, averaged over each switching period, turns out to be sinusoidal and in phase with the line voltage even for constant duty-cycle.

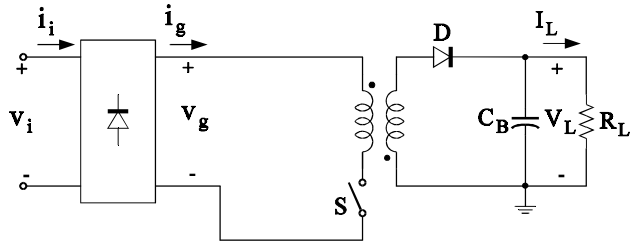


Fig.3 - Flyback converter as PFC

In this topology, the transformer is a critical element: it stores energy in its magnetizing inductance (an air gap is needed, therefore increasing the flux leakage) and works only with unidirectional flux density. Moreover, the switch voltage stress is the sum of peak input voltage and output voltage reflected on the primary side (additional overvoltages are caused by transformer leakage inductances).

A non-negligible advantage of the flyback converter is its inherent start-up capability and overload protection, due to the switch in series to the power path.

Note that capacitor C_B filters the line frequency ripple so that a fast output voltage regulation cannot be achieved.

b) S^2IP^2 converter family

In [8] a family of Single-Stage Isolated Power-factor corrected Power supplies (S^2IP^2) is presented, whose general configuration is shown in Fig.4. The approach is based on the combination of the switches of a PFC cell and a dc/dc cell, whenever they have a common ground. In this way the two cascaded stages of Fig.4 are turned into a single stage with energy storage capacitor C_B inside the converter, thus allowing a tight output voltage regulation.

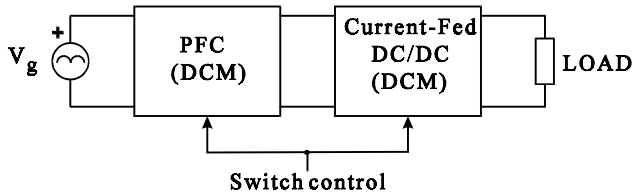


Fig.4 - General structure of S^2IP^2 family

The main limitation of this approach is that both PFC and dc/dc converters can operate in DCM only. In fact, DCM operation is needed in the input stage in order to achieve a high power factor, while in the second stage it removes the dependence of voltage V_B across the energy storage capacitor on the load current, which otherwise would produce unacceptable voltage stresses at light load.

As an example, Fig.5 reports the converter obtained by combining a boost power stage and a forward dc/dc converter into a scheme using a single switch.

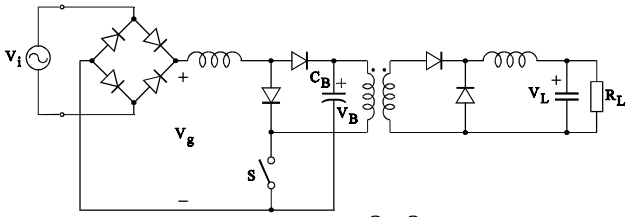


Fig.5 - Boost-forward S^2IP^2 topology

When a boost PFC stage is used, an input current distortion occurs, which depends on the ratio between V_B and rectified voltage V_g. Thus converter design calls for a trade off between input current quality and voltage stresses [8]. In this family, transformer exploitation is the same as for the corresponding insulated converter topology.

c) Dither rectifiers

Rectifiers based on the "dither" effect can considerably improve the power factor of conventional diode-capacitor rectifiers [9-11].

The concept is illustrated in Fig.6. A non-linear dead-zone element is supplied by a sinusoidal voltage whose amplitude is slightly higher than the dead-zone limit V_B. Thus, the output signal is made up of narrow pulses having a high harmonic content (this situation is typical of the diode-capacitor rectifiers where the absorbed current takes the place of the output signal). Adding to the low-frequency input signal a high-frequency dither signal, with amplitude higher than V_B, increases the conduction intervals of the dead-zone element, thus reducing the low-frequency distortion of the output signal, as shown in Fig.6, while its high-frequency harmonic content is removed by the low-pass filter.

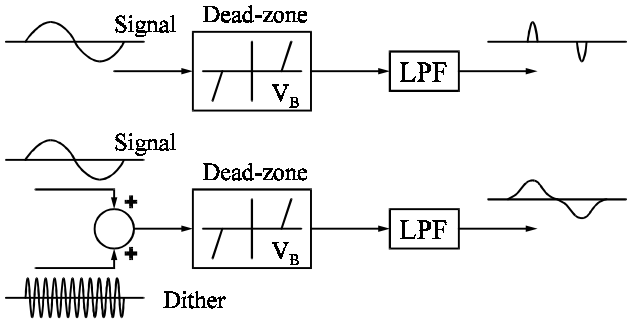


Fig.6 - Principle of dither rectifier

A practical implementation of the dither concept to ac/dc conversion stages is shown in Fig.7. The scheme is a combination of a voltage doubler and a conventional half-bridge converter. By simply changing one input connection from point A to point B, the high-frequency dither signal present in the inverter leg is added to the input voltage. The result is an improvement of the input current

waveform, provided that an inductor is added in series to the line in order to filter the input current.

As the input stage behaves like a boost converter operating in DCM, some low-frequency distortion of the input current is still present, which depends on the ratio between peak input voltage V_i and voltage V_B, which tends to increase greatly when output power decreases. In order to limit this phenomenon while controlling the output voltage, simultaneous control of both duty-cycle and switching frequency must be used. This approach does not suit applications with wide load ranges, but, on the other hand, a fast output voltage regulation can be achieved since the energy storage capacitor is inside the converter.

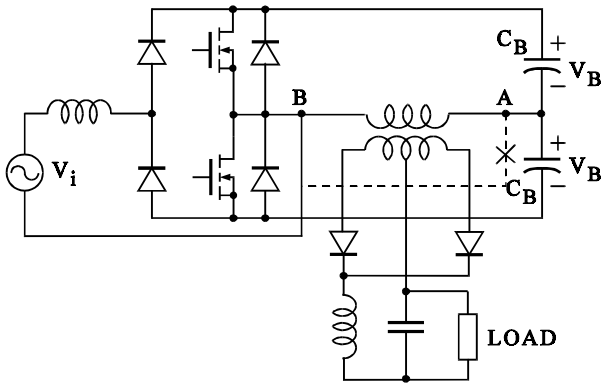
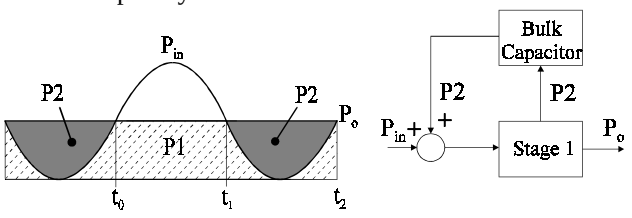


Fig.7 - High-quality rectifier using the dither concept

d) Parallel power factor correction schemes

The concept of parallel power processing is illustrated in Fig.8 [12-13]. The relationship between input and output power of a single-phase PFC, shown in Fig.8a, reveals that not all the power needs to be processed twice, as in conventional two-stage PFCs. In fact, about 68% of the average input power (term P1) can flow to the output through a single power conversion stage, while remaining 32% (term P2), which is stored in an internal capacitor during interval t_0-t_1, needs to be processed twice (it is released during interval t_1-t_2 using the storage capacitor to feed the PFC stage, as shown in Fig.8b). With this approach, both high power factor and tight output voltage regulation can be achieved, at the expense of increased circuit complexity.



a) b)

Fig.8 - Parallel power processing concept: a) power relationship of single-phase PFC; b) parallel PFC scheme

An example suited for low power applications is reported in Fig.9, which shows a flyback parallel PFC [13]. Switch S_1 is modulated in order to control the input current waveform, while switches S_2 and S_3 are modulated (together with S_1), respectively when $P_{in}>P_o$ and $P_{in}<P_o$, to charge and discharge storage capacitor C_B and to regulate the output voltage. An improvement is obtained if switch S_2 is moved to the secondary side, in series with freewheeling diode D, leaving a simple diode in its place. In this way, the transformer leakage inductance is naturally clamped by the bulk capacitor.

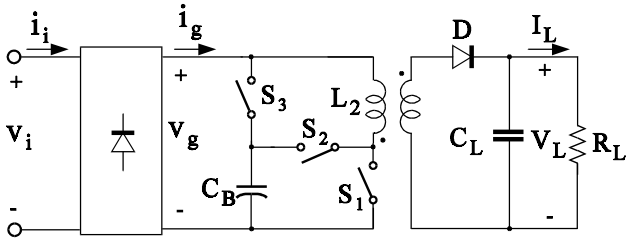


Fig.9 - Flyback parallel PFC converter

e) BIFRED and BIBRED topologies

These topologies, shown in Fig.10a and 10b, can be derived by the cascade connection of a boost converter and a flyback (BIFRED - Boost Integrated with Flyback Rectifier/Energy storage/Dc-dc converter) or buck (BIBRED - Boost Integrated with Buck Rectifier/Energy storage/Dc-dc converter) dc/dc converter [14]. In practice, the converters shown in Fig.10 are simply a Sepic and a Cuk scheme with the addition of an input diode (which is always present owing to input bridge rectifier).

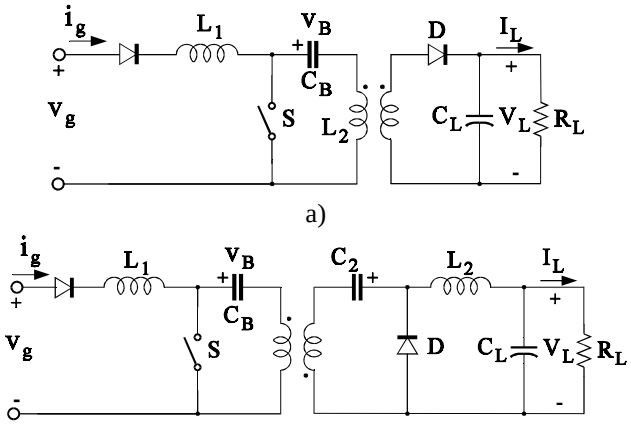


Fig.10 - a) BIFRED converter; b) BIBRED converter

The main differences are that operation is in the discontinuous input current mode and energy storage is done by internal capacitor C_B. In this way, high power factor and fast output voltage regulation are achieved with one switch only. The main drawback, once again, is the dependence of voltage V_B across C_B on the load, and the consequent high voltage stress at light load. As already suggested for the dither rectifier, one way to overcome this problem is to use variable-frequency control together with duty-cycle control [15]. An alternative approach is to operate with discontinuous current also in the second inductor (as done in the S^2IP^2 family).

If other BIBRED topologies having more switches are considered, it is possible to use the additional degrees of freedom to control also the voltage stress [16].

By adding another switch in the converter output stage, a decoupled control of both input current and output voltage is achieved. This approach leads to a new converter family named *capacitive idling converters* [17-18].

5. MEDIUM-POWER PFC TOPOLOGIES

This section embodies a brief review of single-stage PFC's topologies with high-frequency insulation suitable for medium power applications.

a) Insulated boost converter

The boost topology is one of the most popular for PFC applications. It offers many advantages, namely low-distorted input current and almost unity power factor with simple control, minimum circuitry and ground-connected switch. However, it has some drawbacks, namely, difficult implementation of high-frequency insulation, start-up overcurrents, lack of current limitation during overload and short-circuit, output voltage always greater than peak input voltage.

Insulated versions of the boost converter for single-phase power factor correction are discussed in [19-20-21]. Fig. 11 gives the circuit diagram of the insulated full-bridge topology [20-21].

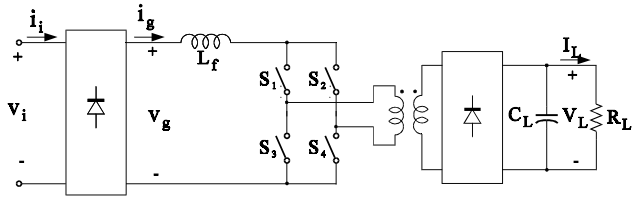


Fig.11 - Insulated boost full-bridge converter.

The bridge circuit operates alternatively in the boost mode (S1 S3 or S2 S4 on, so that the inverter is short-circuited) and in the inverting mode (S1 S4 or S2 S3 on), so that the high-frequency transformer works properly. A sinusoidal wave shape of the line current is obtained by modulating the duration of the boost and inverting intervals.

Similar results are obtained by the scheme shown in Fig.12 [19], where two switches and two windings are used on the primary side. The operation resembles that explained previously, but the auxiliary winding of the input inductor is connected to the output through a diode, so that both switches can be off together and the inductor energy is transferred into the output capacitor. This avoids the typical problems related to transient operation of the boost topology.

In these topologies overvoltages occur due to transformer leakage inductance, so that snubber or clamp circuits must be used.

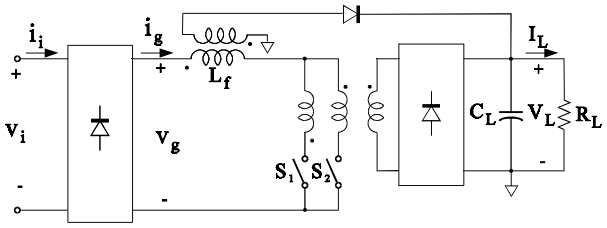


Fig.12 - Two-switch insulated boost converter

b) Cuk and Sepic Converters

As compared to boost or flyback, Cuk and Sepic PFC's are less popular due to their higher complexity. However, they overcome some basic limitations of other topologies, providing current limit and overload protection, step-up and step-down regulation, easy high-frequency insulation.

Fig.13 shows Sepic and Cuk topologies: the input section resembles that of a boost converter, while in the output section the Cuk converter is similar to a buck stage and the Sepic resembles a flyback. A major difference lies on transformer utilization: in Cuk converters the magnetizing inductance does not carry a dc current component, so that the transformer can be fully utilized, while in Sepic converters the average magnetizing current equals the output current. In both schemes, the leakage inductances cause overvoltages on the switch, so that a voltage clamp is needed. Soft switched solutions are also possible [22].

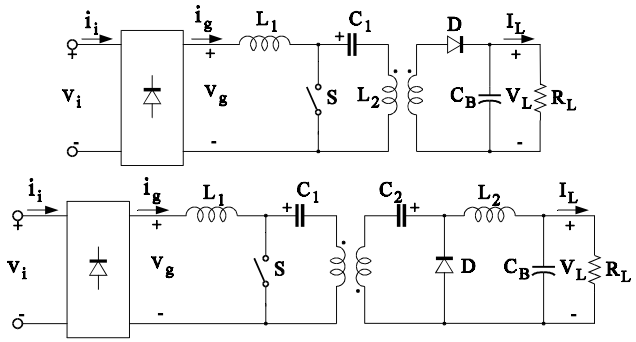


Fig.13 - Sepic and Cuk converters.

It is interesting to note that, with a proper choice of the inductances, the line current of Cuk and Sepic converters remains continuous even if the converter operates in the discontinuous conduction mode [23], thus reducing input filter requirement. When operated in the continuous conduction mode (CCM), an internal current loop is needed to force a sinusoidal current absorption; it must be carefully designed in order to avoid control instabilities [24].

Advantages can be gained by magnetically coupling the two inductors [25-27]. In this case, only one magnetic core is needed saving size and cost; moreover, by a proper design of the magnetic structure the high frequency input current ripple can be greatly reduced.

c) Resonant converters

Fig. 14 shows a load-resonant ac/dc converter [28]. A high power factor is obtained without active control of the input current provided that a small dc link capacitor is used. This derives from the pulsating nature of the dc link and the inherent capability of the converter to boost the voltage conversion ratio during the valleys of the ac input voltage. This latter condition holds for parallel resonant converters and for the series-parallel combination (LCC stage), while it is not true for series resonant converters. A higher power factor can be obtained by controlling the inverter frequency so as to achieve input current shaping.

The resonant approach allows high power density, high switching frequency and low EMI due to the soft commutations and smoothed current and voltage waveforms.

In resonant converters the transformer is fully utilized and the leakage inductances do not disturb, since they are part of the resonant path. Moreover, inherent short circuit protection is provided by series impedances L_r and C_S.

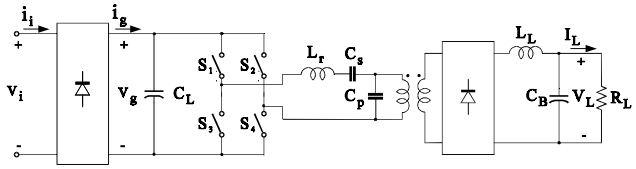


Fig. 14 - LCC full-bridge resonant PFC

d) Parallel power factor correction schemes

This approach, already explained in the previous section, show its full potentialities in high- and medium-power applications. The schemes incorporate two stages working in CCM, and offer high efficiency, high power factor and tight output voltage regulation.

A scheme based on parallel power processing, suitable for medium-power applications, is shown in Fig.15 [12]. As compared to a two-stage PFC, power stage complexity does not increase significantly, while regulator design and other control issues (i.e., switch timing) are difficult. Moreover, two high-frequency transformers are needed; solutions using a single transformer are possible only with discontinuous input current [13].

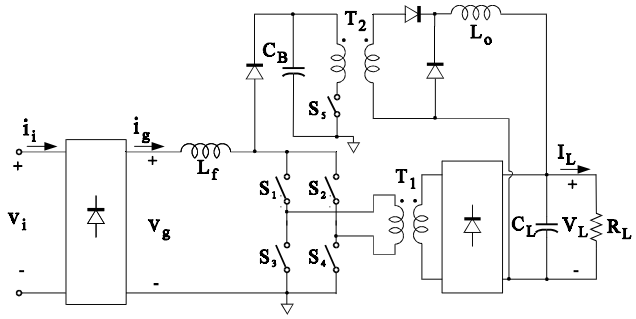


Fig. 15 - Full-bridge boost parallel PFC

6. REVIEW OF PFC CONTROL TECHNIQUES

Power factor correction is achieved by proper line current shaping, therefore an active control of the line current is generally needed (*current control*). Input current control can be avoided only with DCM operation (*Discontinuous current PWM control*) or in the boundary condition between Continuous and Discontinuous Inductor Current Mode (*Borderline control*), where an automatic power factor correction occurs.

1) Current control techniques

A suitable sinusoidal current reference signal is generated by multiplying a scaled version of the rectified line voltage with the output of a voltage error amplifier, which adjusts the magnitude of the current reference.

Several current-control methods are available for the active control of the line current:

a) Average current control. It is very popular for the good performances [3]. The inductor current is sensed, compared to its reference and filtered by a current error amplifier, whose output drives a PWM modulator (Fig.16). This control features constant switching frequency, no need of compensation ramp, commutation noise insensitivity, small input current distortion.

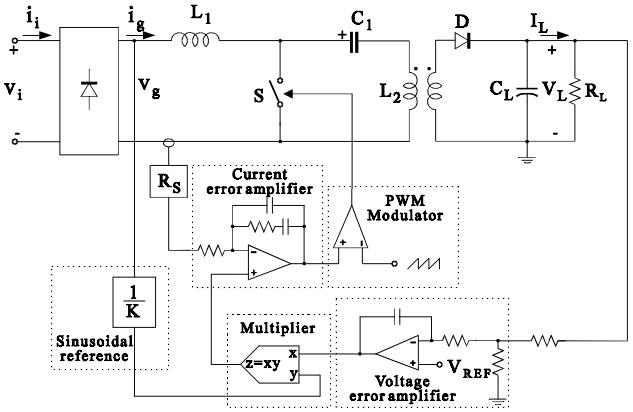


Fig.16 - Average current control scheme

b) Peak current control. In this control [29,30], the switch is turned on at constant frequency, and is turned off when the inductor current (i.e., switch current) reaches the sinusoidal current reference. This control provides true switch current limitation at the expense of a higher input current distortion. It also requires provisions (ramp compensation) to avoid instabilities [3].

c) Hysteresis control. With this type of control two sinusoidal current references are generated, one for the peak and the other for the valley of the inductor current [31]. According to this control technique, the switch is turned on when the inductor current goes below the lower reference and is turned off when the inductor current exceeds the upper reference, giving rise to a variable frequency control. The main advantage is the extreme robustness and stability of the control.

2) Borderline control

As shown in Fig.17, in this control approach the switch on-time is held constant during the line cycle and the switch is turned on when the inductor current falls to zero, so that the converter operates at the boundary between Continuous and Discontinuous Inductor Current Mode (CICM-DICM) [32]. The instantaneous input current is therefore constituted by a sequence of triangles whose peaks and average values are proportional to the instantaneous line voltage.

The switching frequency varies over the line period and is also strongly influenced by the load current.

3) Voltage-follower approach

This approach refers to those topologies where power factor correction can be achieved without duty-cycle modulation during the line cycle [2]. It is therefore applicable to those topologies, like flyback, Cuk and Sepic converters operating in DCM, which automatically draw an input current proportional to the line voltage, so that no active control of the line current is needed to produce unity power factor.

Due to DCM operation, controller design is relatively easy, since only the output voltage must be regulated, while the internal current loop is completely eliminated.

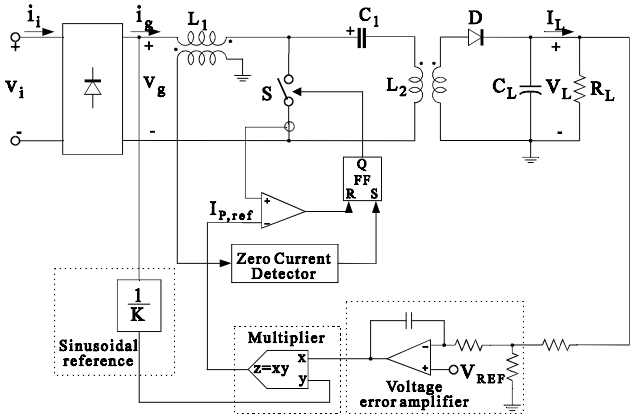


Fig. 17. Borderline control scheme

7. CONCLUSIONS

An overview of single-phase ac/dc converters featuring high power factor and high-frequency insulation has been presented. A selection of topologies useful for various power levels has been discussed, with particular attention to those providing fast output voltage regulation.

Lastly, PFC control techniques have been briefly reviewed.

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