POWER FACTOR PREREGULATORS WITH IMPROVED DYNAMIC RESPONSE

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Abstract. **A improved control strategy of standard Power Factor Preregulators (PFP's) is proposed, which allows fast output voltage response while maintaining a high power factor. This is obtained by compensating for the intrinsic low-frequency output voltage ripple, thus allowing a higher bandwidth of the output voltage control loop.**

This method does not require additional sensing, but only a multiplier and simple analog circuitry, and works well with universal input voltage range.

Experimental tests on a boost converter with average current control confirm the validity of the approach.

I. INTRODUCTION

In the attempt to meet standard regulations and recommendations (like IEC 555-2), many rectifier topologies were proposed, which provide almost unity power factor. In these converters the main effort is devoted to the quality of the input current waveform while, especially with simple single-switch topologies like the Boost one, the dynamic response of the output voltage is sacrificed [1]. In fact, due to the input power fluctuation, the output voltage contains a low-frequency ripple at twice the line frequency which affects the input current waveform unless the voltage loop bandwidth is kept well below the line frequency (typically 20 Hz).

Many techniques have been proposed in literature in order to overcome this problem: for example in [2] the use of sliding mode control was proposed, which allows faster response to the detriment of a higher input current distortion.

Most of the proposed solutions are aimed to remove the low-frequency ripple from the feedback signal so as to allow a higher voltage loop bandwidth. For example, in [3] different techniques like notch filters, sampling networks and the so called "regulation band approach" were analyzed. These solutions have the advantage of a limited increase of the controller complexity and, above all, they do not require additional sensing devices. The main limitation is represented by the moderate improvement achievable in the output voltage dynamic.

Better performances can be obtained by using ripple compensation techniques like those proposed in [4,5]. In these solutions the drawbacks are represented by the need of a precise load power estimation, which requires sensing of the load current, and an increased control complexity (multipliers/dividers, PLL, estimators etc.).

This paper presents a solution based on the ripple compensation technique, which allows a good compromise between dynamic response and control complexity.

The proposed approach features:

- no need of additional sensing;
- good output voltage ripple estimation, even in the presence of distorted line voltage;
- universal input voltage range;
- limited control complexity;
- a voltage loop bandwidth in the range 100-200Hz, which avoids significant input current distortion in the presence of small errors in the ripple estimation while still giving satisfactory performances in terms of speed of response and overshoot limitation.

The added control complexity is limited to a multiplier (besides the one needed to build the input current reference signal) plus simple analog circuitry, which can easily be integrated with the standard control in a single IC.

The approach is general, in the sense that it can be applied to any PFP with current mode control; the boost converter is taken as an example.

Issues regarding the impact of a non-perfect ripple compensation on the input current waveform are analyzed and design criteria for the voltage loop compensator are also given. Experimental results of a boost converter with average current control confirm the validity of the approach.

II. BASICS OF PFP

A boost PFP with current control is shown in Fig.1 [1]. The rectified line voltage v_g is sensed and then multiplied by output $I_{REF}^*(t)$ of the voltage error amplifier to form sinusoidal current reference I_{REF}. Then, a large-bandwidth current loop forces the input current to follow, as close as possible, its reference, i.e.:

$$i_g(t) = I_{REF}^*(t) \cdot v_g(t) \qquad (1)$$

The voltage loop keeps the average output voltage V_o near voltage reference V_{REF}, by adjusting $I_{REF}^*(t)$ so as to vary the amplitude of the input current.

In the assumption of unity power factor and negligible input inductor energy, the fluctuating input power causes a low-frequency voltage ripple Δv_o across C_o which depends only on the load current and is given by:

$$\left|\Delta v_o(t)\right| = \frac{I_o}{2\omega_f C_o}\cdot\sin(2\omega_f t) = \frac{P_o}{2\omega_f C_o V_o}\cdot\sin(2\omega_f t) \quad (2)$$

where ω_f is the line angular frequency (rad/s) and P_o the output power. This holds provided that the voltage loop has a bandwidth well below the line frequency in order to avoid variation of $I_{REF}^*(t)$ within the line cycle, which would cause input current distortion.

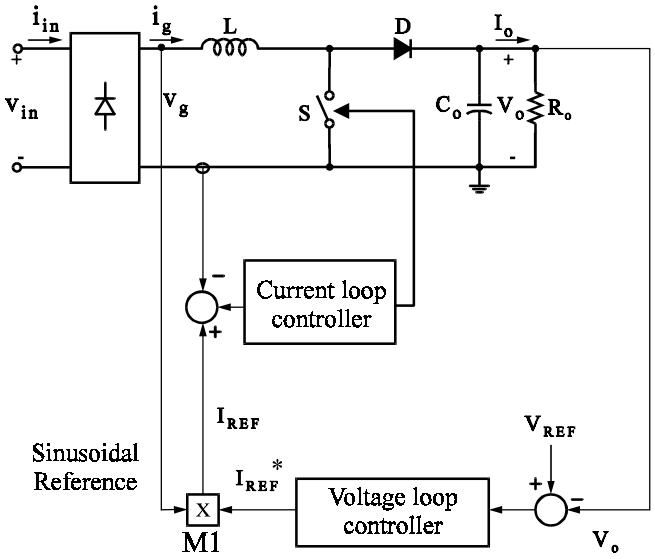

Fig. 1. Power Factor Preregulator basic scheme.

III. Proposed Control Scheme

In the steady state, output voltage $v_o(t)$ is composed by a DC value V_o equal to V_{REF} and a ripple component $\Delta v_o(t)$ given by (2), i.e. $v_o(t)=V_o+\Delta v_o(t)$.

The proposed control scheme is based on the principle of output voltage ripple cancellation [4,5]. This means that ripple $\Delta v_o(t)$ is estimated and subtracted to $v_o(t)$, so that the voltage error amplifier processes a ripple-free signal.

According to (2), estimation of $\Delta v_o(t)$ requires a sinusoidal waveform at twice the line frequency with an amplitude proportional to the output power. In the literature [4,5] signal $\Delta v_o(t)$ is generated by using a PLL, which gives the waveform $\sin(2\omega_f t)$ and by sensing the load current to produce a signal proportional to the load power. Besides the use of an additional sensing, the drawback of this approach is that it works well only with a pure sinusoidal line voltage, since the presence of harmonics in the input voltage causes the ripple signal to deviate from (2).

This paper presents an alternative approach to estimate $\Delta v_o(t)$: in fact, under unity power factor assumption, the input power is given by:

$$p_{in}(t) = v_g(t)\cdot i_g(t) = P_{in} - \frac{\eta P_o}{2}\cdot\cos(2\omega_f t) \quad (3)$$

where η is converter efficiency and $P_{in}=\eta P_o$ is average input power. Comparison between (2) and (3) shows that $\Delta v_o(t)$ can be estimated from the signal $p_{in}(t)$ by eliminating the DC component P_{in}, multiplying the result by a proper gain and phase shifting by ninety degree.

These operations can be provided by the simple compensation network:

$$G_C(s) = K_C\cdot s \quad (4a)$$

where K_c is:

$$K_c = \frac{1}{2\eta\,\omega_f^{\,2} C_o V_o} \quad (4.b)$$

Fig. 2 shows the basic scheme: the input power signal (3) is obtained by multiplying (M2) rectified input voltage v_g by reference current I_{REF}, which is used instead of i_g in the assumption of a large current loop bandwidth. Then, block G_C provides the estimated ripple signal $\Delta v_{oest}(t)$ which is finally subtracted to $v_o(t)$, thus providing a ripple free signal for the voltage error amplifier.

Since the reconstructed ripple signal is proportional to the power, as requested by (2), its action is not affected by load and/or input voltage variations; the PFP can therefore be used

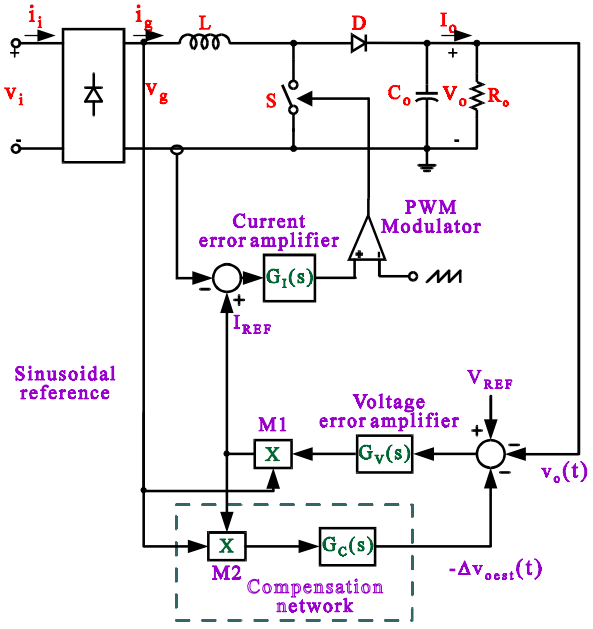

Fig. 2. Boost PFP with proposed output voltage ripple cancellation scheme.

with a wide input voltage range.

It is worthwhile to observe that network $G_C(s)$ may cause errors in the estimation of $\Delta v_o(t)$ due to the presence of the derivative action, especially in the case of a significant harmonic content in the input voltage. In fact while the power stage output filter R_o-C_o attenuates higher harmonics in the output voltage ripple, network G_C performs an opposite

action, thus increasing the harmonic content in the estimated signal.

In order to overcome this problem the compensation network $G_C(s)$ must provide:

a) ninety degrees phase shift
b) elimination of the DC term
c) first-order attenuation of higher harmonics (similarly to the R_O-C_O filter).

These goals can be accomplished by using a band-pass filter tuned at twice the line frequency (which satisfies points b) and c)) followed by a phase shifting network to satisfy point a) (this latter can be implemented by means of a couple negative real pole-positive real zero at the same frequency $2\omega_f$).

IV. Controller Design

This section embodies some considerations useful for a preliminary controller design.

A. Current loop design

As shown in Fig. 2, in the average current mode control the input inductor current i_g is sensed, compared to a sinusoidal reference value I_{REF} and then processed by a suitable current error amplifier $G_i(s)$, which generates the proper driving signal for the switch by comparison with a fixed ramp. The current error amplifier generally proposed in literature has a transfer function with two poles and one zero, i.e.:

$$G_i(s) = \frac{\omega_i \cdot (1 + s/\omega_z)}{s \cdot (1 + s/\omega_p)} \tag{5}$$

where ω_p is placed above half the switching frequency to filter out the high-frequency ripple of the sensed inductor current. Integrator gain ω_i and zero ω_z are chosen to give the desired bandwidth and phase margin to the current loop [1].

B. Voltage loop design

The voltage loop controller keeps the average output voltage V_O close to constant reference voltage V_{REF}, by properly adjusting the amplitude of the inductor current reference. A model applicable for frequencies below the line frequency and useful for designing the voltage error amplifier can be found in [6]; however this model is no longer valid for frequencies above the line frequency.

According to [3], a different model can be obtained by averaging over a switching cycle the converter equations and then using a small-signal approximation. In the assumption of negligible low-frequency voltage drop across the input inductance, the transfer function between I_{REF}^* and v_o is:

$$G_P(s) = \frac{v_o(s)}{I_{REF}^*(s)} = K_B \cdot \frac{1 - s\tau_z}{1 + s\tau_p} \tag{6}$$

where:

$$K_B = \frac{R_o}{V_o} \cdot \frac{\left(V_{gP} \sin(\theta)\right)^2}{2 - \cos(2\theta)} \tag{7}$$

$$\tau_z = \frac{2 L P_o}{V_{gP}^{\,2}} \tag{8}$$

$$\tau_p = \frac{R_o C_o}{2 - \cos(2\theta)} \tag{9}$$

where $\theta = \omega_f t$ and V_{gP} is the peak value of the rectified input voltage.

Eqs. (6-9) hold for resistive load; similar relations can be found for constant-power load by simply taking an infinite R_O in (6-9).

As we can see, while the RHP zero in $G_P(s)$ is independent of angle θ, the gain and the pole depend on it. Consequently, this model is not useful for designing the compensator network of a PFP unless a simple proportional controller is considered: in this case stability criteria can be obtained [7], but any integral action inside the controller makes very complex a stability analysis.

Following [8], a simple and accurate small-signal model for boost high power factor converters with constant switching frequency can be derived; in [8] it is shown that for frequencies below the current loop cross-over frequency the following time-invariant linear model G_P holds for resistive load:

$$G_P(s) = \frac{v_o(s)}{I_{REF}^*(s)} = \frac{R_o}{2} \frac{V_{gRMS}^{\,2}}{V_o} \frac{1 - s\tau_z}{1 + s\frac{R_o C_o}{2}} \tag{10}$$

Model (10) corresponds to (6) for $\theta = \pi/4$. It is interesting to note that this choice corresponds to averaging in (6-9) all the time-varying terms, as it was proposed in [3]. Note also that, whenever τ_z can be neglected, model (10) corresponds to that obtained in [6]. Similar considerations arise when a constant-power load is analyzed.

According to (10), as long as τ_z is negligible (as it normally does), the voltage loop controller can be designed to have a bandwidth up to $f_i/5$, where f_i is the bandwidth of the current loop, so that the assumption of perfect tracking of I_{REF} holds. Even though this approach is possible in theory, as it was proposed in [4], the effect of a non-perfect compensation of the output voltage fluctuating term must be also taken into account. As a consequence, the analysis reported in section V demonstrated that a reasonable trade-off between input current distortion and speed of response yields to a 100-200Hz voltage loop bandwidth range.

Note that the design of the voltage loop PI controller based on (10) holds in the assumption of neglecting the dynamic effect of the compensator loop; in fact, the scheme of Fig.2 cannot be considered a feedforward action because of the loop formed by the two multipliers M1 and M2, the voltage

error amplifier and the compensation network. However, simulations showed that the compensator loop does not introduce any instability problem and does not affect appreciably the converter dynamic behavior.

V. Performance Evaluation of the Compensator Network

The analysis of the impact of a non-perfect compensation on input current distortion can be done through the block diagram of Fig. 3, which shows both voltage and compensator loop.

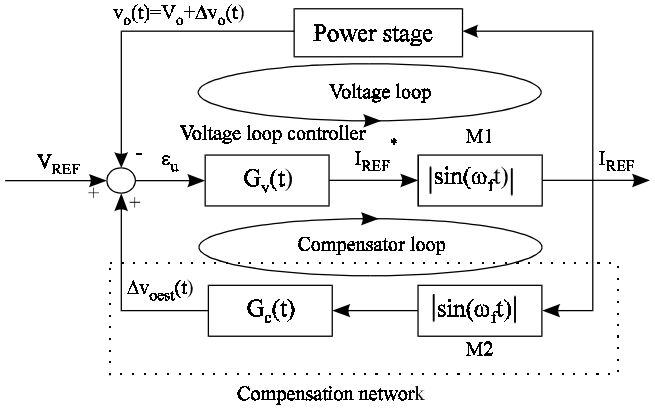

Fig. 3. Block scheme of the ripple compensation network

In the steady state ($V_o=V_{REF}$) a perfect ripple estimation ($\Delta v_o(t) = \Delta v_{oest}(t)$) keeps $\varepsilon_u(t)$ to zero, so that I_{REF}^* is constant and I_{REF} is free of any distortion; whenever an estimation error occurs ($\Delta v_o(t) \neq \Delta v_{oest}(t)$), some harmonic terms appear in $\varepsilon_u(t)$ and thus in I_{REF}^*, each of them contributes to create other harmonics through multiplications by the time-varing terms $|\sin(\omega_f t)|$.

Expressing $\varepsilon_u(t)$ in Fourier series and considering a limited number of harmonics, following the block scheme of Fig. 3, the harmonic content of I_{REF} is obtained. Then, the input current Total Harmonic Distortion (THD) is derived from the harmonic content of I_{REF} in the assumption of perfect tracking of the current loop control.

A. Effects of voltage loop bandwidth on input current distortion

Following the approach outlined above, the diagram of Fig. 4 was derived; it shows input current distortion (THD) versus voltage loop bandwidth for an amplitude relative error ζ of 5% and 15% in $\Delta v_{oest}(t)$ when a P-I compensator with 60 degrees of phase margin is used. As expected, the THD rapidly increases when the bandwidth increases, thus imposing a trade-off between the needs of high power factor and fast dynamic response.

Fig. 4 shows that a voltage loop bandwidth between 100-200Hz is a good choice.

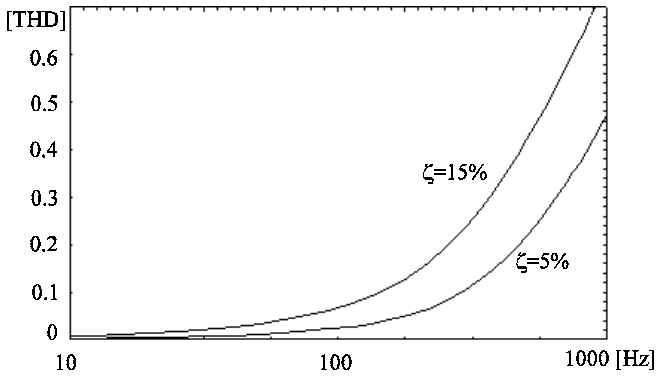

Fig. 4. Input current Total Harmonic Distortion (THD) versus voltage loop bandwidth for a specified amplitude relative error ζ in $\Delta v_{oest}(t)$,

B. Magnitude Errors on $\Delta v_{oest}(t)$

In order to estimate $\Delta v_o(t)$ with the right amplitude, gain K_c must have the value given by (4.b).

While output voltage V_o is fixed and line frequency ω_f does not change significantly, the accuracy of determination of efficiency and output capacitance can be low. In particular:

- being the output capacitor of the electrolytic type it has a wide tolerance; moreover, its value may change with temperature;
- the efficiency depends not only on power stage topology and components, but also on output power level; this means that the efficiency value in (4b) must be referred to the rated power in order to perform the best compensation in the nominal condition; however when the power decreases, the compensation get worse.

The effect on the input current THD caused by an estimation error on $\Delta v_{oest}(t)$ is shown in Fig. 5, where the voltage loop bandwidth is kept constant at 100Hz: as we can see, with this choice, the THD is limited to 5% when the relative error ζ is 10%.

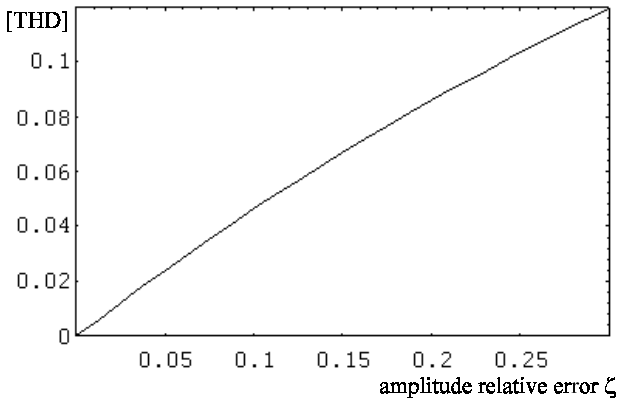

Fig. 5. Input current THD versus amplitude relative error ζ in $\Delta v_{oest}(t)$ (voltage loop bandwidth=100Hz)

C. Phase Errors

Some phase shift may occur in the compensating signal mainly due to:

- non correct phase shift introduced by compensator G_C;
- low current loop bandwidth, which causes actual input current to deviate from reference I_{REF}.
- non negligible inductor energy as compared to the mean input power so that (2) is no longer valid. In this case a phase shift φ appears, which is given by:

$$\varphi = \operatorname{arctg}\left(\frac{\omega_f \, L I_{inRMS}^2}{V_{inRMS} \, I_{inRMS}}\right) \qquad (11)$$

where V_{inRMS} and I_{inRMS} are the RMS value of the input voltage and inductor current respectively.

The effect on the input current THD due to a phase shift error on $\Delta v_{oest}(t)$ is shown in Fig. 6, where the voltage loop bandwidth is still kept at 100Hz: as we can see, the distortion remains within reasonably limits at moderate phase shift errors.

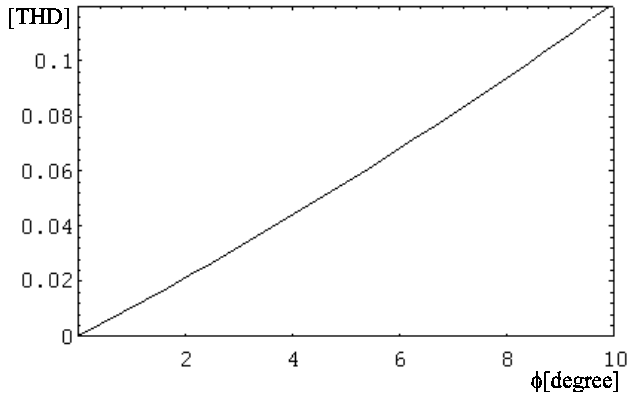

Fig. 6. Input current THD versus phase error ϕ [degree] on $\Delta v_{oest}(t)$ (voltage loop bandwidth=100Hz)

D. Non sinusoidal conditions

If the input voltage is non sinusoidal, the input current gets distorted, causing higher harmonics to appear in $\Delta v_o(t)$; since the harmonics in the input power are filtered out by the output R_O-C_O filter, problems may arise when compensator (4) is used due to its derivative action, which amplifies the harmonics in the input power. This problem is avoided by using the alternative compensator network proposed at the end of section III, which better emulates the power stage behavior.

VI. Experimental Results

A boost PFP with average current mode control was implemented and tested. The parameters are reported in table I.

Table I - Converter parameters

V_g=220V_{RMS}	V_o=380V	f_s=70kHz
L=500μH	C_o=470μF	R_o=260Ω

In order to test the performance improvement due to the proposed compensation scheme, two different controllers were implemented: one following standard rules without compensation network [1] and the other according to the proposed control strategy.

In both cases, the following regulators are used:

$$G_I(s) = K_I \cdot \frac{(1+s\tau_{zi})}{s \cdot (1+s\tau_{pi})} \qquad (12)$$

$$G_V(s) = K_V \cdot \frac{(1+s\tau_{zv})}{s \cdot (1+s\tau_{pv})} \qquad (13)$$

The current amplifier parameters are chosen in order to have a crossover frequency equal to 2kHz and a phase margin of 60 degrees. For the voltage amplifier, the crossover frequency is 20Hz for standard design and 100Hz for compensated control scheme, while the phase margin is 60 degrees for both.

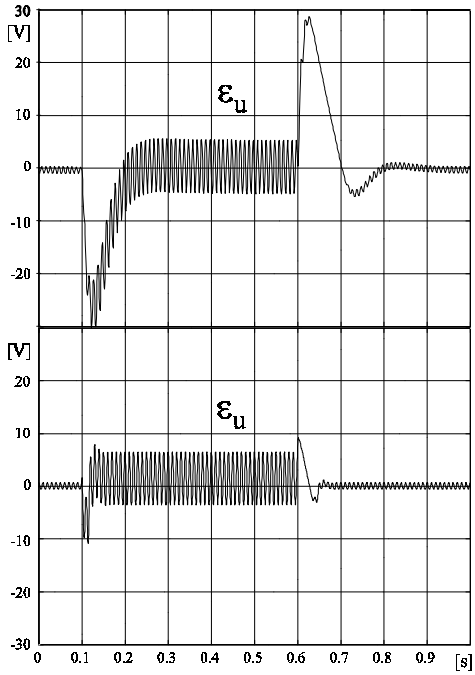

Fig. 7 - Output voltage behavior at load step change. (10%-100% of the nominal load).
a) standard control with no compensation;
b) proposed compensation scheme

In Fig.7 the output voltage behavior for a load variation from 10% to 100% of rated power and vice versa is reported: a comparison between standard approach and compensated scheme reveals that both deviation from reference value and settling time are considerably improved by using the proposed compensation scheme. Note also that the overshoot at load disconnection is just slightly higher than ripple amplitude at rated power.

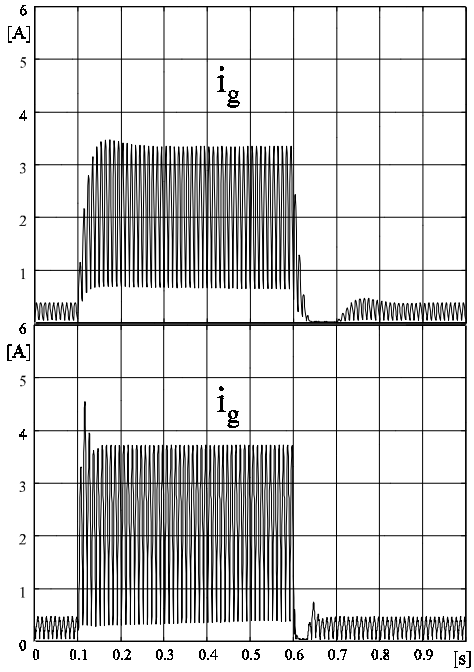

Fig.8 - Rectified input current behavior at step load change (10%-100% of the nominal load).
a) standard control with no compensation
b) proposed compensation scheme

The rectified input current in the same conditions is reported in Fig.8. It is worthwhile to observe the different current amplitudes measured with the two control schemes: in fact, in the prototype with standard controller a higher third harmonic is present in the input current, which causes a reduction of the current amplitude for the same power.

This fact is revealed also by a comparison of the normalized line current spectra reported in Fig.9: the higher input current distortion with standard controller reveals a too high voltage loop bandwidth and/or a poor attenuation of $G_V(s)$ at twice the line frequency.

The effect of the compensating network is shown in Fig.10 which reports the low-frequency output voltage ripple before and after compensation: as we can see the ripple is not perfectly cancelled, even after tuning the gain of $G_C(s)$. This is caused by the tolerance in the filter parameters of $G_C(s)$ which introduces a phase shift in the compensating signal. The line voltage and input current waveforms are shown in Fig.1: voltage THD is 3.2%, while current THD is 4.2%. The power factor is 0.998%.

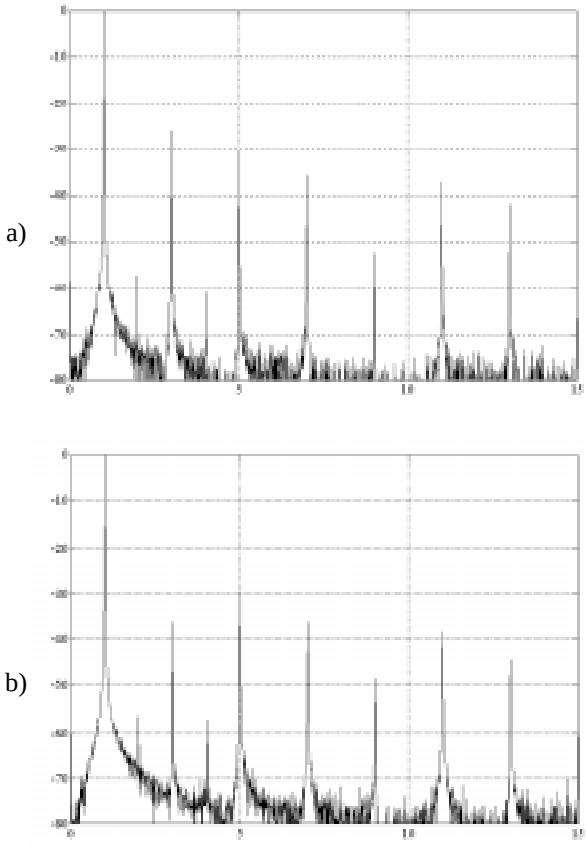

Fig 9. - Normalized line current spectrum. a) Standard controller b) Control with ripple compensation

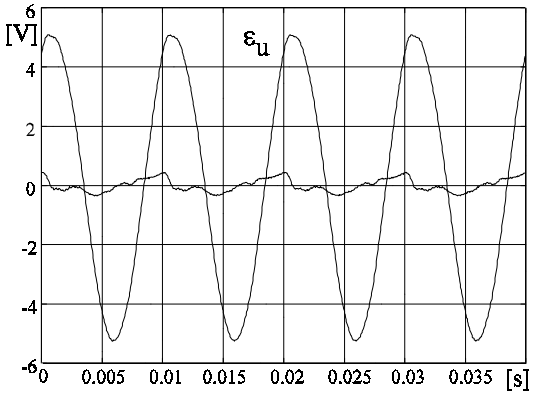

Fig. 10 - Low-frequency output voltage ripple before and after the compensation action

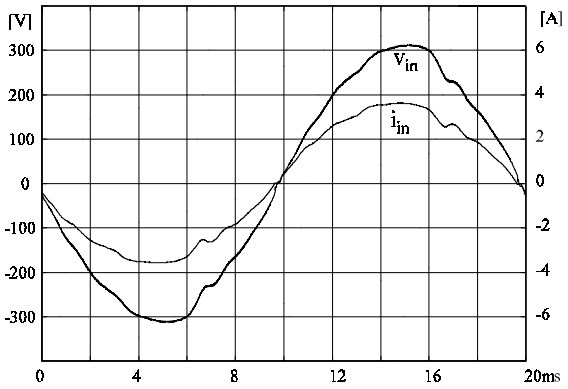

Fig. 11 - Line voltage and current waveforms.

VII. Conclusions

A compensation scheme for the low-frequency output voltage ripple of standard PFP's is proposed, which allows fast response to load step changes and high power factor. This solution does not require additional sensing devices, but only a multiplier and simple analog circuitry. Moreover, it works properly in a wide input voltage range.

Experimental results of a Boost PFP with average current control confirm the validity of the approach.

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