HIGH-QUALITY RECTIFIER FOR RESISTIVE LOADS

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Abstract. A high-quality rectifier for supplying resistive loads is presented. It features high power factor, low input current distortion and high efficiency.

It is a step down converter and its device stresses are the same as for a buck converter, while input current is continuous.

The converter, suitable for heating and lighting applications, is analyzed and experimentally tested on a 1kW prototype.

I. Introduction

For several home appliances, electromechanical control devices are being substituted by electronic power supplies, which offer superior performances at a comparable cost. In particular, feeding resistive loads, for lighting and heating applications, by switching power supplies gives several benefits: continuous power regulation, accuracy irrespective of line voltage variations, protection against short-circuits and open-circuits, power limitation.

On the other hand, electronic power supplies must be carefully considered as regards efficiency, reliability, harmonic distortion, EMI. Common requirements for resistive loads are: supply from the utility line; high power factor; low harmonic distortion of the input current; low conducted and radiated noise (EMI); output power regulation from a few percent to 100% of rated power; high power density; limited power loss.

The care reserved to the utility line interface comes from the attempt to meet standard regulations and recommendations (like IEC 1000-3-2) while the difficult environmental conditions, in terms of space and ambient temperature, in which these power supplies may work (consider for instance heating loads in cooking equipment) call for high power density and efficiency.

In the following, a simple high-quality rectifier for supplying resistive loads is presented. All operation modes are analyzed in detail and suitable design criteria are derived. Then, experimental results of a 1kW prototype are also reported, showing actual converter performances.

II. Circuit Description

Observe first that, in the considered application domain, the need for low cost and high reliability discourage the use of complex topologies.

Moreover, in order to get low input current distortion in a cheap way, topologies with inherent input filtering, like those having an input inductance, are

preferable. Finally, control of resistive loads calls for step-down converters.

These constraints have lead to the choice of the circuit shown in Fig.1. It consists of a diode bridge rectifier followed by a switching cell which is simply obtained by a cyclic rotation of the Cuk cell [1-2]. As shown in [1-2], this particular connection of supply and load yields a non-inverting step-down converter with the same device stresses of a buck converter. However, due to the presence of two inductors and the diode bridge rectifier, more operation modes are possible. In fact, besides the usual Continuous Conduction Mode (CCM) and Discontinuous Conduction Mode (DCM), the converter can work in Discontinuous Input Current Mode (DICM) in which only the input diodes stop conducting during the switch off-interval, and in Discontinuous Input and Output Current Mode (DIOCM), characterized by discontinuous inductor currents. Both these latter operation modes lead to different fundamental relations as compared to the buck converter, and a correct understanding of the converter behavior in all these conditions is needed for proper design.

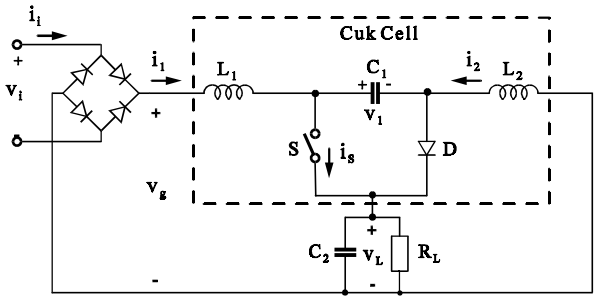

Fig.1 - Proposed converter scheme

It is important to note that, for our application, the instantaneous output voltage, as well as the output power, is allowed to vary during the line cycle, since the goal is to control the average power supplied to the load. Thus the low-frequency energy storage element present in all ac/dc converters can be avoided, reducing size and cost

At full power the switch can be kept close, thus avoiding the commutation losses.

III. Analysis of Operation modes

In the following analysis, with the hypothesis of switching frequency much higher than line frequency, the "quasi-static approach" is used, in which each switching period is studied as the circuit was in the stationary state corresponding to a dc supply voltage equal to v_g. In practice, v_g changes slowly according to the relation:

$$v_g(\theta) = V_i \cdot |\sin(\theta)|, \theta = \omega_l t \qquad (1)$$

where ω_l is the line radiant frequency. Consequently, any current and voltage in the circuit has a sinusoidal waveshape, since each reactive element will be designed on the switching-frequency basis only. In particular, from the power balance we can write, assuming unity converter efficiency:

$$v_g(\theta)\cdot \bar{i}_1(\theta) = \frac{\bar{v}_L^2(\theta)}{R_L} \Rightarrow \bar{i}_1(\theta) = \frac{M^2}{R_L} V_i |\sin(\theta)| \qquad (2)$$

where $M = \frac{\bar{v}_L(\theta)}{v_g(\theta)} = \frac{V_L}{V_i}$ is the voltage conversion ratio and overbar means averaged quantities in a switching period. Thus, high power factor is achieved at constant duty-cycle and switching frequency.

The relations and converter waveforms given hereafter will be valid provided that the high-frequency voltage ripple across capacitors C_1 and C_2 is neglected.

CCM Operation

Fig.2 reports the main converter waveforms during a switching period for the case of CCM operation.

As we can see, both inductor currents are continuous and the converter equations are the same of the usual buck topology. Both switch and freewheeling diode carry the sum of the two inductor currents during the on- and off-intervals respectively.

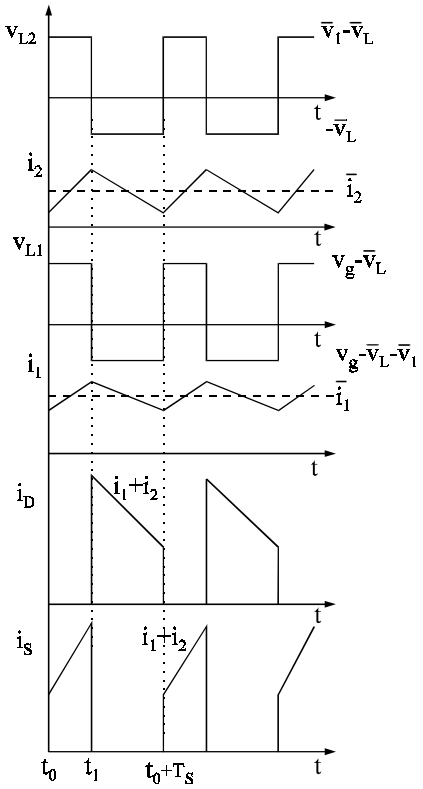

Fig.2 - Main converter waveforms in a switching period (CCM operation)

The volt-second balance applied to inductors L_1 and L_2 gives:

$$\bar{v}_1(\theta) = v_g(\theta) \qquad (3)$$

$$M = \frac{\bar{v}_L(\theta)}{v_g(\theta)} = \frac{V_L}{V_i} = d$$

where d is converter duty-cycle ($dT_S=t_0\div t_1$). It is important to note that, due to the presence of the input diode bridge rectifier, current i_1 must always be greater than zero, leading to the following constraint on inductor L_1:

$$L_1 > \frac{R_L}{2f_S}\cdot\left(\frac{1-M}{M}\right) \qquad (4)$$

where f_S is the switching frequency.

From the waveforms of Fig.2, we can see that during the switch turn-off interval, capacitor C_1 is discharged by the input current. Thus, the relative voltage ripple (peak-to-peak) across capacitor C_1 is derived as follows:

$$r_{V1,CCM} = \frac{\Delta v_1(\theta)}{\bar{v}_1(\theta)} = \frac{M^2(1-M)}{f_S R_L C_1} \qquad (5)$$

As far as the relative output voltage ripple (peak-to-peak) is concerned, we have to take into account that both inductor currents contribute to it. A simple analysis shows that:

$$r_{V2,CCM} = \frac{\Delta v_2(\theta)}{\bar{v}_2(\theta)} = \frac{1-M}{8f_S^2 L_e C_2} \qquad (6)$$

From Fig.2 it is also possible to calculate the peak current in both switch and freewheeling diode:

$$i_{S,peak} = i_{D,peak} = \frac{V_i}{R_L}\cdot M\cdot\left(1+\frac{1-M}{k}\right) \qquad (7)$$

DCM Operation

This operation mode is characterized by the discontinuous freewheeling diode current, as shown in Fig.3. The main difference respect to the buck converter is the non discontinuous input current, since the diode current is the sum of the two inductor currents.

From the analysis of the waveforms of Fig.3 we find that the first of (3) is still valid while the voltage conversion ratio results:

$$M = \frac{2}{1+\sqrt{1+\frac{4k}{d^2}}}, \qquad k = \frac{2L_e f_S}{R_L}, \qquad L_e = \frac{L_1\cdot L_2}{L_1+L_2} \qquad (8)$$

which is the same relation of a buck converter having an inductance equal to L_e.

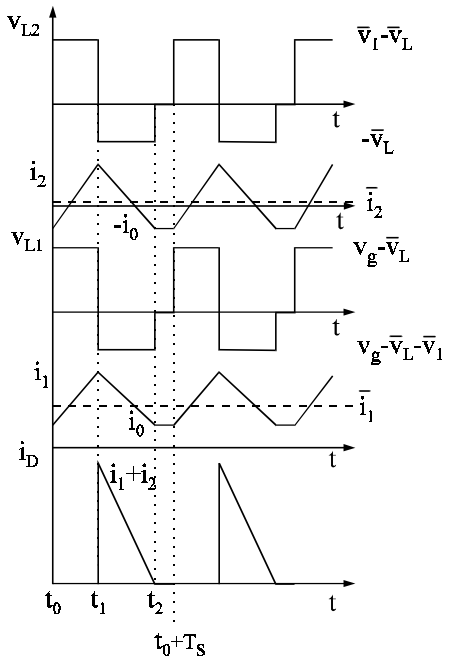

Fig.3 - Main converter waveforms in a switching period (DCM operation)

Note that for the application we are dealing with, parameter k is constant because the load is assigned, while M must vary from zero to one in order to change the power delivered to the load. Thus, the value M_1 corresponding to the boundary between DCM and CCM operation is:

$$M_1 = 1-k \qquad (9)$$

The condition which ensures a current i_1 greater than zero is given by the inequality:

$$\frac{L_1}{L_2} > \frac{1-M}{M} \qquad (10)$$

The relative voltage ripple across capacitor C_1 is found to be:

$$r_{V1,DCM} = \frac{\Delta v_1(\theta)}{\bar{v}_1(\theta)} = \frac{M^2\sqrt{k\cdot(1-M)}}{f_S R_L C_1} \qquad (11)$$

while the relative voltage ripple of the output capacitor results:

$$r_{V2,CCM} = \frac{\Delta v_2(\theta)}{\bar{v}_2(\theta)} = \frac{\sqrt{k\cdot(1-M)}}{8f_S^2 L_e C_2} \qquad (12)$$

The switch and diode current stress is given by:

$$i_{S,peak} = i_{D,peak} = \frac{2V_i}{R_L}\cdot M\cdot\sqrt{\frac{1-M}{k}} \qquad (13)$$

DICM Operation

In this operation mode only the input inductor current is discontinuous.. Fig.4 reports the

corresponding main converter waveforms during a switching period.

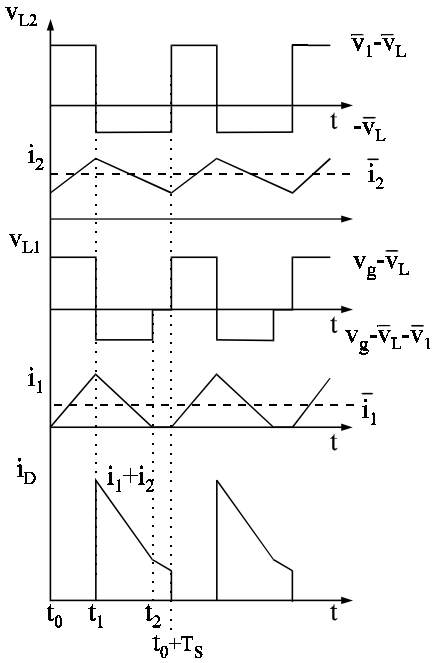

Fig.4 - Main converter waveforms in a switching period (DICM operation)

From the analysis of the converter waveforms the voltage conversion ratio and the voltage across C_1 result respectively:

$$M = d \cdot F(d) \tag{14}$$

$$\bar{v}_1(\theta) = v_g(\theta) \cdot F(d) \tag{15}$$

where

$$F(d) = \frac{(k' - d)}{2k'(1+d)} + \sqrt{\left(\frac{(k' - d)}{2k'(1+d)}\right)^2 + \frac{1}{k'(1+d)}} \tag{16}$$

$$k' = \frac{2L_1 f_S}{R_L}$$

The value of M_3 at the boundary between CCM and DICM operation is given by:

$$M_3 = \frac{1}{1+k'} \tag{17}$$

One important consideration regarding this operation mode is the dependence of the voltage across capacitor C_1 on the duty-cycle (i.e., on the power delivered to the load). As an example, Fig.5 reports the behavior of voltage V_1 normalized to V_i as a function of duty-cycle for a converter designed to change from CCM to DICM operation in correspondence of d≈0.7. As we can see, at light load the voltage stress becomes quite high, making this operation mode not convenient.

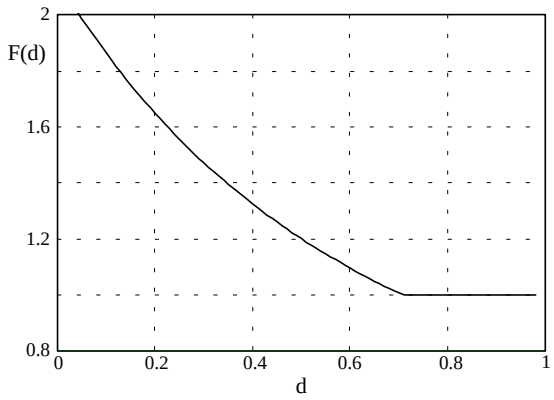

Fig.5 - Voltage across capacitor C_1 normalized to V_i as a function of duty-cycle

DIOCM Operation

This is the last operation mode which can occur and corresponds to the situation in which both inductor currents are discontinuous. The main converter waveforms during a switching period for this operation mode are shown in Fig.6.

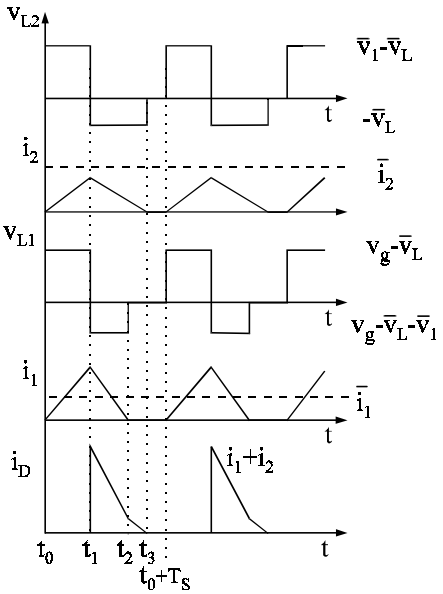

Fig.6 - Main converter waveforms in a switching period (DIOCM operation)

It is not possible to obtain an explicit expression for the voltage conversion ratio M and the voltage across C_1. However, they can be numerically evaluated, and it results a dependence of voltage V_1 on duty-cycle similar to that found in DICM condition.

IV. Power Stage Design Criteria

Before describing the design criteria of the proposed converter, it is worthy to make some

considerations regarding the different operation modes in which this structure can work:

1 - CCM operation ensures the lowest current ripples and thus the minimum current stresses and minimum conduction losses at the expense of high inductance values. However, turn on losses as well as EMI noise increase due to the hard recovery of freewheeling diode.
2 - DCM operation causes high current ripple with increased current stresses and conduction losses. On the other hand, switch turn on losses are greatly reduced and soft diode turn off is achieved. Moreover, due to the particular topology we are dealing with, the input current can be continuous also in DCM by a suitable choice of inductors L_1 and L_2 (see Fig.3).
3 - DICM operation combines disadvantages of both CCM and DCM conditions. In fact, the input current ripple increases, so that, beside the increase of stresses and losses, a larger input filter is required, and the diode turn off is still hard. Moreover the high voltage stress at light load limits the practical load range the converter can work with.
4 - DIOCM has the same drawbacks of DICM condition except for the soft switch turn on and the soft diode turn off.

Taking into account the above considerations, it seems reasonable to design the converter in such a way that its operation mode changes according to the sequence CCM-DCM when the voltage conversion ratio decreases from one to zero. Note that, in this way, the DIOCM operation is avoided for any value of M because it can occur only after the DICM operation (in DIOCM current i_1 zeroes first respect of current i_2). When, during the DCM operation, condition (10) is violated, the converter behavior remains the same, since both inductor currents zeroes at the same instant of time.

Converter Specifications

They are:
Peak Input voltage: ..... V_i
Load Resistance: ..... R_L
Switching Frequency: ..... f_S

Switch and Diode Current Stress

As stated above, at maximum output voltage (M=1) the converter operates in CCM. Calling M_1 the value of the voltage conversion ratio in correspondence of which the converter enters the DCM region, the maximum normalized switch and diode current stress results (from (7) and (13)):

$$i_{SN,peak} = \frac{i_{S.peak} \cdot R_L}{V_i} = \begin{cases} \frac{4}{3\sqrt{3}} \frac{1}{\sqrt{k}} \text{if } k < \frac{1}{3} \\ \frac{(1+k)^2}{4k} \text{if } k > \frac{1}{3} \end{cases} \quad (18)$$

in which the relation $k=1-M_1$ was used (see (9)).

Fig.7 reports the variation of the normalized current stress as a function of parameter k. This plot can be useful to chose the value of k (and thus of M_1) making a trade off between the maximum allowed current stress, which calls for a high k value, and the inductor size, as it will result from the following analysis (in fact, high k means a wider range of CCM operation).

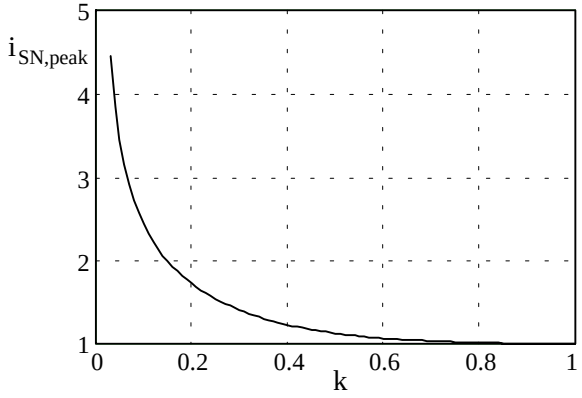

Fig.7 - Normalized switch and diode current stress as a function of parameter k

Switch and Diode Voltage Stress

During both CCM and DCM operation the normalized switch and diode voltage stress is given by:

$$v_{SN,peak} = \frac{v_{S,peak}}{V_i} = 1 + \frac{r_{V1}}{2} \quad (19)$$

while the relative voltage ripple across C_1 can be derived from (5) and (11):

$$r_{V1} = \begin{cases} \frac{1}{f_S R_L C_1} \cdot \frac{16}{25\sqrt{5}} \cdot \sqrt{k} \text{if } k < \frac{1}{5} \\ \frac{1}{f_S R_L C_1} \cdot k \cdot (1-k)^2 \text{ if } \frac{1}{5} < k < \frac{1}{3} \\ \frac{1}{f_S R_L C_1} \cdot \frac{4}{27} \text{if } k > \frac{1}{3} \end{cases} \quad (20)$$

Inductances L_1 and L_2

From (9) the value of parameter k is found as $k=1-M_1$ and from its definition the value of equivalent inductance L_e is obtained as:

$$L_e = \frac{L_1 L_2}{L_1 + L_2} = \frac{R_L}{2f_S} \cdot (1 - M_1) \quad (21)$$

A second constraint on the two inductors is given by inequality (10):

$$\frac{L_1}{L_2} > \frac{1-M_2}{M_2} \qquad (22)$$

where M_2 is the value of the conversion ratio in correspondence of which current i_1 zeroes every switching cycle. This value must be chosen suitably lower than M_1, in order to reduce the input current ripple, thus reducing input filter requirements. From (21) and (22), the values of inductances L_1 and L_2 are derived as follows:

$$L_1 = \frac{R_L}{2f_S} \cdot \left(\frac{1-M_1}{M_2} \right) \qquad (23.a)$$

$$L_2 = \frac{R_L}{2f_S} \cdot \left(\frac{1-M_1}{1-M_2} \right) \qquad (23.b)$$

Note that the value of L_1 obtained from (23.a) automatically satisfies constraint (4) which ensures a transfer from CCM to DCM operation without entering the DICM region.

Capacitance C_1

Using (20), the value of capacitor C_1 is easily found once the desired voltage ripple is given.

Capacitance C_2

The value of this capacitance is also calculated from the desired voltage ripple. Comparing (6) and (12) it is easy to see that the relative voltage ripple is always higher in DCM operation. Thus, we can write:

$$C_2 = \frac{\sqrt{k}}{8\, f_S^2\, L_e\, r_{V2}} \qquad (24)$$

V. Design Example

A prototype was designed and built with the following specifications:

$V_{i,RMS}$ = 220 V; P_L = 1 kW; f_S = 25 kHz.

The converter parameter values are listed in Table I.

Table I - Converter parameters

L_1=400µH	L_2=160µH
C_1=2µF	C_2=1µF
S=IRFP450	D=RURG80100
R_L=48Ω	

With this choice of parameter values, it results:

M_1=0.881	M_2=0.286
r_{v1}=3.8%	r_{v2}=54.8%
$i_{s,peak}$=13.8A	$v_{s,peak}$=316V

The regulation characteristic is shown in Fig.8. The passage between CCM and DCM regions is clearly visible.

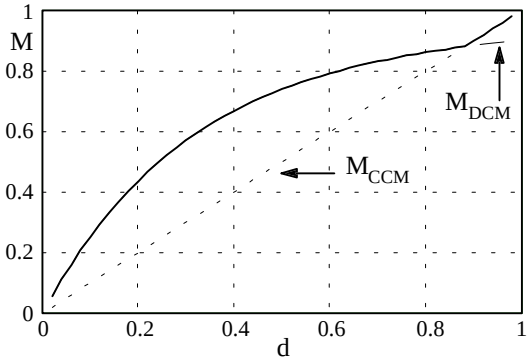

Fig.8 - Regulation characteristic

VI. Experimental Results

Measurements were taken on the prototype in order to verify the theoretical forecasts. The only modification respect to the topology shown in Fig.1 is the presence of a fast diode placed in series with L_1 to avoid problems with the slow bridge diodes when the input current becomes discontinuous. All measurements were taken at d=96%.

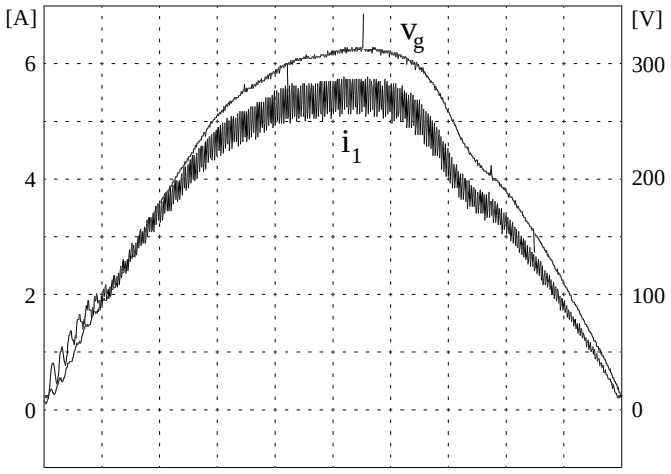

Fig.9 - Rectified input current and voltage (1ms/div)
(Measurement conditions: d=96%, V_i=310V, R_L=48Ω)

The input voltage and current waveforms during half line cycle are shown in Fig.9. As we can see, the input current replicates the line voltage with a small high-frequency ripple. This latter, however, increases at lower values of the conversion ratio.

In Fig.10 the input current spectrum is shown: total harmonic distortion is 5.8%. Note, however, that also the line voltage is distorted with THD=2.8%. The measured power factor was 0.998.

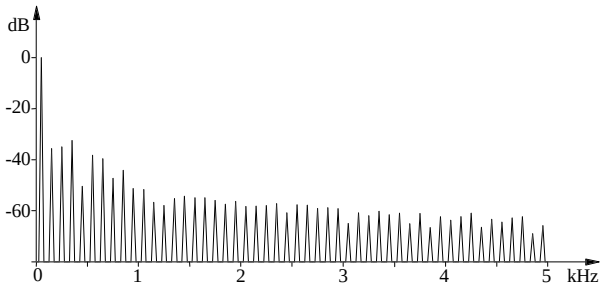

Fig.10 - Line current spectrum

The switch current and voltage waveforms during some switching periods are shown in Fig.11. Observe that, due to the CCM operation, the switch current has a large spike caused by the reverse recovery time of the freewheeling diode D. On the other hand, the switch voltage stress is equal to the peak of the line voltage.

The measured efficiency at rated power was 95%.

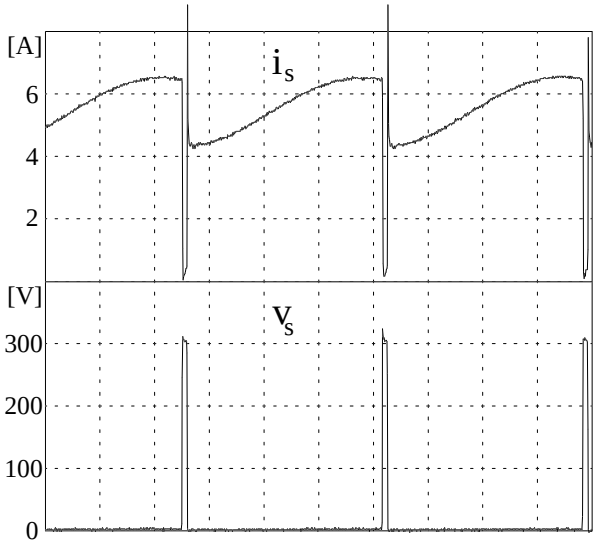

Fig.11 - High frequency switch current and voltage waveforms (10μs/div)

VII. Conclusions

A high-quality rectifier for supplying resistive loads, featuring step-down regulation, high power factor, low input current distortion and high efficiency is presented. It has continuous input current and same device stresses of the buck converter.

Detailed converter design criteria have been given which fully exploit the topology potentialities.

Experimental tests done on a 1kW prototype demonstrate that, in spite of its simplicity, the converter is able to provide excellent operating characteristics for the given application.

References

[1] J. L. White, W. J. Muldoon, "Two-Inductor Boost and Buck Converters," IEEE Power Electronics Specialists' Conf. Rec., 1987, pp. 387-392.

[2] Z. Zhang, S. Cuk, "A High Efficiency 1.8 kW Battery Equalizer," IEEE Applied Power Electronic Conf. Proc., 1993, pp. 221-227.