Design Considerations on Current-Mode and Voltage-Mode Control Methods for Half-Bridge Converters

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***Abstract*. The instability of the input capacitors midpoint voltage in the half-bridge topology observed using peak current-mode control is investigated and a simple solution, which does not require any modification of the converter power stage, is proposed.**

As far as voltage-mode control is concerned, a novel multi-loop control allows to synthesize the desired regulator transfer function by using only low-pass filters, thus reducing the high-frequency noise coupling typical of standard PID regulators and reducing the dependency of crossover frequency and phase margin on output capacitor ESR.

In the paper, useful design considerations are given and verified with an experimental prototype.

I. INTRODUCTION

Compared to other dc-dc converter topologies, the half-bridge one offers several advantages, i.e. minimum device voltage ratings, good exploitation of the transformer core, and recover of the leakage inductor energy to the input voltage. For these reasons it is particularly suitable for off-line applications in which the converter input voltage exceeds the line voltage peak value.

As far as the control method is concerned, the use of standard peak current-mode control is precluded by low-frequency stability problems which show themselves through a drift of the input capacitors midpoint voltage. Thus, voltage-mode control is generally used which must cope with the two-poles transfer function of the converter. In this case, for continuous conduction mode (CCM) of operation, a standard PID controller is adopted in order to achieve reasonable control loop bandwidth, with the drawback of an increase of high-frequency noise coupled with the control circuitry and, above all, with the strong dependency of the crossover frequency on output capacitor ESR.

In the paper a solution for this problem is presented, which exploits the multi-loop control concept to implement a voltage mode controller by using only low-pass transfer functions, without sacrificing the control loop bandwidth. Comparison with the standard approach is also given in terms of converter audiosusceptibility (input to output voltage transfer function) and output impedance.

However, peak current-mode control is more attractive due to the following advantages: inherent switch current limitation, higher loop bandwidth achievable respect to voltage mode control, lower audiosusceptibility.

Unfortunately, due to the above mentioned instability problem, some provisions must be taken. For example, a modification of the converter power stage consisting of a low-power auxiliary winding in the transformer plus two diodes, was proposed in [1].

In this paper, a different approach is presented which provides stability by acting only on the converter control. It requires only few inexpensive components besides a standard current-mode control IC. In the paper, stability of this control loop is investigated and provisions for the control stability are given.

Both the proposed control methods are implemented and tested by using an experimental prototype, and their performances are fully investigated.

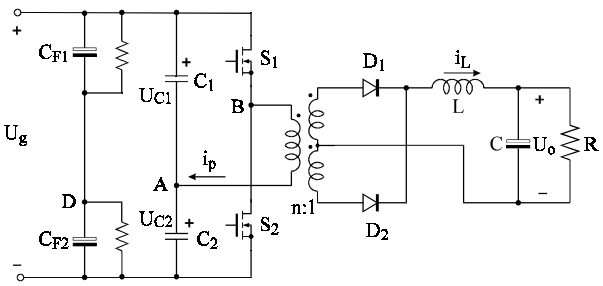

Fig.1 - Basic Half-Bridge converter topology

II. PEAK CURRENT-MODE CONTROL: STABILITY ANALYSIS

The circuit of Fig.1 shows the basic half-bridge topology. Since the experimental prototype was intended to be used in off-line applications, two input capacitors (C_{F1}, C_{F2}), connected in series, are used to filter out the low frequency component of the input voltage due to the rectification process (simple diode-bridge rectifier or power factor preregulator), while two additional small capacitors (C_1, C_2) are used to create the midpoint voltage U_A of the half bridge. In this way the parasitic inductances of the loops formed by these capacitors with the switches and the transformer primary winding, can be minimized, and also the discharge energy during faults is reduced. In order to keep the midpoint voltage U_A at its steady-state value of $U_g/2$, the control technique must ensure a zero primary average current.

As known, in the peak current-mode control control technique, the transformer primary current i_p (which is proportional to the inductor current during the switch on-time) is sensed, rectified and compared with a constant reference signal to determine the turn-off instant. The switches are then turned on and off alternatively at constant frequency. At steady state, the input capacitors C_1 and C_2 are each charged at one half of the input voltage. If, for any reason, the voltage across one capacitor changes, since the current slope depends on the input capacitor voltages, the corresponding on-time duration changes in the direction which enhances the voltage variation (regenerative process). The result is that one switch on-time reaches its maximum value (duty cycle D=50%) while the other is modulated in order to regulate the output voltage.

Experimental waveforms obtained with a standard peak current-mode control are shown in Fig.2 where the rectified, and filtered, transformer primary current and the drain-to-source voltage of the lower switch are reported. The situation explained above is clearly recognized (note the different current slopes during the switch on-times which are the consequence of the voltage imbalancing of the input capacitors).

We want now to analyze more deeply this instability phenomenon. In order to do that, it is convenient to consider the equivalent circuit obtained from the scheme of Fig.1 by moving all primary quantities to the secondary side. From the stability analysis point of view, the capacitor C_1 and C_2 are equivalent to a single capacitor C_{eq} given by:

$$C_{eq} = n^2\left(C_1 + C_2\right) \tag{1}$$

and the midpoint voltage U_A reported to the secondary side is indicated as:

$$U_a = \frac{U_A}{n} \tag{2}$$

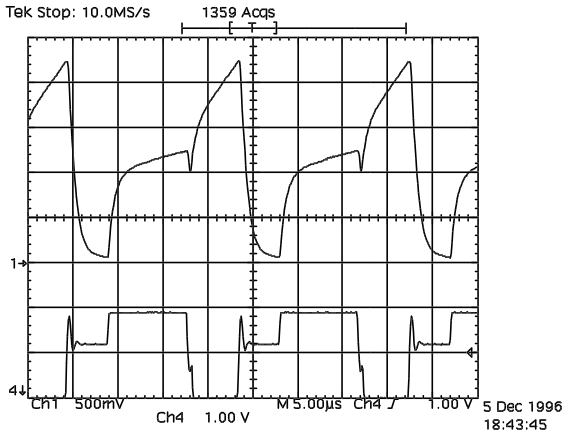

Fig.2 - Experimental results of the instability with peak current-mode control. Upper trace: rectified and filtered primary current [0.735 A/div]; Lower trace: U_{DS} of one switch [200 V/div]

At steady-state (with the assumption of perfect symmetry of both halves of the bridge) the average current flowing into C_{eq} is zero and the inductor current waveform is shown in Fig.3 (solid line). For completeness, the compensation ramp, using to avoid instability at duty-cycle greater than 50%, is also shown.

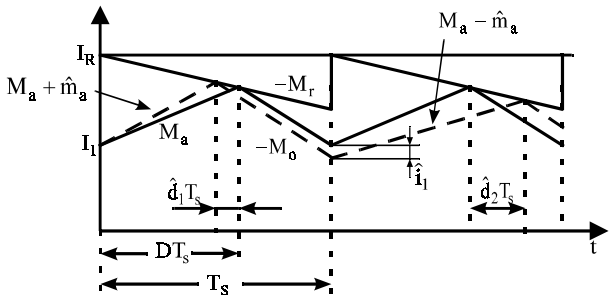

Fig.3 - Inductor current waveform at steady- state (solid line) and during a variation of midpoint voltage U_A

We want now to investigate the effect of a perturbation $\hat{u}_a$ in the midpoint voltage on the average current flowing into the equivalent capacitor C_{eq}, using an approach similar to that presented in [2]. In the following analysis, the small-signal approximation is used so that terms obtained from products of perturbed quantities are neglected.

A perturbation in the midpoint voltage causes an increase of the positive inductor current slope $\hat{m}_a$ in one switching period and a decrease $-\hat{m}_a$ during the next switching period, so that the situation is as described in Fig.3. At steady-state the following equation holds:

$$I_R = I_1 + \left(M_a + M_r\right)D\,T_S = I_1 + M_1 D\,T_S \tag{3}$$

where $M_1=M_a+M_r$. The variation $\hat{m}_a$ is related to the midpoint voltage variation $\hat{u}_a$ by the following equation:

$$M_a = \frac{U_a - U_o}{L} \quad \Rightarrow \quad \hat{m}_a = \frac{\hat{u}_a}{L} \tag{4}$$

This positive current slope variation causes a reduction $\hat{d}_1$ of the duty-cycle in the first switching interval which must satisfy the following equation:

$$I_R = I_1 + \left(M_1 + \hat{m}_a\right)\left(D - \hat{d}_1\right)T_S \tag{5}$$

Using (3) we can calculate:

$$\hat{d}_1 = \frac{D}{M_1}\hat{m}_a \tag{6}$$

At the end of the first switching period the valley inductor current value is changed by the quantity $\hat{i}_1$ given by:

$$\hat{i}_1 = M_o\hat{d}_1T_S - M_r\hat{d}_1T_S = \frac{M_o - M_r}{M_1}DT_S\,\hat{m}_a \tag{7}$$

in which (6) has been used. Thus, during the second switching period, a positive duty-cycle variation $\hat{d}_2$ occurs which can be derived in the same manner as $\hat{d}_1$:

$$I_R = I_1 - \hat{i}_1 + \left(M_1 - \hat{m}_a\right)\left(D + \hat{d}_2\right)T_S \tag{8}$$

$$\hat{d}_2 = \frac{M_a + M_o}{M_1^{\,2}}D\,\hat{m}_a \tag{9}$$

We are now able to calculate the mean current flowing into C_{eq} by taking the average of the inductor current, with the proper sign, during the two switching intervals:

$$\hat{i}_{Ceq} = \frac{1}{2T_S}\int_0^{2T_S} i_{Ceq}(\tau)\,d\tau = \frac{1}{2T_S}\left\{-\frac{D-\hat{d}_1}{2}\left[2I_1 + \left(M_a + \hat{m}_a\right)\left(D-\hat{d}_1\right)T_S\right] + \right.$$
$$\left. + \frac{D+\hat{d}_2}{2}\left[2\left(I_1 - \hat{i}_1\right) + \left(M_a - \hat{m}_a\right)\left(D+\hat{d}_2\right)T_S\right]\right\} \tag{10}$$

Eq.10 assumes a positive value for a positive $\hat{u}_a$ thus demonstrating the regenerative process which is responsible for the instability.

III. Peak Current-Mode Control: Proposed Solution

In order to keep the capacitor midpoint voltage U_A constant, we have to compensate for the inductor current slope variations which occur when U_A moves away from its steady-state value. Thus, a possible solution is to add to the reference current I_R a square wave compensating signal ΔI_R, whose amplitude is proportional to the voltage imbalance. Fig.4 shows an example of such corrective action in which it is possible to recognize the effects of signal ΔI_R in changing the duty-cycle and, as a conseguence, the sign of $\hat{i}_{Ceq}$ so as to reduce the voltage imbalance. In the hypotesis to maintain the duty-cycle D irrespective of the voltage variation $\hat{u}_a$, from Fig.4, the amplitude value of the correcting signal is derived as follows:

$$\Delta I_R = \left(M_a + \hat{m}_a\right)DT_s - \left(M_a\right)DT_s = \hat{m}_aDT_s = \hat{u}_a\frac{DT_s}{L} \tag{11}$$

In our case, since the controller is referred to the secondary side, we used the rectified secondary voltage to derive information on midpoint voltage deviation $\hat{u}_a$. In fact perturbation on U_A causes an oscillation on the secondary rectified voltage amplitude at half the switching frequency. This oscillation can be detected by a sample & hold followed by a high-pass filter, thus obtaining a square signal whose amplitude is equal to the midpoint voltage perturbation. Summing this signal to the input of the voltage regulator, which has a proportional behavior at the switching frequency, we obtain the desired corrected reference signal $I_R+\Delta I_R$ without need of any synchronization. The basic scheme of the adopted controller is shown in Fig.5.

Note that the negative secondary voltage is sampled in order to compensate for phase inversion of the regulator. One possible simple realization of the sample & hold is shown in Fig.6. Transistor Q is needed to discharge the storage capacitor C_s when the sampled voltage is lower than the capacitor one, and resistor R_s filters out voltage spikes.

Experimental results, taken at 50% of the nominal power, are shown in Fig.7. The upper trace represents the rectified and filtered transformer primary current, and the lower waveform is the voltage U_{DS2} across the lower switch: both waveforms show symmetrical behaviors.

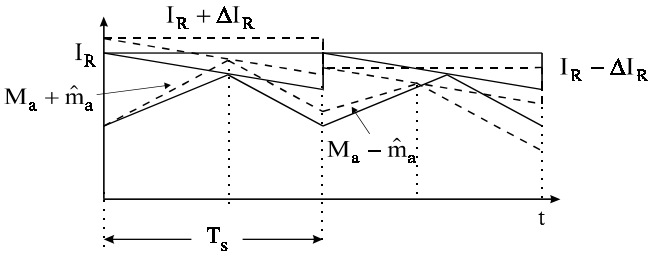

Fig. 4 - Compensated inductor current waveform during a variation of midpoint voltage U_A

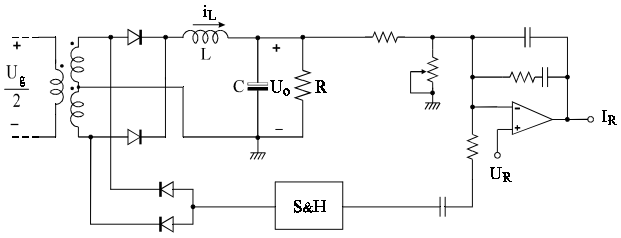

Fig.5 - Implementation of the stabilization circuit of midpoint voltage U_A

IV. Voltage-Mode Control

When high dynamic performances are not required, the voltage-mode control can be profitably used. It represents the simplest control technique and, in theory, it provides better noise immunity than the peak current mode control.

However, due to the converter second order transfer function, a PID controller is generally used in order to obtain a

reasonable loop bandwidth. As a consequence, the derivative action affects its intrinsic noise immunity. Moreover, there is a strong dependency of the crossover frequency and phase margin on the ESR of the output capacitor. To give an idea of such dependency, a PID controller was designed for a converter whose parameters are reported in Table I. The chosen transfer function is:

$$G_{ru}(s)=\frac{\hat{u}_c}{\hat{u}_o}=\frac{\omega_{ru}}{s}\cdot\frac{(1+s\tau_{z1})(1+s\tau_{z2})}{(1+s\tau_{p1})(1+s\tau_{p2})} \tag{12}$$

and its parameters are reported in Table II. The components were selected in order to obtain a closed-loop crossover frequency of about 22kHz with a phase margin greater than 100°. But with an ESR equal to one half of the nominal value, the crossover frequency reduces to 7.5kHz, and the phase margin reduces to about 90°

It is possible to overcome this problem by using the multi-loop control shown in Fig.8a. As we can see, besides the main path between the output voltage and the PWM modulator which provides zero DC error, there is an auxiliary path which takes the AC component of the freewheeling diode voltage and is designed so as to dominate the high frequency part of the loop gain T. In this way, the second order transfer function of the converter output stage is bypassed at high frequency by a first order one, ensuring suitable phase margin. This gives the following advantages: first, allows selection of a proper loop bandwidth using only low-pass filters, thus maintaining excellent noise immunity, second, the loop crossover frequency and phase margin are no more dependent on the ESR of the output filter capacitor.

The corresponding small-signal equivalent model is reported in Fig.8b and the shown transfer functions are listed below:

$$G_p(s)=\frac{1+\frac{s}{\omega_{z3}}}{1+\frac{s}{Q_p\omega_{rp}}+\frac{s^2}{\omega_{rp}^2}},\quad \omega_{z3}=\frac{1}{R_{ESR}C},\quad \omega_{rp}=\frac{1}{\sqrt{LC}}$$

$$Q_p=\frac{1}{\frac{1}{R}\sqrt{\frac{L}{C}}+R_{ESR}\sqrt{\frac{C}{L}}} \tag{13}$$

$$Y_1(s)=\frac{k_1}{1+\frac{s}{\omega_{p3}}},\quad k_1=\frac{1}{R_1+R_2},\quad \omega_{p3}=\frac{R_1+R_2}{C_1R_1R_2} \tag{14}$$

$$Y_2(s)=\frac{sk_2}{1+a_1s+a_2s^2}=\frac{sk_2}{\left(1+\frac{s}{\omega_{p1}}\right)\left(1+\frac{s}{\omega_{p2}}\right)}$$

$$k_2=C_5,\quad a_1=C_5(R_5+R_6)+C_6R_6,\quad a_2=C_5R_5C_6R_6 \tag{15}$$

$$Z_F(s)=\frac{k}{s}\cdot\frac{1+\frac{s}{\omega_{z1}}}{1+\frac{s}{\omega_{p4}}},\quad k=\frac{1}{C_3+C_4}$$

$$\omega_{z1}=\frac{1}{R_4C_3},\quad \omega_{p4}=\frac{C_3+C_4}{R_4C_3C_4} \tag{16}$$

The transfer function parameters are reported in Table III.

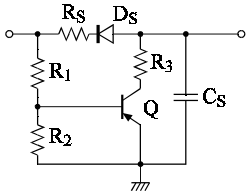

Fig.6 - Sample & Hold implementation

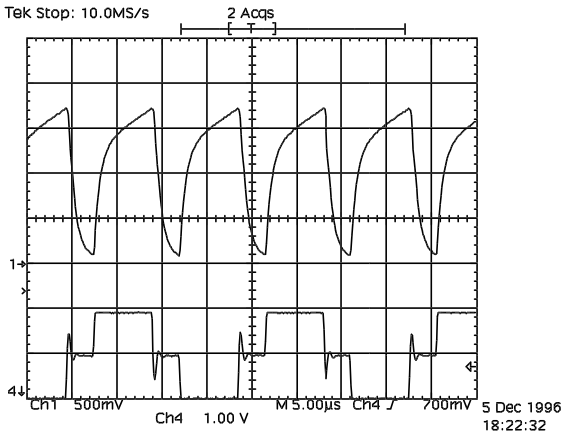

Fig.7 - Experimental results with the proposed control strategy. Top trace: rectifier primary current [0.735 A/div]; bottom trace: lower switch voltage U_{DS2} [200 V/div]

TABLE I - CONVERTER SPECIFICATIONS AND PARAMETERS

U_g = 380V	U_o = 24V	I_o = 25A	f_s = 100kHz	n = 5
L = 18µH	$C_{F1,2}$ = 470µF	ESR = 40mΩ	$C_{1,2}$ = 4.7µF	

TABLE II - PID REGULATOR PARAMETERS

f_{z1} = 882Hz	f_{z2} = 5kHz	f_{ru} = 637Hz
f_{p1} = 59Hz	f_{p2} = 60kHz	

TABLE III - TRANSFER FUNCTION PARAMETERS

f_{z1} = 882Hz	f_{z3} = 4.23kHz	f_{rp} = 1.22kHz	
f_{p1} = 368Hz	f_{p2} = 1.89kHz	f_{p3} = 8.84kHz	f_{p4} = 89.1kHz
$k_1 = 2.78\cdot10^{-4}$	$k_2 = 2.7\cdot10^{-8}$	$k = 4.5\cdot10^{7}$	

From the small-signal block diagram of Fig.8b, the loop gain can be derived as follow:

$$T(s) = G_{PWM}(s) \cdot \frac{U_g}{2n} \cdot Z_F\left(Y_1'(s) + Y_2(s)\right) \qquad (17)$$

where

$$Y_1'(s) = G_p(s) \cdot Y_1(s) \qquad (18)$$

and $G_p(s)$ is the transfer function of the converter output filter.

The asymptotic diagrams of the magnitude of $Y'_1(j\omega)$, $Y_2(j\omega)$ and $T(j\omega)$ are reported in Fig.9: as we can see below f_{z2} the first path (Y'_1) dominates ensuring zero DC error at steady-state, while above f_{z2} the auxiliary path with its -20dB/decade roll-off ensures sufficient phase margin. Note that G_{PWM} was considered constant.

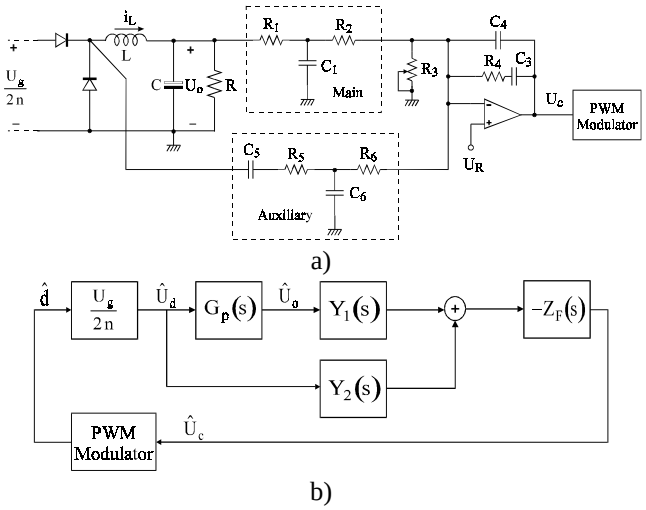

Fig.8- Multi-loop voltage-mode control; a) control scheme, b) small-signal equivalent model

The selected crossover frequency f_c is about 21kHz while the phase margin is 62°. If the ESR of the output capacitor is halved, the crossover frequency reduces to 19.7kHz while the phase margin actually increases to 70°, thus ensuring a converter dynamic practically independent of the output filter parameters.

The actual magnitude of $Y'_1(j\omega)$, $Y_2(j\omega)$ are reported in Fig.10: the crossing frequency f_{z2} is 5.45kHz.

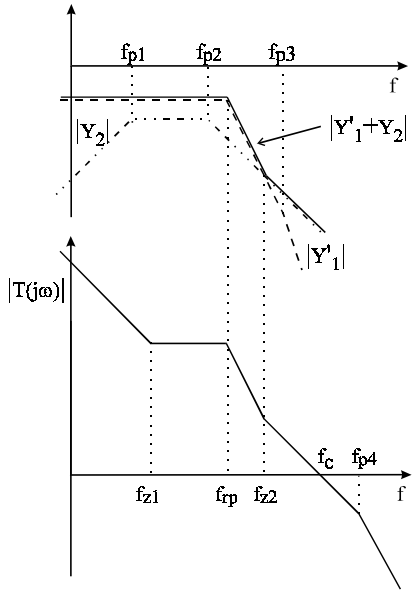

Fig.9 - Bode plot of $Y'_1(j\omega)$, $Y_2(j\omega)$ and of loop gain $T(j\omega)$

V. Comparison of Standard PID and Multi-Loop Voltage-Mode Control Techniques

A. Loop Gain Comparison

Fig.11 shows the Bode plots of magnitude and phase of the loop gain $T(j\omega)$ of both standard (curve a) and multi-loop (curve b) control techniques: note the strong leading effect of the ESR on the loop gain of the standard PID controller. Instead, the greater gain of the multi-loop control ensures faster and more precise behaviour of the converter dynamics.

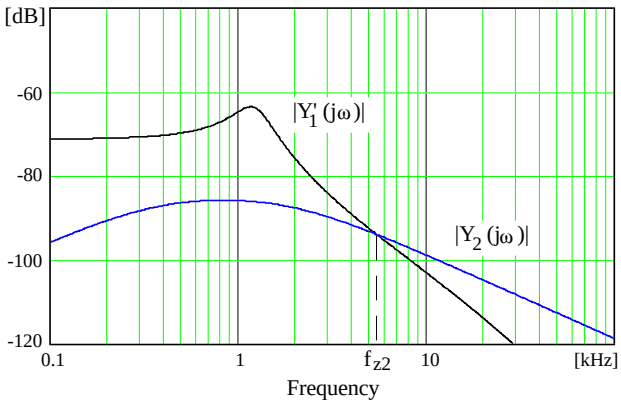

Fig.10 - Actual magnitude of $Y'_1(j\omega)$, $Y_2(j\omega)$

B. Audiosusceptibility Comparison

The converter audiosusceptibility for both control techniques is shown in Fig.12, together with its open-loop behavior. As we can see, the multi-loop approach, which allows a selection of a higher low-frequency loop gain without

penalizing the phase margin, gives a better supply voltage rejection from dc up to 10kHz.

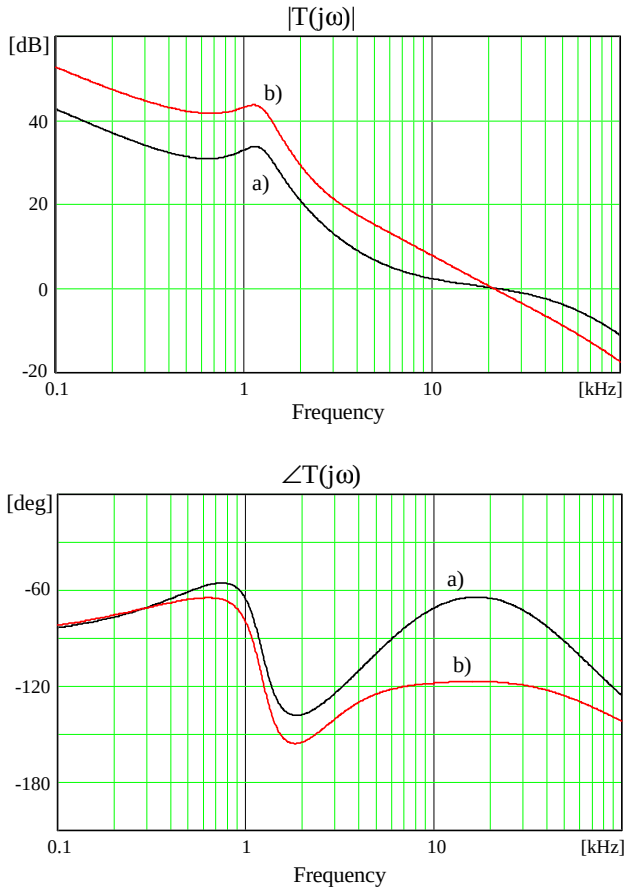

Fig.11 - Magnitude and phase plots of loop gain T(jω); a) with PID controller; b) with multi-loop control

C. Output Impedance Comparison

The comparison between the converter output impedance of both control techniques is reported in Fig.13. In this case, the proposed control techniques shows a worse behavior respect to the standard approach, because, at high frequencies, the output filter is no more included in the control loop so that its output impedance cannot be reduced by the feedback. Note, however, that the maximum output impedance is still dominated, at high frequency, by the output capacitor ESR.

V. Experimental Results

In this section, we report some experimental results taken on a prototype whose parameters are reported in Table I. All the converter control is referred to the secondary side while the transformer primary current is sensed with a current transformer.

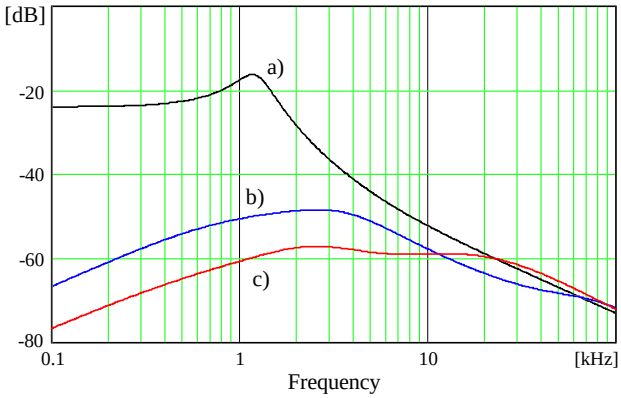

Fig.12 - Audiosusceptibility; a) open loop; b) with PID controller; c) with multi-loop control

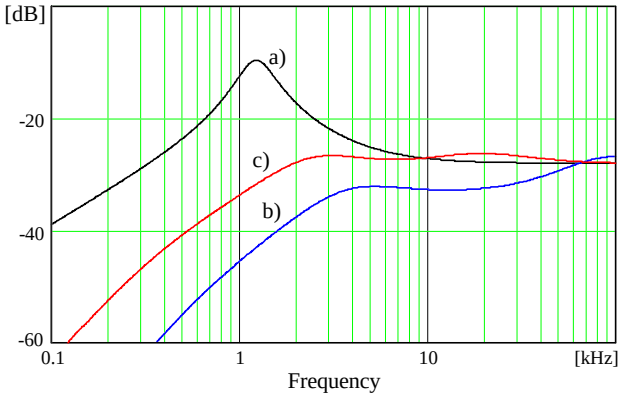

Fig.13 - Output impedance; a) open loop; b) with PID controller; c) with multi-loop control

The following figures refer to the converter with the multi-loop control shown in Fig.8. Before to illustrate the obtained results, it is worthy to do some consideration on the stability of the midpoint voltage U_A. In fact the voltage control itself does not correct for any midpoint voltage imbalance because it keeps, in any case, a constant duty-cycle. For this reason, at high load current, we found a low frequency oscillation (470Hz) on the midpoint voltage U_A. The oscillation frequency value is close to the resonant frequency given by C_1, C_2 and the transformer magnetizing inductance. This problem can be solved introducing a compensation of the voltage imbalance as shown in Fig.5 for the case of the peak current-mode control. More simply, and this is the provision we took, this resonant oscillation can be dumped by using a 100Ω resistor connected between points A and D of Fig.1. During normal operation the voltage across these two points is equal to the high-frequency voltage ripple of voltage U_A. As a consequence, the power dissipated by this resistor is very small.

We can now discuss the converter performances. Fig.14 reports: drain-to-source voltage U_{DS1}, regulator output voltage U_c, and rectified primary current $|i_p|$. All the waveforms are taken under nominal conditions (I_o = 25A). As

we can see the behavior is regular with some high-frequency ripple on U_c due to the regulator high bandwidth.

The dynamic behavior of the converter is illustrated by Fig.15 which reports output voltage U_o, control voltage U_c and load current variation ΔI_o for a load step change from 2 to 22A and viceversa: as we can see the converter response is quite fast, especially during the positive load transition. In order to better appreciate the converter performances in this situation, the time scale, during the positive load transition, is enhanced in Fig.16: note that the sharp decrease of the output voltage to the load connection is mainly due to the output capacitor ESR (about 40mΩ) and thus it is unavoidable. After that the converter returns at the steady-state value in less then 200µs.

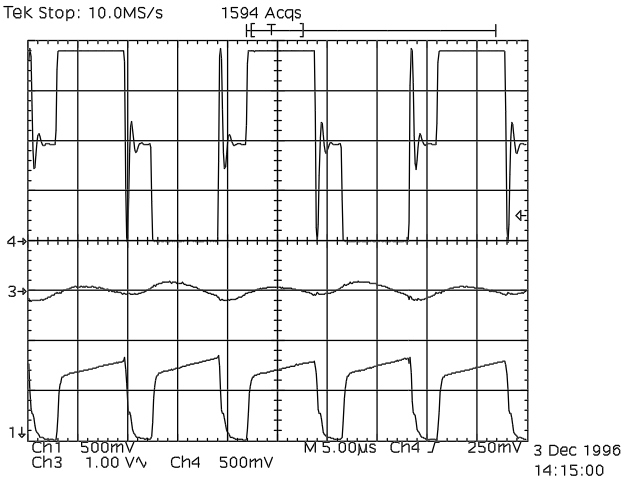

Fig.14 - Main converter waveforms at nominal conditions. Upper trace: U_{DS2} [100V/div]; middle trace: U_c [1V/div]; lower trace: i_p [3.33A/div]

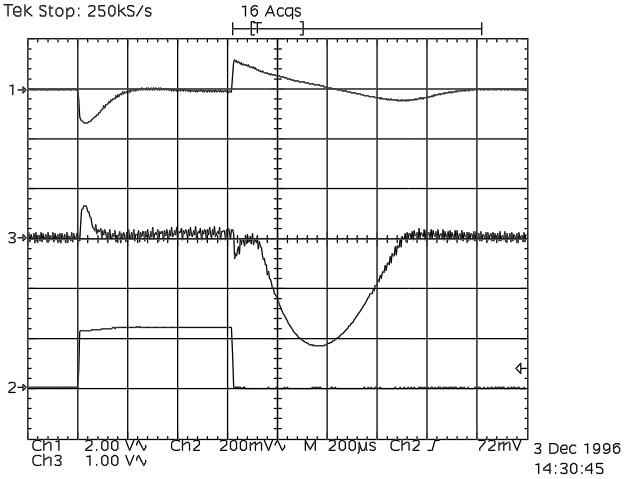

Fig.15 - Waveforms for a load step variation from 2 to 22A and viceversa. Upper trace: U_o [2V/div]; middle trace: U_c [1V/div]; lower trace: ΔI_o [18 A/div]

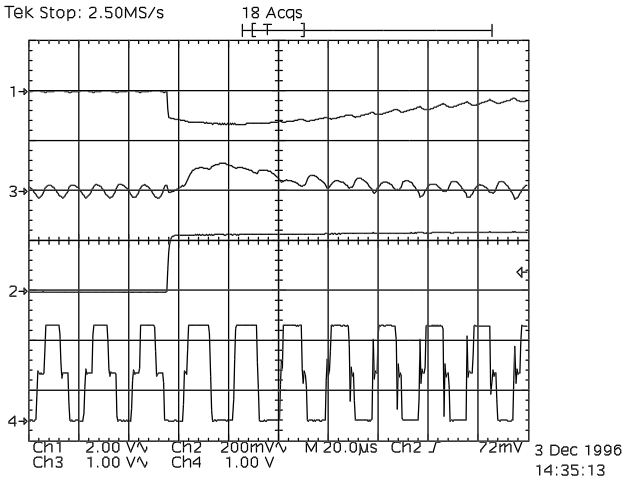

Fig.16 - Particular of the load step variation from 2 to 22A From top to bottom. First trace: U_o [2V/div]; second trace: $U_{control}$ [1V/div]; third trace: ΔI_o [18 A/div]; fourth trace: U_{DS2} [200 V/div]

VI. CONCLUSIONS

Current-mode and voltage-mode control techniques are investigated for application to half-bridge converters. A solution for the instability problem of the peak-current controlled half-bridge converters is presented which ensures the control of the input capacitors midpoint voltage without need of any modification of the converter power stage.

A multi-loop control scheme concept was exploited in order to design a high-bandwidth voltage-mode control in which the desired transfer function is implemented by using only low-pass filters, thus reducing the high-frequency noise coupling typical of standard PID controllers, and which gives a reduced dependency of crossover frequency and phase margin on output capacitor ESR.

Experimental results taken on a 600W prototype confirmed the theoretical expectations.

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