Analysis of Buck Converters Used as Power Factor Preregulators

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Abstract. **Buck-type converters are analyzed for application as power factor preregulators. In particular, the maximum power for which the IEC 1000-3-2 standards are met is calculated for different conversion ratios and modulation techniques.**

Two step-down converters are proposed, which comply with EMC standards thanks to an auxiliary flyback stage which uses the same switches of the main converter plus a small power switch commutated at the line frequency. With proper design, the voltage stress of the main switch remains the same as for a conventional buck topology.

Simulations and experimental results are reported to validate the theoretical analysis.

I. INTRODUCTION

In ac-to-dc conversion, equipment having a rated current less than 16A/phase must comply with IEC 1000-3-2 standard which limits the harmonic content of the current absorbed from the mains [1]. For this purpose, many converter topologies have been analyzed in the literature for use as power factor preregulators, i.e. to provide an almost sinusoidal current absorption and regulated dc output voltage [2-5]. Among them, the most popular is certainly the boost preregulator, which provides the following advantages: simplicity, inherent input current filtering due to the input inductance, almost unity power factor when working in CCM with average current mode control [5]. Still, it has some drawbacks, namely, no limitation of the inrush current at start-up, lack of short-circuit protection and output voltage greater than peak input voltage (V_o = 380-400V for universal input voltage range).

These limitations can be overcome by using a buck-type preregulator which, however, shows a pulsed input current and some line current distortion, due to the notches around zero crossing of the line voltage. Nevertheless, since IEC 1000-3-2 standards allow a certain amount of line current distortion [1,6], usually a power range exists in which the buck-type preregulator meets the standards.

This power range is calculated, in the first part of the paper, for different voltage conversion ratios and modulation strategies. In the second part, two step-down topologies are proposed which include a main buck converter and an auxiliary flyback stage. This latter is used to absorb current even during the time intervals in which the main buck converter is inactive. In this way, the input current distortion is reduced, thus increasing the useful power range.

Differently from the scheme proposed in [7], the flyback stage uses the same switches of the main converter for the modulation and requires only additional line-frequency-commutated switches. Moreover, this auxiliary converter is rated for a fraction of the total power.

Lastly, simulation and experimental results are reported which confirm the theoretical expectations.

II. THE BUCK-TYPE PREREGULATOR

The basic scheme of a buck converter used as a preregulator is shown in Fig. 1. It consists of a diode bridge rectifier followed by a standard buck converter.

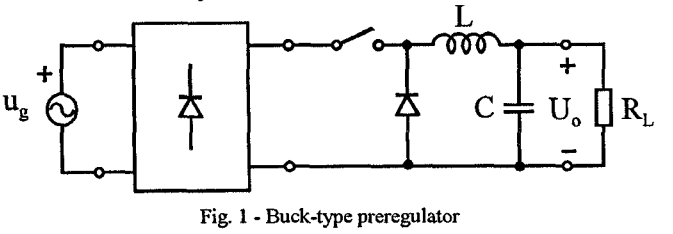

Fig. 1 - Buck-type preregulator

As in boost-type preregulators, the output capacitor filters out the low-frequency components of the input power. However, unlike the boost converter, the converter shown in Fig. 1 is able to draw current from the line only when the input voltage is greater than the output voltage. As a

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consequence, notches appear in the line current around zero crossing of the line voltage, causing distortion.

Fig. 2 shows a typical filtered line current waveform of the converter whose parameter values are specified in table I. This waveform is obtained by using a sinusoidal input current reference, which gives the lowest possible current distortion.

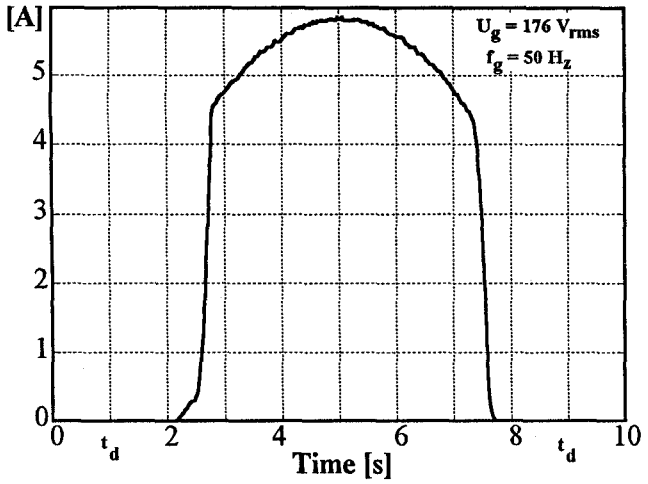


Fig. 2 - Filtered line current waveform of the buck preregulator for sinusoidal-current reference

As we can see, the input current remains zero until the input voltage becomes greater than the output one. Clearly, the dead angle $\theta_d = \omega t_d$ at the beginning and at the end of the line half-period is a function of the voltage conversion ratio M, i.e.:

$$\theta_d = \sin^{-1}(M), \quad M = \frac{U_o}{\hat{U}_g} \tag{1}$$

where $\hat{U}_g$ is the line voltage peak. The initial limited slope of the input current is unavoidable since the inductor current can increase with a slope limited by $(U_g-U_o)/L$. Moreover, since at the beginning of the conduction phase the inductor voltage during turn-on is very low (U_g close to U_o), initially the converter works in discontinuous conduction mode (DCM), which further limits the current rise-time.

A comparison between the current spectrum and the limits imposed by IEC 1000-3-2 standard for Class A (Class D equipment limits are the same for a power greater than 600W) shows that this solution, for this particular output power and voltage conversion ratio, does not meet the standards for high-order harmonics. Thus, it becomes interesting to find the maximum power that a buck converter can deliver while satisfying the standards for different voltage conversion ratios.

III. Analysis of the Current Absorbed by a Buck Preregulator: Ideal Waveforms

In the following, we will consider two different modulation strategies, i.e. constant-current reference (also called input-current-clamping) and sinusoidal-current reference. A typical filtered input current waveform for constant-current reference is shown in Fig. 3. The advantages of using constant-current reference are reduced current stresses of the power semiconductors and limited current load around the peak of the line voltage, which could partially compensate for the peak-clipping effect of conventional diode-capacitor rectifiers. On the other hand, a sinusoidal-current reference allows, for the same voltage conversion ratio, a higher input power without exceeding the harmonic limits.

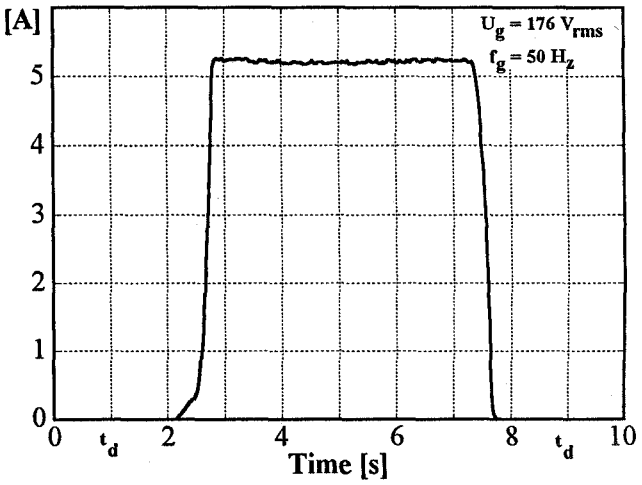


Fig. 3 - Filtered line current waveform of the buck preregulator for constant-current reference

A. Constant-Current Reference

As we can see from Fig. 3, the average input current can be approximated by a three-level square wave, for which the peak harmonic currents are given by:

$$I_{n\_peak} = \frac{4I_{REF}}{n\pi} \cdot \cos(\theta_d) \tag{2}$$

In practice, the input current waveform has an equivalent dead angle greater than θ_d due to the DCM operation when the inductor current starts to flow. The duration of this operation mode depends on input and output voltages and inductance values [6].

From (2) it is possible to find the maximum input power that the buck converter can deliver without exceeding the standards (IEC 1000-3-2 Class A equipment). The results are shown in Fig. 4 as a function of the voltage conversion ratio and for three different input voltage levels. As we can see, with this type of modulation the load power cannot exceed some hundred watts.

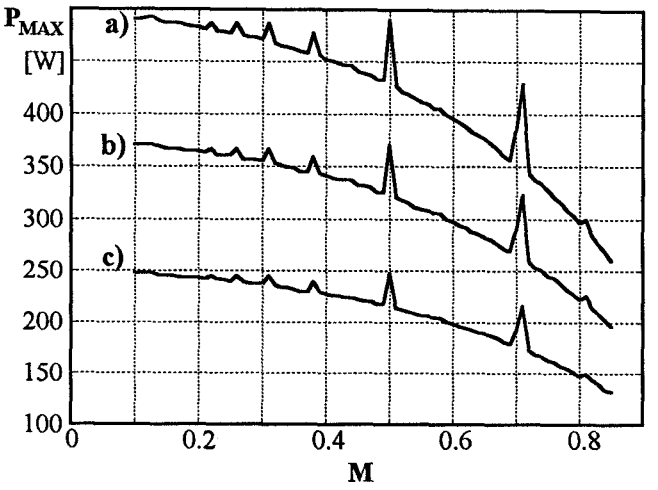


Fig. 4 - Maximum input power as a function of voltage conversion ratio M in case of constant-current reference modulation.
a) $U_g = 220\ V_{RMS}$, b) $U_g = 165\ V_{RMS}$, c) $U_g = 110\ V_{RMS}$

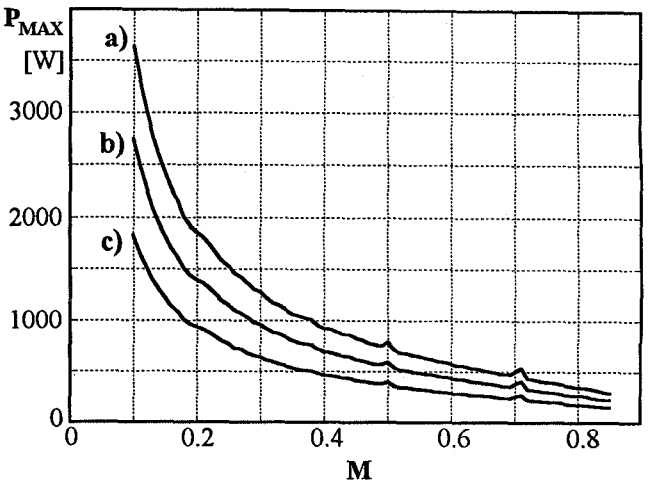


Fig. 5 - Maximum input power as a function of voltage conversion ratio M in case of sinusoidal-current reference modulation.
a) $U_g = 220\ V_{RMS}$, b) $U_g = 165\ V_{RMS}$, c) $U_g = 110\ V_{RMS}$

For higher voltage conversion ratios the dead angle θ_d increases thus increasing the input current harmonic content.

Note the peaks in the curves of Fig. 4 which occur at 50% and 71.5% of duty-cycle revealing some harmonics cancellation at these duty-cycle values. Results obtained with other idealized input current waveforms are given in [6].

The curves end for a duty-cycle equal to 85% in order to remain within the Class A specifications (for higher duty-cycles the input current waveform belongs to Class D).

B. Sinusoidal-Current Reference

Using a sinusoidal-current reference, the maximum input power achievable tends to infinity as M approaches zero, because the average input current becomes a pure sinusoid. Analyzing an ideal truncated sinusoidal waveform (approximation of the real behavior shown in Fig. 2) the input current harmonic content is given by:

$$I_{1\_peak} = \frac{I_{REF}}{\pi} \cdot \left| \pi - 2\theta_d + \sin(2\theta_d) \right| \qquad (3)$$

$$I_{n\_peak} = \frac{2I_{REF}}{\pi} \cdot \left| \frac{\sin[(n+1)\theta_d]}{n+1} - \frac{\sin[(n-1)\theta_d]}{n-1} \right|, \qquad n = 3,5,7\ldots$$

where I_{REF} is the peak of the sinusoidal current reference. The plots of the maximum input power calculated in the same conditions of Fig. 4 are reported in Fig. 5.

Combined sinusoidal- and constant-current reference techniques can be used in order to gain some advantages of both approaches. In this case the maximum power achievable lays between the correspondent curves of Figs. 4 and 5.

IV. Proposed Solution

As we have seen, the dead angle of the input current strongly affects the maximum power delivered by the converter. Thus, by allowing current absorption during the line intervals in which the main buck converter is inactive, the maximum power achievable can be greatly increased. This was the solution proposed in [7] which includes, besides the main buck converter, an auxiliary parallel flyback converter feeding the same load. This auxiliary power stage is activated only in the fraction of the line period in which the main converter is idle and thus can be designed in order to handle a power which is just a small fraction of the total input power. One of the drawbacks of the solution given in [7] is that a complete second power stage is needed, thus increasing the whole cost of the converter.

The aim of this paper is to propose solutions which integrate the buck and the flyback stages, thus reducing the components count. One of these solutions is shown in Fig. 6.

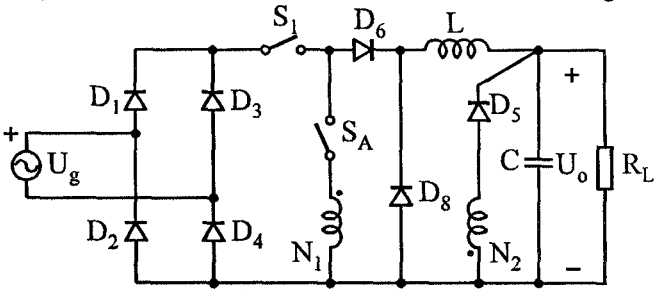


Fig. 6 - Proposed integrated buck+flyback converter

Diode bridge (D_1-D_4), switch S_1 and components D_6, L and C form the main buck power stage, while the remaining components constitute the auxiliary flyback converter. One important difference with respect to the solution proposed in

[7] is that the flyback stage exploits the same switch of the buck converter (S_1) to perform the modulation, while switch S_A is operated at line frequency in order to enable and disable the auxiliary flyback converter.

The converter operation can be subdivided into two parts:

a) $U_g < U_o$. During this fraction of the line period, the current in the filter inductance L remains zero for the presence of diode D_6; switch S_A is kept closed and switch S_1 is modulated so as to absorb the desired line current by operating the auxiliary flyback stage.

b) $U_g > U_o$. In this case, switch S_A is turned off so as to disable the flyback stage, while S_1 is modulated in order to achieve proper operation of the buck converter.

A typical simulated filtered input current waveform is shown in Fig. 7 (in case of sinusoidal-current reference) for the same converter parameters reported in table I. Indeed, in Fig. 7, the flyback operation was enabled for an input voltage slightly greater than the output one so as to partially compensate for the initial DCM operation of the buck stage. As we can see, the sinusoidal reference peak value for the flyback operation was kept intentionally lower ($k \cdot I_{REEF}$, $k < 1$) than that for the buck operation in order to limit the power handled by the flyback stage to the minimum required to satisfy the harmonic limits and, at the same time not to worse the peak current stress of switch S_1.

The analysis performed on an idealized waveform (which approximates the behavior shown in Fig. 7) gives the following harmonic peak values:

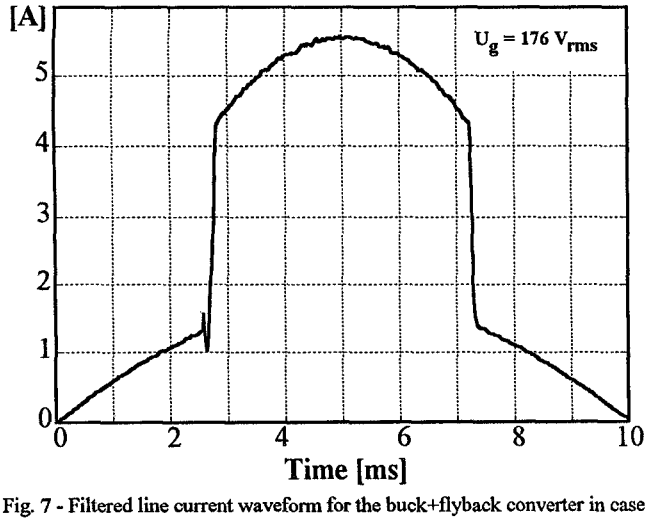


Fig. 7 - Filtered line current waveform for the buck+flyback converter in case of sinusoidal-current reference (k = 0.25)

$$I_{l\_peak} = \frac{I_{REF}}{\pi} \cdot \left| \pi - 2\theta_d(1-k) + (1-k)\sin(2\theta_d) \right| \quad (4)$$

$$I_{n\_peak} = \frac{2I_{REF}(1-k)}{\pi} \cdot \left| \frac{\sin[(n+1)\theta_d]}{n+1} - \frac{\sin[(n-1)\theta_d]}{n-1} \right|$$

$$n = 3,5,7\ldots$$

where k is the ratio between the sinusoidal reference peak value for the flyback operation and the sinusoidal reference peak value I_{REF} for the buck operation. Note that, for k = 1, the ideal absorbed current becomes a pure sinusoid, having a peak value equal to I_{REF}.

The harmonic content of the waveform of Fig. 7 now complies with the standards.

From (3) and (4), the peak of the fundamental component of the input current during flyback operation is given by:

$$I_{l\_fly} = \frac{kI_{REF}}{\pi} \cdot \left| -2\theta_d + \sin(2\theta_d) \right| \quad (5)$$

Thus, the ratio between the power handled by the flyback stage and the total input power is simply given by:

$$\frac{P_{fly}}{P_{tot}} = \frac{I_{l\_fly}}{I_{l\_peak}} \quad (6)$$

A plot of this power ratio as a function of the voltage conversion ratio is reported in Fig. 8 for different values of parameter k. These curves show that, if M is not too high, it is possible to design a converter at whatever power we want while keeping the power rating of the auxiliary stage at a small fraction of the total power.

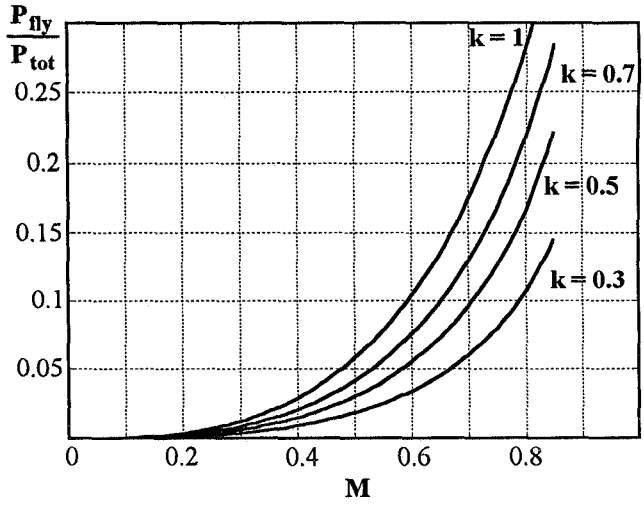


Fig. 8 - Normalized power of flyback stage as a function of output voltage conversion ratio M for different values of parameter k

The curves in Fig. 9 show the maximum power achievable with the converter of Fig. 6. From this plot it is possible to derive, for given input and output voltages, the value of parameter k which ensures input current harmonics complying with the standards. Then, the plots of Fig. 8 allow to find the power rating of the flyback stage components.

It is important to note that similar results can be obtained also for the constant reference current. However, in this case, for the same power, a greater utilization of the flyback stage is needed in order to comply with the standards. Moreover, the maximum power is anyway limited due to the square-wave shape of the absorbed current (see Fig. 4). More information about this modulation technique can be found in [7].

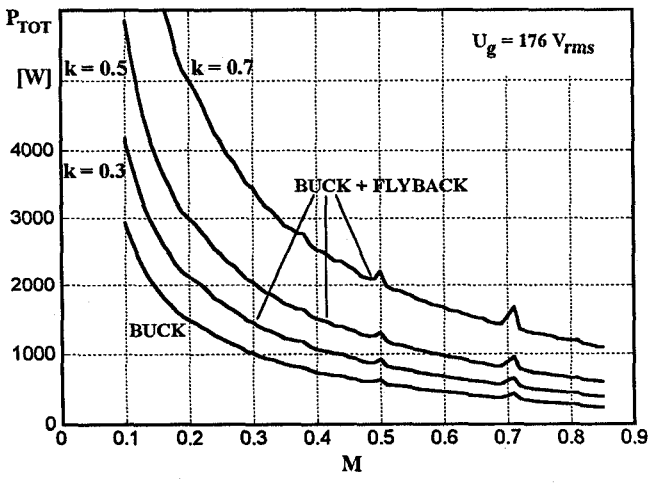


Fig. 9 - Maximum input power as a function of voltage conversion ratio M in case of sinusoidal-current reference

V. Converter Design

The power stage design can start from the simple buck converter and then extended to the complete power stage.

A. Inductor

The average inductor current can be determined by considering the following relations:

$$\bar{i}_g(\theta) = \bar{i}_L(\theta)\, d(\theta) \tag{7}$$

$$\bar{i}_g(\theta) = \begin{cases} \hat{I}_g \left|\sin(\theta)\right| & \text{for } \theta_d + n\pi \le \theta \le (n+1)\pi - \theta_d \\ 0 & \text{for } -\theta_d + n\pi \le \theta \le \theta_d + n\pi \end{cases} \tag{8}$$

$n = 0, 1, 2, \ldots.$

where $\bar{i}_g(\theta)$ is the switch (i.e. input) current averaged over a switching period. From 3) and the power balance we can find:

$$\hat{I}_g = I_{REF} = \frac{2\pi P_o}{\hat{U}_g \left|\pi - 2\theta_d + \sin(2\theta_d)\right|} \tag{9}$$

Considering CCM operation the duty-cycle is given by:

$$d(\theta) = \frac{U_o}{u_g(\theta)} = \frac{M}{\sin(\theta)} \tag{10}$$

Thus, the peak of the average inductor current from (7) and (10) is given by

$$\hat{I}_L = \bar{i}_{Lmax}(\theta) = \bar{i}_L(\theta)\Big|_{\theta=\frac{\pi}{2}} = \frac{\hat{I}_g}{M} \tag{11}$$

while the maximum value of its instantaneous current ripple results:

$$\Delta i_{Lmax} = \Delta i_L\Big|_{\theta=\frac{\pi}{2}} = \frac{U_o}{L f_s}(1-M) \tag{12}$$

The inductor value can than be calculated from the desired maximum current ripple:

$$L = \frac{U_o}{\hat{I}_g}\frac{M}{2 f_s r_i}(1-M) \tag{13}$$

where

$$r_i = \frac{\Delta i_{Lmax}}{2\hat{I}_L} \tag{14}$$

The maximum instantaneous inductor current can be calculated from (12) and (13).

When the operation of the flyback stage is taken into account, equations (10-14) can still be used provided that $\hat{I}_g = I_{REF}$ is calculated from (4) and the power balance.

B. Capacitor

As usual, the output filter capacitor is selected from the constraint regarding the low-frequency output voltage ripple. The latter is derived by integrating the capacitor current over part of a half-line period. The expression for the capacitor current is as follows:

$$\bar{i}_C(\theta) = \bar{i}_L(\theta) - I_o = \ldots$$

$$\ldots \begin{cases} \hat{I}_L \sin^2(\theta) - I_o & \text{for } \theta_d + n\pi \le \theta \le (n+1)\pi - \theta_d \\ -I_o & \text{for } -\theta_d + n\pi \le \theta \le \theta_d + n\pi \end{cases} \tag{15}$$

The peak-to-peak voltage ripple is then given by:

$$\Delta u_o = \frac{1}{2\omega C}\left[(\pi - 2\theta_1)(\hat{I}_L - 2I_o) + \hat{I}_L \sin(2\theta_1)\right] \tag{16}$$

where ω is the line angular frequency and

$$\theta_1 = \sin^{-1}\left(\sqrt{\frac{I_o}{\hat{I}_L}}\right) \tag{17}$$

Capacitor C is then selected from (16).

These equations can still be used also for the complete power stage provided that the power handled by the flyback stage is much lower than the total one.

C. Transformer turns ratio

The selection of the transformer turns ratio is a trade-off between voltage and current switch stresses; in particular, during flyback operation the maximum switch voltage stress is given by:

$$\hat{u}_{s\max}(\theta) = \hat{u}_s(\theta_d) = u_g(\theta_d) + \frac{N_1}{N_2}U_o = \left(1+\frac{N_1}{N_2}\right)U_o \quad (18)$$

while, during buck operation the maximum voltage stress is limited to $\hat{U}_g$. For the converter specifications given in table I it is convenient to choose a unity turns ratio, so that the maximum voltage stress during flyback operation results lower than $\hat{U}_g$. In this way, no increase of the main switch voltage stress occurs.

VI. Experimental Results

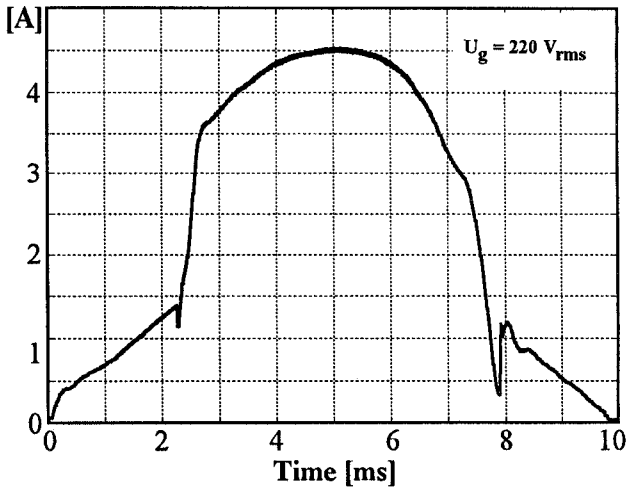
A converter having the specifications and parameters listed in table I was built and tested in order to verify the theoretical expectations.

TABLE I
CONVERTER PARAMETERS

U_g = 176÷264 V_{RMS}	U_o = 160 V	P_o = 600 W
L = 450 μH	C = 2·680 μF	f_s = 50 kHz
L_M = 500 μH	N_1:N_2 = 1	

A charge control was used in order to force a sinusoidal average input current for both buck and flyback operation modes, i.e. the input current is sensed and than integrated cycle by cycle. The main switch S_1 is turned on at constant frequency and turned off when the integral of the switch current reaches a suitable sinusoidal reference (after that the integrator is reset) [8]. To implement such control, a standard PFC controller like the MC34261, which is normally used in boost PFC's designed to operate at the boundary between continuous and discontinuous conduction modes, was employed with some external circuitry.

The filtered input current wafeform during operation of both buck and flyback stages is shown in Fig. 10a together with its spectrum (Fig. 10b): as we can see now this converter complies with the standards. The power handled by the flyback stage is about 7.2% of the total input power.



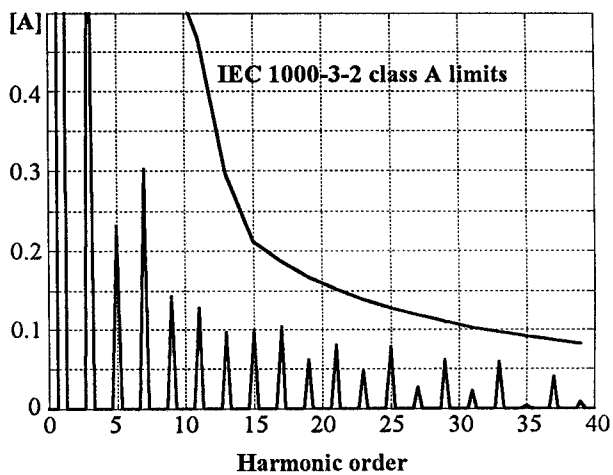


Fig. 10 - a) Filtered line current waveform for buck+flyback operation (nominal power); b) current spectrum and IEC 1000-3-2 limits

VII. Other Converter Topology

In the converter of Fig. 6, the addition of diode D_6 in series with the power path reduces the converter efficiency, even if its effect becomes relevant only for low output voltages. Thus, when high power and low output voltage are needed, the circuit shown in Fig. 11 can be profitably used instead of that previously proposed. The converter operation remains very similar except for the fact that switches S_1-S_A and S_2-S_B operate alternatively each half line period: when U_g is positive, S_1 modulates both flyback and buck stages, depending on the instantaneous input voltage value, while S_A enables and disables the flyback stage (line-frequency commutations); when U_g is negative, the same operations are done by S_2 and S_B respectively. Besides the reduction of the devices number in the power path (i.e. higher efficiency), this solution allows a reduction of the power rating of switches S_1 and S_2 (one half of the total power each).

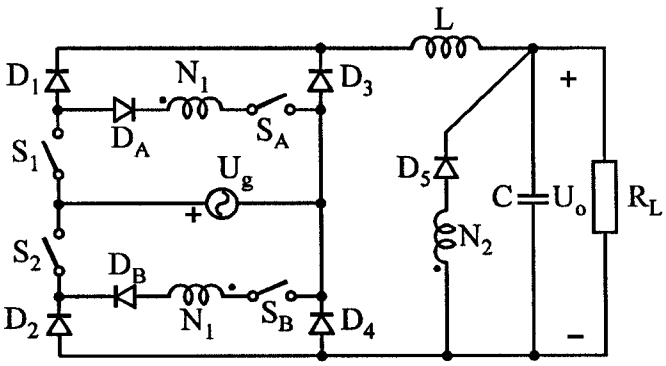


Fig. 11 - Two-switch buck + flyback converter

VIII. Conclusions

The use of buck-type converters as power factor preregulators was investigated. The maximum input power for which the input current harmonics do not exceed the IEC 1000-3-2 limits is calculated for different voltage conversion ratios and for constant- and sinusoidal-current references.

Then a modification of the buck converter which fully complies with the standards was proposed which includes an auxiliary flyback stage. This stage uses the same switch of the main converter, without voltage stress increase, plus a small power switch commutated at the line frequency.

The solution was also extended to a two-switch buck converter.

Simulated and experimental results of a 600W prototype validated the theoretical analysis.

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