Power Factor Preregulator Based on Modified Tapped-Inductor Buck Converter

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Abstract

Power factor preregulators based on buck-type converters with capacitive output filter do not allow a unity power factor due to their inability to draw current from the ac line during those intervals when the input voltage is lower than the output one. This limitation can be overcome by using a modified tapped-inductor buck topology, which can be arranged to operate as a flyback converter when desired. This modification, which requires only an extra line-frequency commutated switch and a diode, allows to extend the input current conduction angle, thus making the converter compliant with harmonic standards like IEC 1000-3-2. A 1kW converter has been designed, built and tested to validate the theoretical forecasts.

1. Introduction

Off-line converters connected to the utility grid, which supply equipment having a rated current lower than 16A/phase, must provide a reduced input current harmonic content, so as to comply with international standards like the IEC 1000-3-2 [1]. High-quality rectifiers based on the boost topology have already been widely analyzed in the literature and are also commonly used in the industry due to their inherent advantages over other topologies, i.e. simplicity, input current filtering due to the input inductance, almost unity power factor when working in CCM (Continuous Conduction Mode) with average current mode control. On the other hand, the lack of any limitation of the inrush current at start-up and of short-circuit protection calls for additional provisions, like a series switch, which increase cost and complexity of the overall rectifier. Moreover, the output voltage is constrained to be higher than the peak input voltage (i.e. U_o = 380-400V for universal input voltage range).

The use of buck-type preregulators allows to overcome the aforementioned drawbacks at the expense of a greater input current distortion, both at line and switching frequency. The low frequency distortion in the line current arises from its unavoidable notches around the zero crossings of the line voltage, caused by the inability of the buck converter to draw current when the instantaneous input voltage is lower than the output one. The high-frequency distortion instead, is caused by the pulsating (at switching frequency) input current. Anyway, the IEC 1000-3-2 standards allow a certain amount of line current distortion and thus permit the use of buck-type preregulators, at least up to a determined power level, which depends on the voltage conversion ratio.

In [2], the utilization of a flyback converter connected in parallel to the main buck preregulator was proposed in order to absorb current from the line even during those intervals when the buck converter is idle. This concept was extended in [3], where the main buck and the auxiliary flyback converter are integrated with the aim of reducing the number of components and consequently the cost.

This paper proposes a similar approach based on a modified tapped-inductor buck converter: with the addition of only a line-frequency commutated switch and a diode, both flyback and buck operation are achieved. In order to provide an almost sinusoidal current absorption, the operating mode is switched from buck to flyback and vice versa twice per period.

The paper initially describes the operation and the design criteria of the proposed converter. Then the experimental tests performed on a 1kW prototype are discussed. The results of the measurements are reported to validate the theoretical analysis and the design procedure.

2. Tapped-Inductor Buck Converter

The tapped-inductor buck converter is simply a buck converter where the free-wheeling diode is connected to a tap in the filter inductor, as shown in Fig. 1a. The behavior of this converter is very similar to that of the standard buck, except for the current waveform in the windings. In fact, during the switch on-time, the current in the two windings N_1 and N_2 is the same and increases with a slope equal to $(U_g-U_o)/L$, while during the switch off-time, the input current zeroes, and current i_2 steps up to maintain the flux continuity

in the core. This behavior is shown in Fig. 1b which reports the voltage and current in the second winding N_2 for the continuous conduction mode of operation (CCM). During the switch turn-off interval, the current i_2 decreases from the initial value $i_2'' = i_2' \cdot (1+1/n)$ with a slope given by $(1+1/n)^2 \cdot (U_o/L)$, where *n* is the turns ratio N_2/N_1. As a consequence, the voltage conversion ratio becomes:

$$M = \frac{U_o}{U_g} = \frac{d}{1 + \frac{1-d}{n}} \qquad (1)$$

where *d* is the duty-cycle. The switch current and voltage stresses become:

$$\hat{i}_S = U_o \left[\frac{1}{R_L} \frac{n+M}{n+1} + \frac{1-M}{2\,L\,f_S} \left(\frac{1+n}{n+M} \right) \right] \qquad (2.a)$$

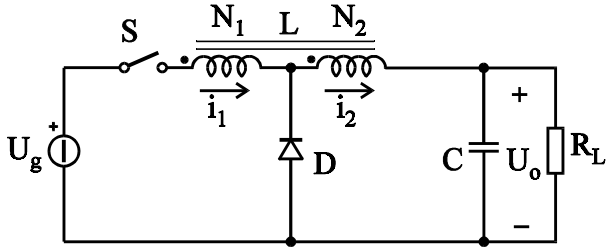
$$\hat{u}_S = U_g + \frac{U_o}{n} \qquad (2.b)$$

The diode current and voltage stresses are proportional to the corresponding switch stresses and are given by:

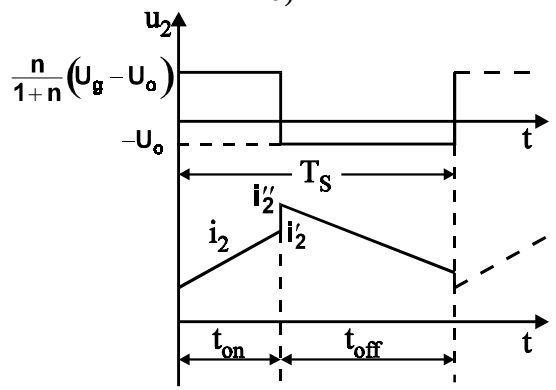
$$\hat{i}_D = \frac{1+n}{n} \hat{i}_S \qquad (3.a)$$

$$\hat{u}_D = \frac{n}{1+n} \hat{u}_S \qquad (3.b)$$

Note that the switch voltage stress is equal to that of a flyback converter with the same turns ratio.



a)



b)

Fig. 1 - a) tapped-inductor Buck converter; b) winding N_2 voltage and current

Actually, with simple modifications, it is possible to operate this converter also as a flyback stage, as it is illustrated in the following section.

The converter can be easily used as a power factor preregulator (PFP) by controlling the average input current so as to make it proportional to the line voltage, which is the best way to obtain a low input current harmonic distortion. As it is well known, this kind of control implies the absorption of a pulsating input power. Similarly to any boost-type PFP, the output capacitor filters out the low-frequency components of the input power. However, unlike the boost converter, the converter shown in Fig. 1 is able to draw current from the line only when the input voltage is greater than the output voltage. As a consequence, notches appear in the line current around the zero crossings of the line voltage, causing an appreciable distortion.

Fig. 2 shows a typical filtered line current waveform: as we can see, the input current remains zero until the input voltage becomes greater than the output one. Clearly, the dead angle $\theta_d = \omega t_d$ at the beginning and at the end of the line half-period is a function of the voltage conversion ratio M, i.e.:

$$\theta_d = \sin^{-1}(M), \quad M = \frac{U_o}{\hat{U}_g} \qquad (4)$$

where $\hat{U}_g$ is the line voltage peak.

The initial reduced slope of the input current is unavoidable since it equals the inductor current whose slope is limited by $(u_g - U_o)/L$. Moreover, since at the beginning of the conduction phase the inductor voltage during turn-on is very low (u_g close to U_o), the converter works initially in discontinuous conduction mode (DCM), which further limits the current rise-time.

The input current harmonic content can be derived for the idealized current waveform

$$\bar{i}_g(\theta) = \begin{cases} \hat{I}_g \left| \sin(\theta) \right| & \text{for } \theta_d + h\pi \le \theta \le (h+1)\pi - \theta_d \\ 0 & \text{for } -\theta_d + h\pi \le \theta \le \theta_d + h\pi \end{cases}$$

h = 0, 1, 2, ... (5)

and is given by

$$I_{1\_peak} = \hat{I}_g \cdot F, \qquad F = \left| 1 - \frac{2\theta_d}{\pi} + \frac{\sin(2\theta_d)}{\pi} \right| \qquad (6.a)$$

$$I_{n\_peak} = \frac{2\hat{I}_g}{\pi} \cdot \left| \frac{\sin[(n+1)\theta_d]}{n+1} - \frac{\sin[(n-1)\theta_d]}{n-1} \right| \qquad (6.b)$$

$n = 3, 5, 7 \ldots$

It is worth noting that, given the similarity between the actual input current waveform shown in Fig. 2, and the idealized one given by (5), the harmonic content estimated by (6) well approximates the actual one. The above harmonic values can be calculated for different voltage conversion ratios and compared to the limits imposed by IEC 1000-3-2 standard, so as to find the maximum power that a PFP based on a buck topology can deliver, while satisfying the limits. Such analysis can be found in [3].

3. Modified Tapped-Inductor Buck Converter

In order to extend the input current conduction angle, it is possible to operate the converter in the flyback mode in the intervals corresponding to $|u_g| < U_o$, and in the buck mode when $|u_g| > U_o$ [3]. This objective can be accomplished simply by adding a line-frequency commutated switch S_A and a diode D_6, as shown in Fig. 3. When S_A is kept closed, the converter becomes a flyback stage in which diode D_6 acts as rectifying diode. Instead, when S_A is open the converter operates in the normal tapped-inductor buck mode. A typical input current obtained with such control strategy is shown in Fig. 4.

Note that a certain amount of current distortion is allowed by the standards. For this reason, there is no interest in obtaining a truly sinusoidal input current. Thus, the sinusoidal current reference signal can be reduced during flyback operation so as to limit the switch current stress, as shown in Fig. 4. In fact, during the flyback mode, winding N_1 takes the input voltage u_g, so that the input current slope S_{fly} during the switch on-time becomes:

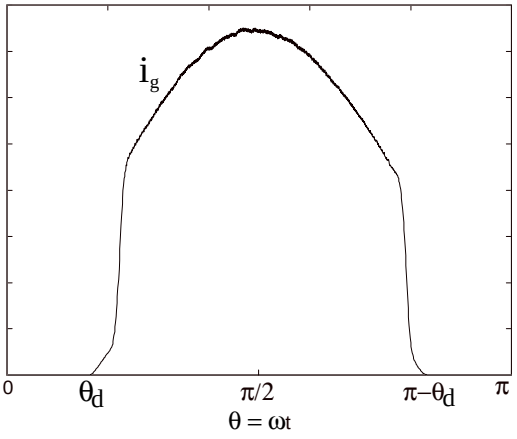


Fig. 2 - Filtered line current waveform of the tapped inductor buck preregulator for sinusoidal current reference

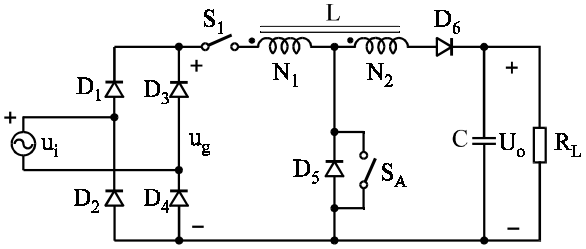


Fig. 3 - Proposed modified tapped-inductor buck preregulator

$$S_{fly}(\theta) = \frac{u_g(\theta)}{L_1} = \frac{u_g(\theta)}{L}(1+n)^2 = \frac{(1+n)^2}{1-\frac{U_o}{u_g(\theta)}} S_{buck}(\theta) \quad (7)$$

where S_{buck} is the input current slope during buck operation. This slope is much higher as compared to that of the buck operation, giving rise to a possible high switch current stress. In the following section, suitable design guidelines are given which ensure compliance with the standards without worsening the switch current stress.

4. Converter Design

The power stage design starts from the tapped-inductor buck converter and is then extended to the complete power stage represented in Fig. 3. In the following, the line over the variable indicates the average of the variable in a switching period.

4.1 Inductor

The inductor value L and turns ratio *n* can be calculated from the switch current and voltage stresses. To this purpose, we must take into account the converter operation as PFP, considering the non-ideality given by the dead

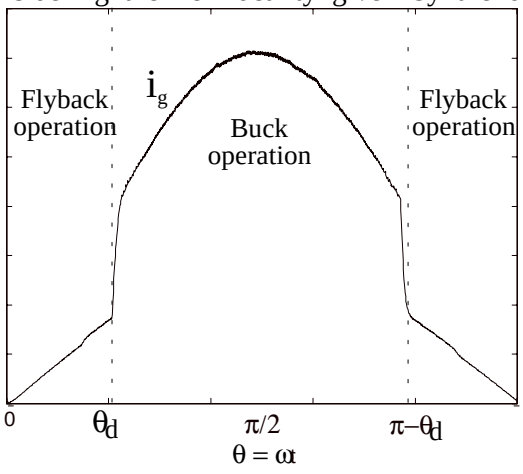


Fig. 4 - Filtered line current waveform for the modified tapped-inductor converter

angle θ_d. The peak of the average input current can be found from (6.a) and the power balance, i.e.:

$$\hat{I}_g = \frac{2P_o}{\hat{U}_g}\frac{1}{F} \tag{8}$$

Since the inductor value stores negligible energy at line frequency, the average second winding current $\bar{i}_2(\theta)$ during the conduction angle can be found by power balance as:

$$\bar{i}_2(\theta) = \frac{p_{in}(\theta)}{U_o} = \frac{\hat{U}_g \hat{I}_g \sin^2(\theta)}{U_o} \tag{9}$$

As a consequence, the apparent load seen by the converter results:

$$r_L(\theta) = \frac{U_o}{\bar{i}_2(\theta)} = \frac{R_L}{2\sin^2(\theta)}F \tag{10}$$

The voltage conversion ratio is given by:

$$m(\theta) = \frac{U_o}{u_g(\theta)} = \frac{M}{|\sin(\theta)|} \tag{11}$$

Substituting (10) and (11) into (2.a), the maximum switch current stress can be calculated for $\theta = \pi/2$ as:

$$\hat{i}_{S\max} = U_o\left[\frac{2}{R_L}\frac{n+M}{n+1}F + \frac{1-M}{2Lf_S}\left(\frac{1+n}{n+M}\right)\right] \tag{12.a}$$

The maximum switch voltage stress is simply given by:

$$\hat{u}_{S\max} = \hat{U}_g + \frac{U_o}{n} \tag{12.b}$$

Considering the flyback+buck operation, the idealized input current waveform can be expressed as:

$$\bar{i}_g(\theta) = \begin{cases} \hat{I}_g|\sin(\theta)| & \text{for} \quad \theta_d + h\pi \le \theta \le (h+1)\pi - \theta_d \\ k\hat{I}_g|\sin(\theta)| & \text{for} \quad -\theta_d + h\pi \le \theta \le \theta_d + h\pi \end{cases}$$

$h = 0, 1, 2, ...$ (13)

where *k* is the ratio between the sinusoidal reference peak value for the flyback operation and the sinusoidal reference peak value for the buck operation. Note that, for $k = 1$, the ideal absorbed current becomes a pure sinusoid.

All the above expressions during the buck mode remain valid provided that the factor F is modified as:

$$F = \left|1 - \frac{2\theta_d(1-k)}{\pi} + \frac{(1-k)\sin(2\theta_d)}{\pi}\right| \tag{14}$$

The switch current stress and the average input current during the flyback mode, assuming DCM operation, are given by:

$$\hat{i}_S(\theta) = S_{fly}(\theta)\, d(\theta) T_S \tag{15}$$

$$\hat{i}_g(\theta) = \hat{i}_S(\theta)\frac{d(\theta)}{2} = k\,\hat{I}_g\,|\sin(\theta)| \tag{16}$$

Thus, from (15) and (16), the maximum switch current stress results:

$$\hat{i}_{S\max} = \hat{i}_S(\theta_d) = \sqrt{2k\,\hat{I}_g\,|\sin(\theta_d)|\,S_{fly}(\theta_d)\,T_S} \tag{17}$$

From all the above equations the following converter design procedure is outlined:

- given the nominal power and voltage conversion ratio, the minimum value of *k* is calculated which makes compliance with the standards;
- the value of turns ratio *n* is selected from the desired switch voltage stress (12.b);
- the inductor value is calculated from the desired switch current stress in the buck mode (12.a);
- the maximum switch current stress during the flyback mode is checked: if it is lower then the value given by (12.a) a higher value of *n* can be selected; in the other case, a lower value of *n* should be chosen, thus increasing the voltage stress, or a higher current stress should be accepted. An optimum design should have the same current stress during both flyback and buck modes.

4.2 Capacitor

As usual, the output filter capacitor is selected from the constraint regarding the low-frequency output voltage ripple. The latter is derived by integrating the capacitor current over part of a half-line period. The expression for the capacitor current is the following:

$$\bar{i}_C(\theta) = \bar{i}_2(\theta) - I_o \tag{18}$$

The worst case peak-to-peak voltage ripple is given by:

$$\Delta u_o = \frac{1}{2\omega C}\left[(\pi - 2\theta_1)\left(\hat{I}_2 - 2I_o\right) + \hat{I}_2\sin(2\theta_1)\right] \tag{19}$$

where ω is the line angular frequency, $\hat{I}_2$ is the peak value of $\bar{i}_2(\theta)$ and

$$\theta_1 = \sin^{-1}\left(\sqrt{\frac{I_o}{\hat{I}_2}}\right) \qquad (20)$$

Capacitor C is then selected from (19) based on the desired output voltage ripple.

5. Experimental Results

A converter having the specifications and parameters listed in Table I was built and tested in order to verify the theoretical expectations.

TABLE I

CONVERTER PARAMETERS

U_g = 176÷264 V_{RMS}	U_o = 185 V	P_o = 1000 W
L = 580 µH	C = 2·680 µF	f_s = 50 kHz
n = 0.8		

A charge control was used in order to force a sinusoidal average input current for both buck and flyback operation modes, i.e. the input current is sensed and integrated cycle by cycle. The main switch S_1 is turned on at constant frequency and turned off when the integral of the switch current reaches a suitable sinusoidal reference (after that the integrator is reset) [4]. To implement such control, a standard PFC controller like the MC34261, which is normally used in boost PFC's designed to operate at the boundary between continuous and discontinuous conduction modes, was employed with some external circuitry.

The converter was tested at first in the tapped inductor buck PFP configuration. The outcoming filtered line current is shown in Fig. 5a together with the line voltage. The distortion in the voltage waveform is due to the impedance of the transfomer used to connect the converter to the grid. The spectrum of the line current is shown in Fig. 5b. Note that in the following measurements the input voltage amplitude is set to 230 V_{RMS}, as requested by the standards. As it is possible to see, the line current exhibits a noticeable low frequency distortion due to the dead-zone around the voltage zero crossings.

Nevertheless, as is confirmed by Table II which reports the amplitude of the first 19 harmonics, it is only the 15th harmonic which is above the limit imposed by the IEC 1000-3-2 standard. This basically depends on the output voltage level

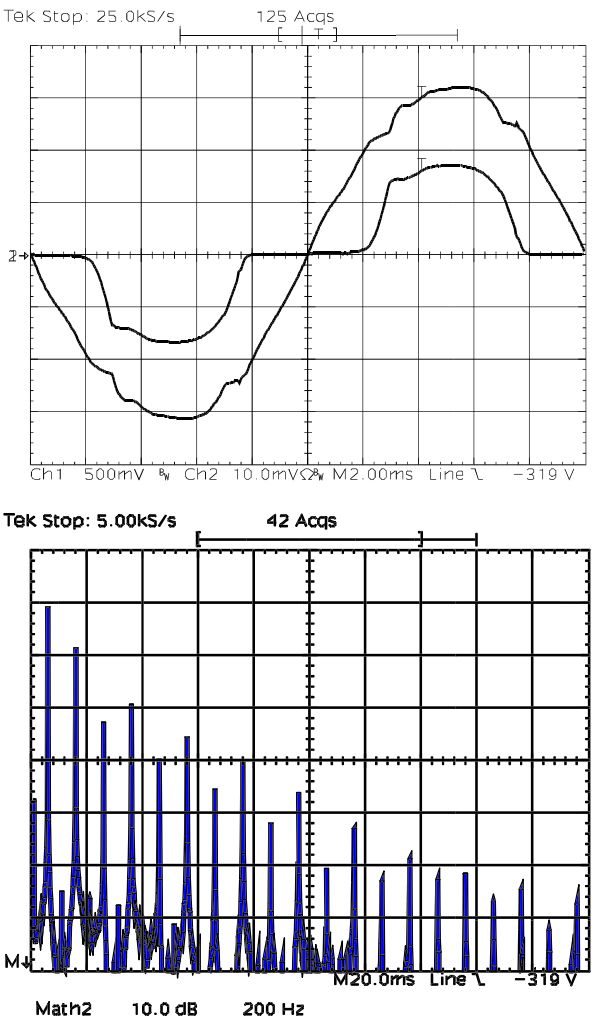


Fig. 5 - a) line voltage [100V/div] and current [5A/div] during buck operation;
b) spectrum of the line current - top line corresponds to 24dBA_{RMS} [10dB/div]

which, being fairly low with respect to the line voltage peak amplitude, allows a quite large conduction interval for the buck converter. For higher output voltage levels this may no longer be the case and lower order harmonics can be expected to exceed the standard limits.

The filtered input current waveform during operation of both buck and flyback stages is shown in Fig. 6a together with its spectrum (Fig. 6b); as it is possible to verify in Table II, the converter now complies with the standards.

6. Conclusions

The use of buck-type converters as power factor preregulators is limited by their inherent input current distortion to a maximum input power level, depending on the required voltage conversion ratio. Exceeding such power limit

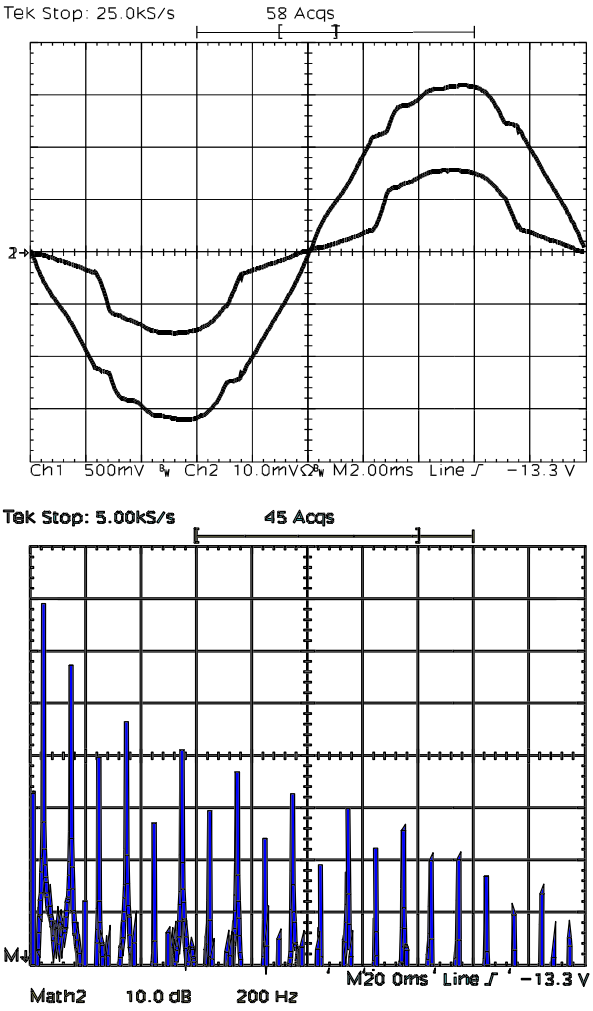


Fig. 6 - a) line voltage [100V/div] and current [5A/div] during buck+flyback operation;
b) spectrum of the line current - top line corresponds to 24dBA$_{RMS}$ [10dB/div]

implies the violation of the IEC 1000-3-2 standards, normally in the high order harmonic range.

This paper proposes a modification of the tapped-inductor buck converter which, employing only a line-frequency commutated switch and a diode, provide fully compliance with the standards.

A prototype of the proposed converter has been developed and tested. The paper reports the results of the experimental tests, which demonstrate the validity of the solution.

TABLE II
LINE CURRENT HARMONICS

Harmonic Order	Buck [A_{RMS}]	Buck+ Flyback [A_{RMS}]	IEC 1000-3-2 [A_{RMS}]
1	4.695	4.650	
3	1.930	1.195	2.30
5	0.374	0.160	1.14
7	0.560	0.335	0.77
9	0.162	0.035	0.40
11	0.278	0.175	0.33
13	0.082	0.050	0.21
15	**0.166**	**0.110**	**0.15**
17	0.040	0.025	0.13
19	0.088	0.065	0.12
21	0.016	0.010	0.11

References:

1- IEC 1000-3-2, First Edition 1995-03, Commission Electrotechnique Internationale, 3, rue de Varembé, Genève, Switzerland.

2 - A. S. Kislovski, "Internal Active Parallel DC Power-Factor and Line-Current Correctors," IEEE INTELEC Conf. Proc., 1996, pp. 131-136.

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4 - W. Tang, Y. Jiang, G.C.Hua and F.C.Lee, "Power Factor Correction With Flyback Converter Employing Charge Control," APEC Conf. Proc., 1993, pp. 293-298.