

# Analysis of EMI Filter Induced Instabilities in Boost Power Factor Preregulators

\*Giorgio Spiazzi, \*\*Leopoldo Rossetto

\*Dept. of Electronics and Informatics - \*\*Dept. of Electrical Engineering

University of Padova - Via Gradenigo 6/a - 35131 - Padova (ITALY)

Phone: +39.49.8277525 - Fax: +39.49.8277599

and José Antenor Pomilio

School of Electrical and Computer Engineering

University of Campinas - C.P. 6101 - 13081-970 Campinas - SP (BRAZIL)

Phone: +55.19.2393911 - Fax: +55.19.2391395

**Abstract.** The effects of a non negligible source impedance, due to the presence of an input EMI filter, on the stability of boost Power Factor Preregulators (PFP) are analyzed by using a simple State Space Averaged model. Differently from previous approach, it allows to derive a simple expression for the loop gain in terms of the converter current loop gain.

Based on this model, a simple modification of the standard converter current control loop is proposed which improves the converter robustness.

In order to assess the validity of the proposed approach, comparison between model predictions and experimental measurements were done using a boost PFP prototype rated at 600W.

## I. INTRODUCTION

The boost converter working in Continuous Conduction Mode (CCM) with average current control is probably one of the most popular solution for single-phase Power Factor Correction (PFC) thanks to its simplicity, low input current ripple and availability on the market of many control IC's. Moreover, the design of such converter is broadly described in many papers [1]. However, the complete AC to DC conversion requires an external EMI input filter in order to get rid of the high-frequency noise generated by the converter.

When the EMI filter is added, instabilities can arise in the system due to the interaction between the filter and the converter. This phenomenon is well known and many papers have already addressed it [2-6]. In particular [4] reports an analysis similar to that is presented here, but the derived loop gain does not provide easy insight into the PFC design. Moreover, it is not able to predict instabilities that the analysis presented here does and this is the main reason for this work.

The results of the performed analysis lead to a simple modification of the inner current loop of boost PFP's

which allows to improve converter robustness against filter-induced instabilities.

Measurements on a converter prototype allow useful comparison with previous analysis and highlight merits and limitations of the proposed approach.

## II. PROBLEM ANALYSIS

A simplified scheme of a boost PFP with average current mode control is shown in Fig.1 together with the EMI input filter. As we can see, an inner current loop forces the inductor current to follow a suitable reference signal which is obtained by sensing the rectified input voltage  $u_g$ . The output  $u_c$  of the voltage-error amplifier of the external output voltage loop sets the correct current reference amplitude based on the desired output voltage and power. Note that this signal is practically constant at frequencies above the line frequency since the voltage loop has a bandwidth much lower than the line frequency in order to maintain a good power factor [1]. The same figure also shows the circuit model which represents the interface between the filter and the converter in which the Thevenin equivalent circuit of the filter output was used ( $H_F$  is the filter attenuation,  $Z_{OF}$  is the filter output impedance and  $Z_{IC}$  is the converter input impedance). From this we can write:

$$\frac{u_g}{u_i} = \frac{H_F}{1 + \frac{Z_{OF}}{Z_{IC}}} = \frac{H_F}{1 + T_F} \quad T_F = \frac{Z_{OF}}{Z_{IC}} = Z_{OF} Y_{IC} \quad (1)$$

where  $T_F$  can be interpreted as a loop gain which must satisfy the Nyquist criterion for stability. If  $|T_F(j\omega)|$  were always lower than one, no instabilities could arise in the system and this sufficient criterion was largely used in the past, especially for dc-dc converters. However, in the case of ac-dc converters with high power factor, limitations exist both on the filter component values and on the converter design [7]. Thus we will see that it is quite

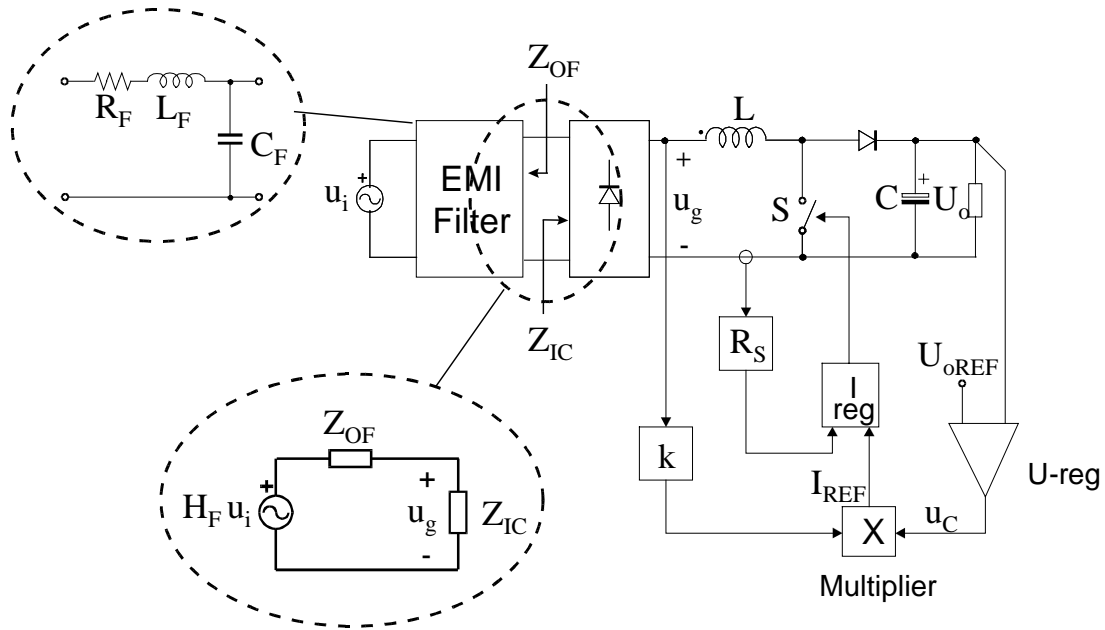


Fig. 1 - Basic scheme of a boost PFP with average current mode control

common to have  $|T_F(j\omega)| > 1$  in a frequency range above the inner current loop crossover frequency, especially at low line voltage and high load currents, and in this case the general approach for stability analysis must be followed.

From (1), the knowledge of the converter input impedance becomes a prerequisite for the stability analysis.

### III. CONVERTER INPUT IMPEDANCE

The converter input impedance (or admittance) is derived starting from the well known state space average model of the boost converter in CCM shown in Fig. 2a. In this figure, hat means perturbation respect to steady-state value represented by uppercase letters and d is the converter duty-cycle ( $d'=1-d$ ). For the purpose of input impedance calculation, the converter output voltage can be assumed constant due to the high output capacitor value needed to filter out the low frequency input power fluctuation. Thus, the model can be simplified as shown in Fig. 2b. From this model, the input current perturbation can be derived as follows:

$$\hat{i}_g = Y_{HF}(s)\hat{u}_g + G_{id}(s)\hat{d} = \frac{1}{sL}\hat{u}_g + \frac{U_o}{sL}\hat{d} \quad (2)$$

where  $Y_{HF}$  represents the high frequency input admittance, i.e. the admittance at frequency above the current loop crossover frequency in which d is constant, while  $G_{id}$  represents the transfer function between duty-cycle and input current which is used for the current loop gain calculation. In order to complete the analysis we need to express the perturbation of the duty-cycle as a function of controller parameters. To this purpose, let us consider the average current mode controller scheme shown in Fig. 3 which refers to a standard IC controller like the UC3854 or the L4981 (ignore for the moment capacitor  $C_6$ ).

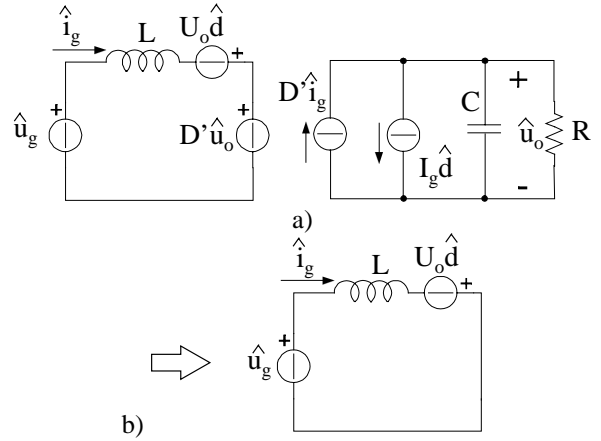


Fig. 2 - a) State space average model of boost converter in CCM; b) simplified model for input impedance calculation of a boost PFP

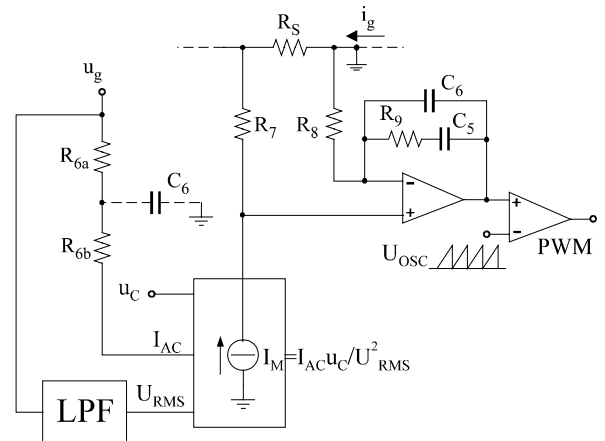


Fig. 3 - Average current mode controller scheme

From this scheme, considering that signals  $U_{RMS}$  and  $u_c$  are constants at the frequencies we are dealing with, the

converter duty-cycle can be expressed as a function of rectified input voltage  $u_g$  and input current  $i_g$ :

$$\hat{d} = K_u(s)\hat{u}_g + K_i(s)\hat{i}_g \quad (3)$$

where coefficients  $K_u$  and  $K_i$  are given by (see Appendix I):

$$K_i(s) = -\frac{R_S}{U_{OSC}} G_{ri}(s) \quad (4a)$$

$$K_u(s) = -\frac{I_g}{U_g} K_i(s) = -G_{IC} K_i(s) \quad (4b)$$

where  $R_S$  is the current sensing resistance,  $U_{OSC}$  is the amplitude of the PWM modulator ramp signal and  $I_g$  and  $U_g$  are input current and voltage RMS values.

Combining (2-4), the input admittance can be derived as follows:

$$Y_{IC}(s) = \frac{1}{sL} \frac{1}{1+T_i(s)} + G_{IC} \frac{T_i(s)}{1+T_i(s)} \quad (5)$$

where  $G_{IC}$  is the low frequency input conductance given by

$$G_{IC} = \frac{1}{R_{IC}(s)} = \frac{I_g}{U_g} = \frac{P_{OUT}}{U_g^2} \quad (6)$$

and  $T_i(s)$  is the current loop gain which can easily derived from (2) and (3) by setting  $\hat{u}_g = 0$ , and is given by:

$$T_i(s) = -G_{id} K_i(s) = \frac{U_o}{sL} \cdot \frac{R_S}{U_{osc}} \cdot G_{ri}(s) \quad (7)$$

From (3) we can make the following considerations:

- differently from a previously derived model [4], the input impedance does not depend on the instantaneous input voltage but only on its RMS value through  $G_{IC}$  (see (4));
- at frequencies below the current loop bandwidth ( $|T_i(j\omega)| \gg 1$ ) the input impedance is constant and equal to  $R_{IC}$ , while at higher frequency it coincides with the input inductance impedance  $sL$ .

Gain and phase plots of  $Z_{IC}(s)$  for three different values of the input voltage are reported in Fig. 4 (converter parameters values are reported in table I of the experimental measurements section): the worst case condition is for the minimum input voltage and maximum load current.

#### IV. EXPERIMENTAL MEASUREMENTS

In order to validate the model, a boost PFC, whose parameter values are reported in table I, was built and tested. It was supplied from the utility grid using an isolating transformer plus an autotransformer in order to vary the converter input voltage. The output inductance of

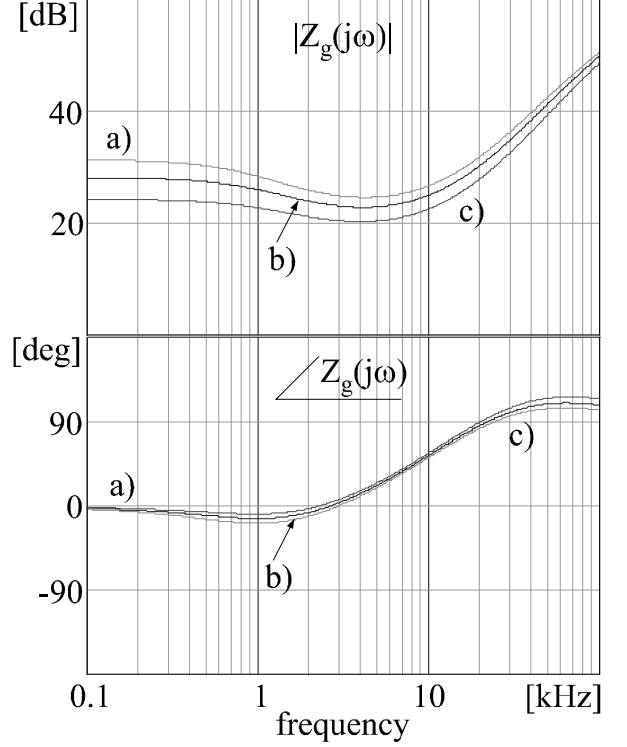


Fig. 4 - Bode plots of gain and phase of input impedance of the boost PFC.

a)  $U_g = 127V+20\%$ , b)  $U_g = 127V$ , c)  $U_g = 127V-20\%$

the supply line, which works as a filter inductance, was measured at different voltages so has to use it in the input filter model. The latter is thus a simple single-cell  $R_F$ - $L_F$ - $C_F$  filter as shown in Fig. 1.

The current loop regulator transfer function  $G_{ri}(s)$  is a PI regulator with a high frequency additional pole in order to reject the high-frequency input current ripple, i.e.:

$$G_{ri}(s) = 1 + \frac{\omega_{ri}}{s} \left( \frac{1+s\tau_{zi}}{1+s\tau_{pi}} \right) \quad (8)$$

With the parameter values used for the current error amplifier listed in table I, the current loop bandwidth varies from 5kHz to 8.3kHz in the output voltage range  $U_o = 180\div 300V$ . Comparisons between experimental measurements of the boost PFC and model predictions are reported in table II for different operating points. The column corresponding to the experimental measurements reports the value of peak input voltage at which instability arises together with the corresponding oscillation frequency, the column labeled MODEL PREDICTION I reports the same information derived from the model and the column MODEL PREDICTION II reports the crossover frequency and the phase margin as given by the model in correspondence of the measured input voltage

Table I - Boost converter parameter values

$U_g = 127 V_{RMS} \pm 20\%$	$U_o = 300 V$	$P_o = 600 W$	$f_s = 70 kHz$	$L = 650 \mu H$	$C = 235 \mu F$
$R_S = 33 m\Omega$	$U_{osc} = 5 V$	$\omega_{ri} = 1.92 \cdot 10^5$	$f_{zi} = 1.8 kHz$	$f_{pi} = 34.5 kHz$	$f_{ci} = 8.3 kHz$

**Table II - Comparison between model forecasts and experimental measurements for the boost PFP**

N°.	OPERATING POINT ( $U_o, I_o$ )	FILTER PARAMETERS ( $L_F, C_F$ )	EXPERIMENTAL RESULTS	MODEL PREDICTION I	MODEL PREDICTION II	PREVIOUS MODEL $\theta = \pi/200$	PREVIOUS MODEL $\theta = \pi/2$
1	180V 2.75A	0.89mH 0.47 $\mu$ F	$\hat{U}_g = 119V$ $f_{osc} = 17.24kHz$	$\hat{U}_g = 125V$ $f_{osc} = 16.34kHz$	$f_{cr} = 16.7kHz$ $m_\phi = -1.4deg$	$\hat{U}_g = 130V$ $f_{osc} = 16kHz$	$\hat{U}_g = 98V$ $f_{osc} = 19.7kHz$
2	220V 0.8A	1.12mH 0.47 $\mu$ F	$\hat{U}_g = 76.4V$ $f_{osc} = 17.86kHz$	$\hat{U}_g = 71V$ $f_{osc} = 17.2kHz$	$f_{cr} = 16.6kHz$ $m_\phi = 2.3deg$	$\hat{U}_g = 91.5V$ $f_{osc} = 15.1kHz$	$\hat{U}_g = 70.5V$ $f_{osc} = 17.5kHz$
3	220V 1A	1.12mH 0.47 $\mu$ F	$\hat{U}_g = 84.4V$ $f_{osc} = 18.12kHz$	$\hat{U}_g = 79.6V$ $f_{osc} = 17.2kHz$	$f_{cr} = 16.7kHz$ $m_\phi = 2deg$	$\hat{U}_g = 102.5V$ $f_{osc} = 15kHz$	$\hat{U}_g = 77V$ $f_{osc} = 17.8kHz$
4	220V 1.5A	1.07mH 0.47 $\mu$ F	$\hat{U}_g = 100V$ $f_{osc} = 18.2kHz$	$\hat{U}_g = 98V$ $f_{osc} = 17.2kHz$	$f_{cr} = 17kHz$ $m_\phi = 0.7deg$	$\hat{U}_g = 125V$ $f_{osc} = 15.1kHz$	$\hat{U}_g = 90V$ $f_{osc} = 18.7kHz$
5	220V 2A	0.89mH 0.47 $\mu$ F	$\hat{U}_g = 118V$ $f_{osc} = 18kHz$	$\hat{U}_g = 115V$ $f_{osc} = 17.34kHz$	$f_{cr} = 17.13kHz$ $m_\phi = 0.9deg$	$\hat{U}_g = 145V$ $f_{osc} = 15.4kHz$	$\hat{U}_g = 101.5V$ $f_{osc} = 19.5kHz$
6	300V 1A	1mH 0.47 $\mu$ F	$\hat{U}_g = 105V$ $f_{osc} = 18.5kHz$	$\hat{U}_g = 90V$ $f_{osc} = 19.3kHz$	$f_{cr} = 17.74kHz$ $m_\phi = 6.1deg$	$\hat{U}_g = 133V$ $f_{osc} = 16.1kHz$	$\hat{U}_g = 99V$ $f_{osc} = 19kHz$
7	300V 1.5A	0.67mH 0.47 $\mu$ F	$\hat{U}_g = 127V$ $f_{osc} = 17.86kHz$	$\hat{U}_g = 114V$ $f_{osc} = 19.5kHz$	$f_{cr} = 18.5kHz$ $m_\phi = 4.1deg$	$\hat{U}_g = 166V$ $f_{osc} = 16.6kHz$	$\hat{U}_g = 117V$ $f_{osc} = 20.4kHz$
8	300V 2A	0.55mH 0.47 $\mu$ F	$\hat{U}_g = 144V$ $f_{osc} = 18.2kHz$	$\hat{U}_g = 136V$ $f_{osc} = 19.8kHz$	$f_{cr} = 19.2kHz$ $m_\phi = 2.3deg$	$\hat{U}_g = 193V$ $f_{osc} = 17kHz$	$\hat{U}_g = 133V$ $f_{osc} = 21.3kHz$

value in which oscillations appear. As we can see, there is a pretty good agreement between model forecasts and experimental measurements.

Note that the value used in the model for  $R_F$  was the DC value equal to  $0.9\Omega$ . However, in this case the model is not much sensible to the value of this resistance. For example, using a non linear  $R_F$  value of the type  $R_F(f) = 0.9 + 0.1\sqrt{f}$  so as to better model the skin effect in the equivalent input filter only small variations of the values reported in Table III were observed.

Table II reports also the results obtained with a previously proposed model [4]: in particular, the last two columns report the values of peak input voltage at which instability arises together with the corresponding oscillation frequency in correspondence of two different points of the line half period. As we can see, the dependency of these model predictions on the line angle  $\theta$  is not negligible as assessed in [4] and leads to a bigger error on the instability prediction compared to the proposed one. The bode plots of loop gain  $T_F(j\omega)$  corresponding to the operating point of measurement N°. 5 of table II for the proposed and previous models are reported in Fig. 5. The latter is reported for the two line angle  $\theta = \pi/200$  and  $\theta = \pi/2$ .

#### V. MODEL ACCURACY

A more careful reading of the data reported in table II for the boost converter, reveals that the difference between measurements and model predictions depends on the output voltage value, i.e. depends on the bandwidth of the inner current loop. In order to assess the model accuracy experimental measurements were done on the boost PFP at different current loop bandwidths. The results can be

summarized as follows: the phase margin given by the model in the operating conditions in which instabilities occurs in the prototype is plotted in Fig. 6 against the current loop bandwidth normalized to the switching frequency. As we can see the model prediction becomes more accurate, in terms of phase margin, at lower current loop bandwidths, while the oscillation frequency

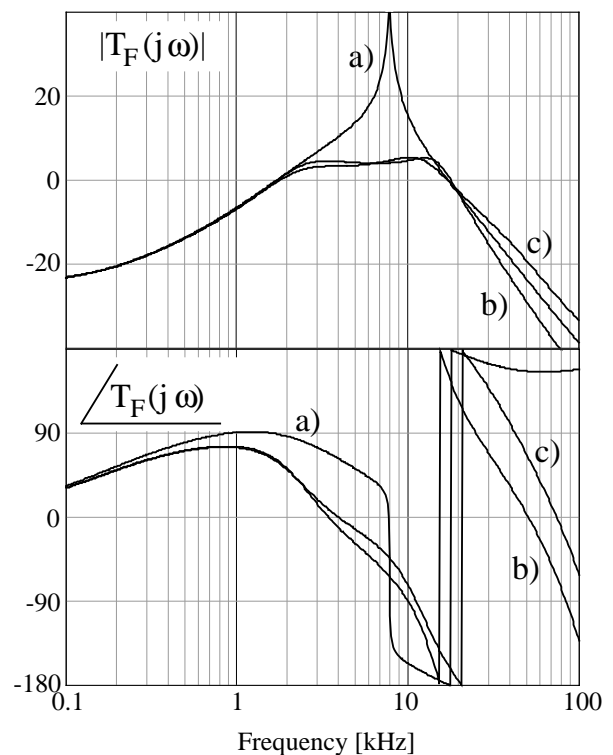


Fig. 5 - Gain and phase plots of loop gain  $T_F(j\omega)$  at  $\hat{U}_g = 118V$ . a) proposed model; b) model [4] with  $\theta = \pi/200$ ; c) model [4] with  $\theta = \pi/2$

prediction remains pretty good even at higher current loop bandwidths. Clearly, delays in the loops exist which are not accounted for by the simple small signal model employed.

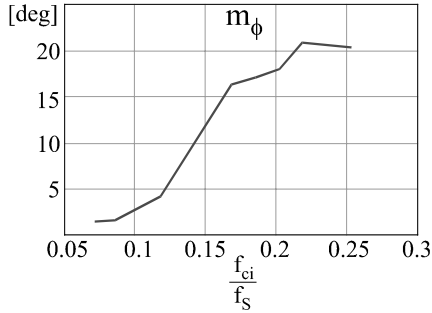


Fig. 6 - Predicted phase margin calculated in the conditions in which instabilities occur in the prototype as a function of the normalized current loop bandwidth

## VI. CURRENT LOOP MODIFICATION

The derivation of expression (5) suggests a simple modification of the controller so as to increase the system robustness against instabilities. In particular, we can note that the second term at the right hand side of (5), which comes from the term  $K_u(s)$  in (3) i.e. from the path from  $u_g$  to  $I_{REF}$  shown in Fig. 1, is the term which depends on the RMS input voltage. If we insert a low pass filter into the current reference path with a sufficiently high corner frequency so as not to appreciably degrade the rectified sinusoidal reference, then the converter input admittance  $Y_{IC}(s)$  modifies as:

$$Y_{IC}(s) = Y_{HF}(s) \frac{1}{1 + T_i(s)} + G_{IC} \frac{T_i(s)}{1 + T_i(s)} \frac{1}{1 + s\tau_{PB}} \quad (9)$$

Comparison between the resulting loop gain  $T_F(j\omega)$  and the previous one without low-pass filter is shown in Fig. 7 ( $f_{PB} = 1/(2\pi\tau_{PB}) = 1.85\text{kHz}$ ) which refers to the boost converter in the operating point corresponding to measure n°. 5 in table II. As we can see, this simple controller modification reduces the loop crossover frequency from 17.13kHz ( $f_{ca}$  in figure) to 12.2kHz ( $f_{cb}$  in figure) and increases the phase margin from  $0.9^\circ$  to  $18.4^\circ$ .

This low-pass filter can be inserted simply by modifying the controller scheme with the insertion of capacitor  $C_6$  as shown in Fig. 3.

Adding this low pass filter in the current reference path the system turns out to be stable in all operating conditions, even at the higher current loop bandwidth (17kHz).

## VII. CONCLUSIONS

In this paper the interactions between the input EMI filter, and the boost Power Factor Preregulator with average current control are analyzed. A simple expression for the loop gain in terms of the converter current loop

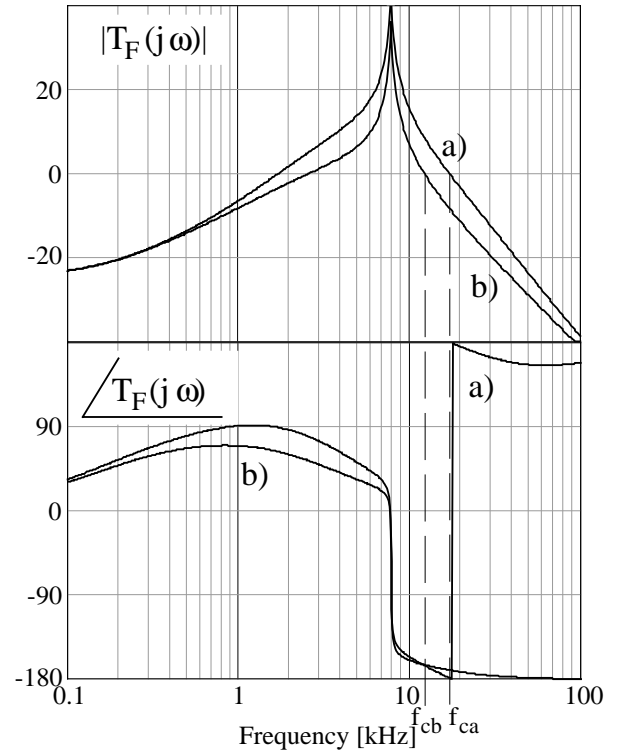


Fig. 7 - Gain and phase plots of loop gain  $T_F(j\omega)$  at  $\hat{U}_g = 118\text{V}$ . a) standard implementation; b) with the low-pass filter in the current loop

gain was derived which allows useful insight into the converter controller design.

Based on this model, a simple modification of the standard converter current control loop is proposed which improves the converter robustness.

Experimental measurements on a boost PFP prototype revealed merits and limitations of the proposed approach.

## VIII. REFERENCES

- [1] - C. De Sae Silva, "Power Factor Correction with the UC3854," Unitrode Integrated Circuit Co., February 1990.
- [2] - R. D. Middlebrook, "Input Filter Considerations in Design and Application of Switching Regulators," IEEE IAS Conf. Rec., 1976, pp.366-382.
- [3] - S. Y. Erich, W. M. Polivka, "Input Filter Design for Current-Programmed Regulators," IEEE APEC Conf. Proc., 1990, pp.781-791.
- [4] - R. Redl, A. S. Kislovsky, "Source Impedance and Current-Control Loop Interaction in High-Frequency Power-Factor Correctors," IEEE PESC Conf. Proc., 1992, pp.483-488.
- [5] - R. D. Middlebrook, "Input Filter Considerations in Design and Application of Switching Regulators," IEEE IAS Conf. Rec., 1976, pp.366-382.
- [6] - R. D. Middlebrook, "Design Techniques for Preventing Input-Filter Oscillations in Switched-Mode Regulators," Power Conversion Conf. Proc., May 4-6, 1978.

- [7] - V. Vlatkovic, D. Borojevic, F. C. Lee, "Input Filter Design for Power Factor Correction Circuits," IEEE Trans.on Power Electronics, Vol.11, No.1, January 1996, pp.199-205.

#### IX. APPENDIX I

From the control scheme shown in Fig. 3, which represents the standard implementation of the average current mode control (see [1]) we can derive the expression for the duty-cycle as:

$$d(\theta) = \frac{G_{ri}(s)}{U_{OSC}} (R_7 i_M(\theta) - R_S i_g(\theta)) \quad (A.1)$$

From Fig. 3, the multiplier produces an output current  $i_M$  which is given by (as already stated in the paper, signal  $U_{RMS}$ , which represents a feedforward path, is constant during a line period and thus it can be considered constant at the much higher frequencies we are interested in):

$$i_M(\theta) = \frac{u_g(\theta)}{k} u_c \quad (A.2)$$

where  $k = (R_{6a} + R_{6b}) U_{RMS}^2$ . At steady state, the average (in a switching period) input current is equal to its reference, i.e.

$$R_7 I_M(\theta) = R_S I_g(\theta) \quad (A.3)$$

where uppercase means steady state conditions.

Considering a perturbation around an instantaneous (during the line period) working point, from (a.2) we can obtain

$$\hat{i}_M = \frac{U_c}{k} \hat{u}_g + \frac{U_g(\theta)}{k} \hat{u}_c = \frac{I_M(\theta)}{U_g(\theta)} \hat{u}_g + \frac{I_M(\theta)}{U_c} \hat{u}_c \quad (A.4)$$

Now substituting (a.4) into (a.1) and using (a.3) we can write (remember that we assumed for this calculation  $\hat{u}_c = 0$ )

$$\hat{d} = \frac{G_{ri}(s)}{U_{OSC}} \left( R_S \frac{I_g(\theta)}{U_g(\theta)} \hat{u}_g - R_S \hat{i}_g \right) \quad (A.5)$$

from which the coefficients of (3) can be easily derived as

$$K_i(s) = -\frac{R_S}{U_{OSC}} G_{ri}(s) \quad (A.6)$$

$$K_u(s) = -\frac{I_g(\theta)}{U_g(\theta)} K_i(s) = -\frac{I_g}{U_g} K_i(s) = -G_{IC} K_i(s) \quad (A.7)$$

where a sinusoidal input current was assumed. In this derivation we neglected capacitor  $C_6$  which is the control modification proposed in the paper. Taking it into account (a.2) modifies as

$$i_M(\theta) = \frac{u_g(\theta) u_c}{k} \frac{1}{1 + s\tau_{PB}} \quad (A.8)$$

where  $\tau_{PB} = C_b \frac{R_{6a} R_{6b}}{R_{6a} + R_{6b}}$ . Consequently, (5) becomes (9).

