Simplified Control Technique for High-Power-Factor Flyback Cuk and Sepic Rectifiers Operating in CCM

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Abstract - **Control techniques for high power factor rectifiers which do not need input voltage sensing are gaining considerable attention due to their simpler implementation and inherently superior stability, as compared to conventional average or peak current mode control. Among these, the solutions based on integration of a current signal (switch, diode or inductor current) provide an inherent noise immunity, which makes them further appealing.**

This paper proposes a simple implementation of one of such control techniques for high power factor flyback, Cuk or Sepic rectifiers, which, while still retaining a high power factor, further reduces the control complexity, thus making the solution very attractive for smart-power integration.

A 200W flyback rectifier with the proposed control technique was implemented and tested. The achieved results are in good agreement with the expected performance.

I. INTRODUCTION

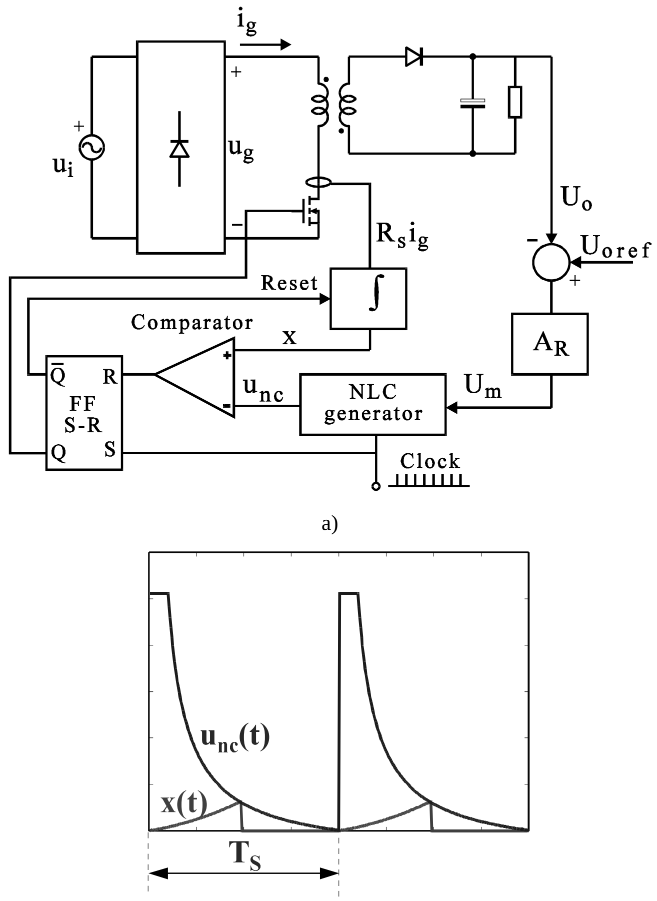
Recently, control techniques for high power factor rectifiers operating in continuous conduction mode (CCM), which avoid the input voltage sensing, have received great attention due to their advantages, in terms of control complexity, compared to the well known average or peak current mode control. In particular, the absence of the multiplier/divider and of the current error amplifier, together with the inherent stability of the current loop are the main advantages of these solutions, with respect to the standard controllers. In many of the presented solutions, suitable nonlinear carrier (NLC) waveforms are utilized together with the switch, diode or inductor current sensing in order to achieve high power factor ([1]-[3]). Such NLC waveforms are derived based on the steady-state voltage conversion ratio and thus depend on the converter topology and on which current is sensed. In other cases, a linear negative ramp carrier is employed as proposed in [4] and [5] with the aim of simplifying the carrier generator circuit. The latter solutions allow to derive unity power factor flyback rectifiers only by complex manipulation of the converter current signal. For example, a double integral of the switch current is proposed in [4], [5] and [6] with different possible implementations.

Not all of these solutions are able to achieve unity power factor and, in any case, all of them suffer for some degree of input current distortion in the case of discontinuous conduction operating mode of the converter (which can occur only during a portion of the line half-period). However, this does not represent a big problem, since low frequency harmonic standards like IEC 1000-3-2 allow a certain degree of current distortion, which simplifies the PFC design especially at low power levels (Class A equipment). The modest residual input current distortion is in any case abundantly below the limits, considering also the reduced power levels achievable with the considered converter topologies.

In this paper a rugged and robust control technique for flyback, Cuk and Sepic rectifiers operating in CCM is proposed, which basically consists of a simplification of the control approach presented in [4]-[6]. Its final reduced complexity makes it very attractive for the integration in a smart-power integrated circuit (IC), comprising both the control circuitry and the power switch. The availability of such an IC will make it possible to develop cost-effective and compact PFCs' designs, with minimum number of components on the printed circuit board.

In particular, in section II, the NLC control technique is reviewed together with its variations, while in section III some general features regarding the technology which is going to be employed for the future integration of the control circuit and the power switch on the same silicon chip are discussed.

In section IV a detailed description of the control implementation is presented, where the peculiarities of the integration technology and the available design options are discussed. Finally, some experimental results from a 200 W flyback prototype, built using discrete components, are shown in section V. These demonstrate the validity of the proposed approach.



a)

b)

Fig. 1 - a) High power factor flyback rectifier with a general nonlinear carrier control; b) main controller waveforms

II. REVIEW OF NLC CONTROL FOR FLYBACK RECTIFIERS

This control technique was originally presented by Maksimovic at al. for the boost power factor corrector in [1] and extended to flyback, Cuk and Sepic rectifier in [2].

Let us refer to Fig. 1a which shows the basic scheme of a high power factor rectifier based on the flyback topology, together with a general NLC controller, whose operation is based on the switch current sensing. The latter is preferred over the diode current information since it allows an easy switch protection implementation. The average input current is given by:

$$\bar{i}_g(\theta)=\frac{1}{T_S}\int_0^{dT_S} i_g(\tau)\,d\tau=\frac{u_g(\theta)}{R_e}, \qquad (1)$$

where the second equality states that, in order to obtain a unity power factor, the absorbed current must be proportional to the input voltage (R_e is the emulated resistance which depends on actual power delivered to the load). Note that overlined variables are averaged in a switching period, and therefore are, in general, a function of the instantaneous line angle *θ*. Assuming a continuous conduction mode (CCM) of operation, the voltage conversion ratio m(θ) is given by:

$$m(\theta)=\frac{U_o}{u_g(\theta)}=n\frac{d(\theta)}{1-d(\theta)}, \qquad (2)$$

where $n = N_2/N_1$ is the transformer turns ratio.

By deriving $u_g(\theta)$ from (2) and substituting it into (1) we obtain:

$$\frac{R_S}{T_S}\int_0^{dT_S} i_g(\tau)\,d\tau=\frac{R_S}{R_e}\frac{U_o}{n}\left(\frac{1-d(\theta)}{d(\theta)}\right)=U_m\left(\frac{1-d(\theta)}{d(\theta)}\right) \qquad (3)$$

where R_s is the equivalent current sensing resistance.

In (3), the emulated resistance R_e can by varied by the control signal U_m produced by the outer voltage feedback loop (see Fig. 1a). In the steady state $R_e = U_{gpeak}^2 / 2P_o$, as can be derived from the converter power balance (unity efficiency assumed) while the control signal is $U_m = \frac{R_S}{R_e}\frac{U_o}{n} = 2nM^2R_SI_o$, where $M = U_o/(n\cdot U_{gpeak})$. Since the duty-cycle d is defined as T_{on}/T_s, (3) can be written as:

$$\frac{R_S}{T_S}\int_0^{t} i_g(\tau)\,d\tau=U_m\left(1-\frac{t}{T_S}\right)\frac{T_S}{t}=u_{nc}(t), \qquad (4)$$

where the equality holds for $t = T_{on}$. Thus, the control strategy is as follows: a clock signal determines the switch turn on instant while the instant of turn off is derived by comparing the integral of the switch current with the nonlinear carrier waveform $u_{nc}(t)$ given by the right hand side of (4) (trailing-edge control). It is important to note that the same control approach can also be used with Cuk and Sepic rectifiers since they have the same voltage conversion ratio and the average switch current is equal to the average input current. The NLC control scheme is shown in Fig. 1a, and its main waveforms are reported in Fig. 1b.

As we can see, such control does not need any input voltage sensing nor multiplier/divider and current error amplifier. However, the generation of the exact nonlinear carrier signal $u_{nc}(t)$ is not straightforward.

In section IV, a simplified control strategy is proposed which allows the minimization of the controller complexity, at the only expense of a little increase in the input current harmonic distortion. As it will be explained in the following, this is one of the main concerns in the design of the smart power IC we are aiming at. Before that, in the following section, some general issues regarding the integration technology are presented.

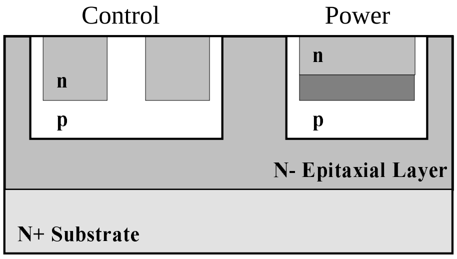


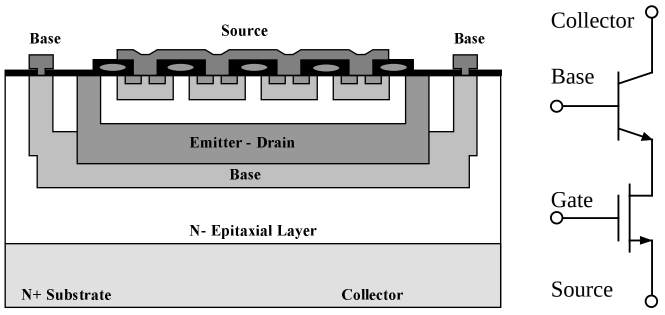
Fig. 2 - VIPower® Technology

III. VIPOWER® M3 TECHNOLOGY

The reference technology for the application this paper deals with is the VIPower® M3 technology by ST Microelectronics. This technology allows the integration of a new type of power device called *emitter switching* and of all the required protection and control circuitry. As shown in Fig. 2, the control part is, at least in static conditions, electrically isolated from the power device part of the IC by means of reverse-biased p-n junctions. In the M3 level of the VIPower technology a BCD-based control circuit can be implemented, where bipolar (both NPN and PNP), CMOS and DMOS devices can be employed. The typical operating voltage is about 25 V.

Based on the thickness and resistivity of the N+ substrate, the voltage rating of the power stage can range from 400 V to 1500 V. The maximum current level, depending on the size of the power stage, can get to 10÷15 A maximum.

Fig. 3 shows the typical emitter switching structure. As can be seen, even if in Fig. 3.b the emitter switching is represented as an equivalent series connection of two discrete devices, the actual power device is made up of the combination in a *sandwich* structure of a high voltage bipolar NPN transistor and a low voltage DMOS transistor. It is worth noting that this solution allows the integration of the DMOS inside the emitter area of the BJT, which implies that the used silicon area is that due only to the bipolar device. Moreover, the emitter of the bipolar device also represents the drain of the DMOS. This connection is buried inside the component, and therefore a much shorter current path, compared with the series connection of two discrete devices, is achieved.



a) b)

Fig. 3 - Emitter Switching device: a) schematic of device structure; b) equivalent circuit

Finally, a key feature of this device is the minimization of the storage time in the bipolar component at turn-off, which gives to the emitter switching a quite high switching speed, comparable to that of a power MOSFet. This effect is achieved by giving a suitable discharge path to the base current which, at turn-off is instantaneously made equal to the collector current by the quick opening of the DMOS transistor. Being as high as the collector current, the turn-off base current very quickly sweep the accumulated charge off the bipolar transistor base, determining a very fast turn-off of the bipolar switch.

IV. PROPOSED CONTROL IMPLEMENTATION

The exact hyperbolic waveform $u_{nc}(t)$, derived from (4) in section II, can be actually well approximated by a clamped exponential waveform, as proposed in [2]; however, its hardware implementation still requires a sample and hold circuit and an extra capacitor, whose discharge voltage provides the desired exponential waveform.

A different implementation can be derived by rearranging (4), as shown in the following:

$$\frac{t}{T_S}\frac{R_S}{T_S}\int_0^t i_g(\tau)d\tau = U_m\left(1-\frac{t}{T_S}\right). \tag{5}$$

Here, simply moving the term $d(\theta)$ from the right to the left-hand side of (3), the carrier waveform becomes a simple linear decreasing ramp, whose amplitude is imposed by the output of the voltage error amplifier. The control's complexity is now limited to the generation of the left-hand term of (5). Actually, this can be seen as an increasing ramp having a variable amplitude, given by the average input current value in a particular switching period (or in the previous one, as proposed in [5]). Alternatively, it can be approximated by the double integration of the switch current (if the inductor current has a small relative ripple), as proposed in [4] and [6]. Both of these solutions, however, appear to be a little too complicated for a cost-effective and reliable smart-power integrated circuit. It is worth underlining that the solution we are here presenting is aimed at the implementation of a general purpose and low-cost type of product and, therefore, our goal is to achieve a satisfactory performance level with the minimum control circuit complexity.

Moreover, the harmonic standards like IEC 1000-3-2, provided that a Class A input current waveform is achieved, allow a significant amount of current distortion, especially at the low power levels achievable with such a converter topology. Based on these considerations, a simple single switch current integration was chosen as an approximation of the left-hand side of (5).

Besides, since the control signal U_m is a slowly varying signal (the output voltage control loop has a bandwidth well below the line frequency), the negative slope ramp appearing on the right-hand side of (5) can be generated by integrating the control signal U_m itself, together with the current signal. According to this approach, the control equation can be rewritten as:

$$U_m = \frac{1}{T_s}\int_0^t \left(R_s i_s(\tau) + U_m\right) d\tau = \frac{R_s}{T_s}\int_0^t i_s(\tau)\, d\tau + \frac{U_m}{T_s} t \qquad (6)$$

As a result, the control implementation modifies as shown in Fig. 4. As can be seen, only one integrator with reset is needed to perform the integration of the sum of the control signal U_m and the signal proportional to the switch current. The resulting signal is compared with U_m, so as to derive the switch on-time. Note that this scheme is similar to that reported in [6], but a single integrator is used here instead of two.

Such a simple control approach, requiring very few blocks and having a potentially high immunity to the switching noise, thanks to the signal integration, is suitable for the implementation in the VIPower® M3 technology. Moreover, the intended universal input voltage range of operation (90÷264 V_{RMS}) and the power rating of about 200 W for the typical application, imply a switch current stress of 6.5 A and a switch voltage stress of 800 V (taking into account the snubber operation in the flyback converter, not shown in Fig. 1), which are well within the power handling capability of this technology.

A possible block diagram of the smart power chip is given in Fig. 5. It is worth noting a peculiar feature of the M3 level of VIPower® technology: the switch current is internally sensed by means of an integrated low value resistor. The number of external components needed to complete the circuit is therefore limited to the minimum. The voltage drop across the sensing resistor is then converted into a current, which is finally integrated through the external capacitor C_{INT} together with a current proportional to the output of the voltage error amplifier. Note that this second voltage-to-current converter can be avoided by using a transconductance error amplifier, also available in the technology blockset. The switch shown in figure reset the integration capacitor every switching cycle. The other blocks shown in Fig. 5 (comparator, flip-flop, clock generator, etc.) are standard blocks, which can be found in any control IC and are of course also available in the VIPower technology. Note that a cycle-by-cycle switch current protection can be easily added to the controller due to the internal current sensing. Finally, the internal power switch is the *emitter switching* structure described in the previous section.

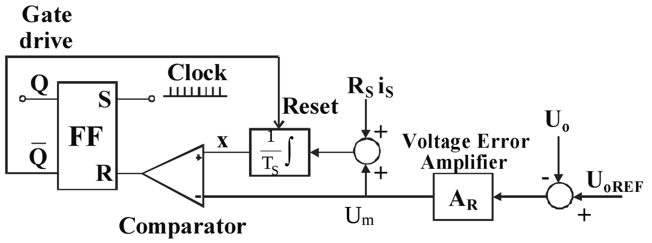


Fig. 4 - Proposed control scheme

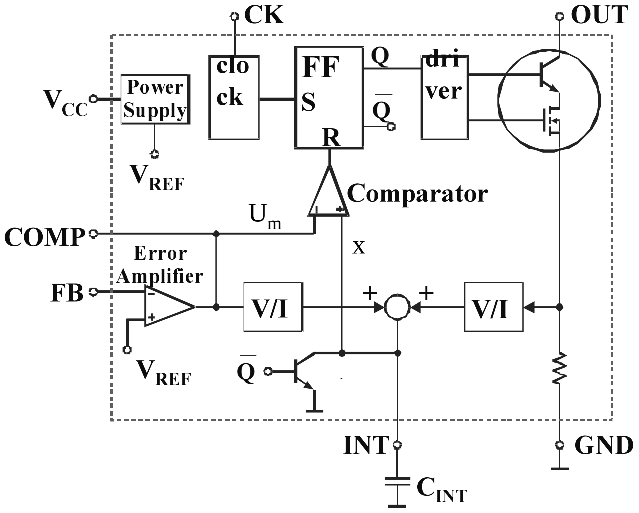


Fig. 5 – Possible smart power integration scheme

We now complete the analysis of the control technique we have chosen, by investigating its intrinsic residual current distortion. In order to have an idea of the deviation of the average input current from the ideal sinusoidal one we must observe that the chosen control strategy is equivalent to neglect the term $d(\theta)$ at the denominator of the right side of (3), that is to say:

$$\bar{i}_g(\theta) = \frac{U_m}{R_s}\left(1 - d(\theta)\right) = \frac{U_m}{R_s}\frac{\left|\sin(\theta)\right|}{\left|\sin(\theta)\right| + M} \qquad (7)$$

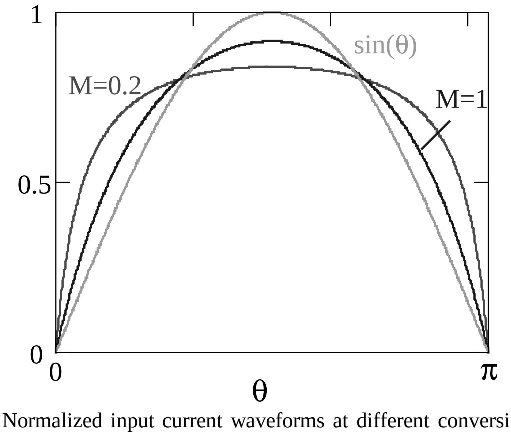


Fig. 6 - Normalized input current waveforms at different conversion ratios M compared to the ideal sinusoidal waveform (same unity fundamental component amplitude)

Fig. 6 reports a comparison between the ideal sinusoidal and the waveforms given by (7) for two different conversion ratios M (all waveforms normalized to a unity fundamental component). These waveforms have an harmonic content well below Class A limits of IEC 1000-3-2, at least up to some hundred Watts. It is worth noting that a certain amount of input current distortion would be produced in any case, even if the exact non linear carrier signal was used. This happens because of the converter transition to discontinuous conduction mode of operation (DCM) which takes place when the input voltage is close to zero.

V. EXPERIMENTAL RESULTS

A 200W flyback rectifier, whose parameters are listed in Table I, was built using standard discrete components in order to test the performance of the proposed simplified control. The input current and voltage waveforms, in the nominal conditions, are shown in Fig. 7a for $U_g = 90V_{RMS}$, and Fig. 7b for $U_g = 230V_{RMS}$.

TABLE I

CONVERTER PARAMETERS

Input Voltage U_g	90-260 V_{RMS}
Output Voltage U_o	48 V
Output Power P_o	200 W
Inductor L	1 mH
Filter Capacitor C	2200 μF
Switching Frequency f_s	50 kHz
Transformer Turns Ratio n	0.165

TABLE II

MEASURED INPUT CURRENT HARMONICS FOR THE PROPOSED RECTIFIER AT $U_g = 230V_{RMS}$

I_n	**Harm. [A_{rms}]**	**Class A limits [A_{rms}]**
I_3	0.0794	2.30
I_5	0.0339	1.14
I_7	0.0257	0.77
I_9	0.0148	0.40
I_{11}	0.0219	0.33
I_{13}	0.0138	0.21
I_{15}	0.008	0.15
I_{17}	0.0105	0.132
I_{19}	0.005	0.118
I_{21}	0.005	0.107

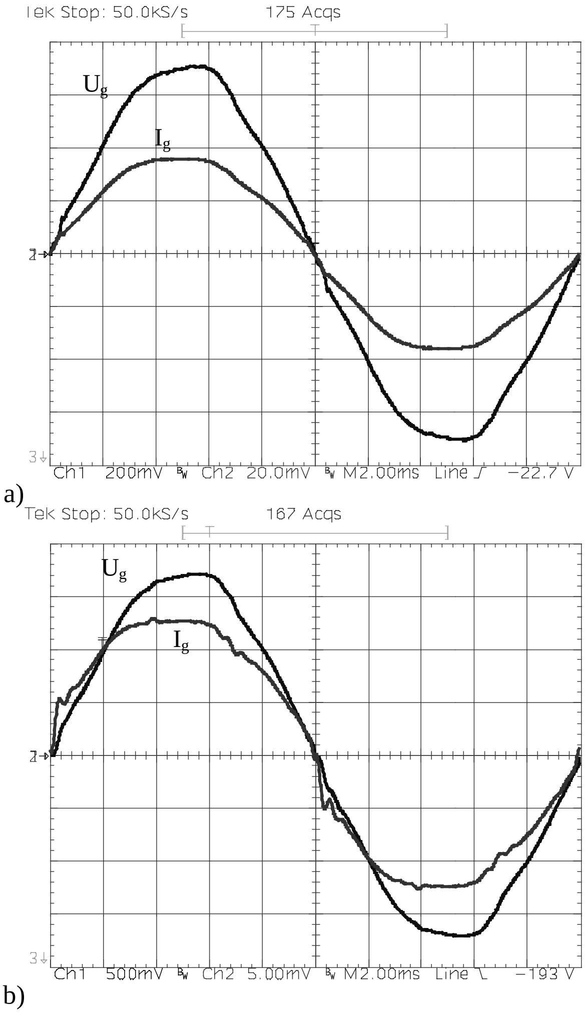


Fig. 7 - Measured input voltage and filtered input current waveforms at $U_o = 50V$, $P_o = 200W$. a) $U_g = 90V_{RMS}$, [40V/div], I_g [2A/div]; b) $U_g = 230V_{RMS}$, [100V/div], I_g [0.5A/div]

As can be seen, measured input current harmonics, reported in Table II, are well below the corresponding limits, and correspond to a total harmonic distortion (THD) for the input current slightly higher than 10%. Actually, as far as the compliance with the standards is concerned, this control approach can be employed at power levels well beyond the value recommended for the flyback topology.

Finally, to describe the control circuit operation, in Fig. 8 the main control waveforms are depicted. As can be seen, the current reference is compared to the integral signal x(t) according to the block diagram of Fig. 4. From this comparison, the switch command is generated.

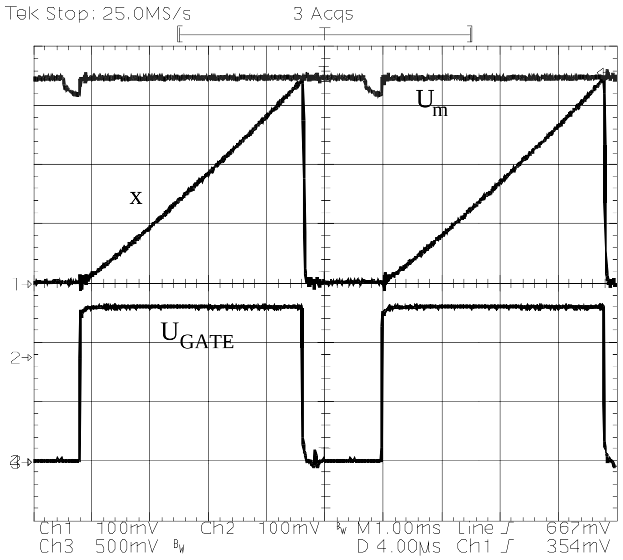


Fig. 8 - Measured control waveforms. Current reference U_m [1V/div], integral signal x [1V/div], switch command U_{GATE} [5V/div].

VI. CONCLUSIONS

This paper presented a simple implementation of the NLC control technique for high power factor flyback, Cuk or Sepic rectifiers, which makes the solution very attractive for smart-power integration, while still retaining a high power factor.

A 200W flyback rectifier with the proposed control technique was implemented with discrete components and tested to evaluate the effectiveness of the control.

The results show a good agreement with the expected performance. Further research and experimental work is in progress to test the fundamental blocks of the future smart-power IC, already available as single integrated circuits.

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