

A New Family of Zero-Current-Switching Variable Frequency dc-dc Converters

Giorgio Spiazzi*, Paolo Mattavelli**

*Dept. of Electronics and Informatics - University of Padova (Italy)

**Dept. of Electrical Engineering - University of Padova (Italy)

Via Gradenigo 6/a, 35131 Padova - ITALY

Phone: +39-049-8277525 - Fax: +39-049-8277699

E-mail: spiazzi@dei.unipd.it - mattavelli@light.dei.unipd.it

Abstract - A new family of zero-current-switching variable-frequency dc-dc converters is presented. It employs two unidirectional current switches, one diode, two small reactive components and a filter capacitor. Zero current turn-on and turn-off ensure low switching losses and smooth current waveforms result in low electromagnetic noise emission. The discontinuous operating mode and the variable switching frequency make the presented topology suitable for low-power applications or for high-power low-frequency applications where SCR's can be profitably used. Experimental results of a prototype confirm the theoretical expectations of the proposed solution.

I. INTRODUCTION

The increasing demand for high-power density dc-dc converters has led to a great effort in developing converter topologies capable of working at high switching frequency with reasonable overall efficiency [1-6]. The family of Quasi Resonant Converters (Zero-Current [1] or Zero-Voltage [2]) are valuable examples of such compact dc-dc converter structures. However, the sensitivity of the soft-switching condition on the load current and/or the input voltage greatly increases the device stresses [3], thus making them suitable for particular applications only, i.e. for those having reduced input and load variations.

This paper proposes a new family of dc-dc converters which employs two unidirectional current switches with zero current at both turn-on and turn-off. Besides the output filter capacitor, only two small reactive components are used, while output voltage control is achieved by switching frequency variation. Compared to zero current-switching quasi-resonant converter family (ZCS-QRC), the proposed solution ensures soft-switching condition independently on load or input voltage variation. This is, however, achieved using two unidirectional current switches in addition to the output diode, which practically implies that three devices are in series during the powering phase, thus making the proposed solution suitable for high voltage input. Moreover, the switching frequency is inversely proportional to the load resistance, thus making the proposed solution suited for applications with almost constant loads, as for any variable-frequency quasi-resonant converter.

The proposed family is based on a switching cell which generalizes the converter operation under different topologies. Steady-state analysis is firstly performed for the

boost converter and then extended also to the buck and buck-boost topologies. Voltage and current stresses for different topologies are also analyzed. Finally, a small signal model for the basic switching cell, suitable for control design of any of the proposed topologies, is also proposed. Experimental results of a boost converter prototype confirm the theoretical analysis and the foreseen performance.

II. TOPOLOGY DESCRIPTION

The core of the new family of ZCS-VF dc-dc converters is the switching cell depicted in Fig. 1. As we can see, it is composed by two unidirectional current switches S_1 and S_2 , one diode D and two reactive components L and C_a . The three cell ports P_1 , P_2 and P_3 are all voltage ports, i.e. only voltage generators or smoothing capacitors can be connected to. Being P_2 a voltage port, capacitor C_a can be substituted by a capacitor in parallel to diode D without modifying the cell operation. By connecting the input voltage generator and the output filter capacitor to two of the three cell ports and selecting the correct current direction, the basic converter topologies buck, boost, buck-boost are derived, as shown in Fig. 2. Since the cell operation is the same for all topologies, the boost converter is taken as an example and only its operation is described hereafter. For a better understanding of the converter behavior refers to Fig. 3, which reports the main converter waveforms during a switching period. Let us start the converter analysis at instant $t = 0$, where all switches and diodes are off, capacitor C_a is charged to $-U_o$ and inductor current is zero.

A. Charging Phase $0 < t < T_1$

During this interval, S_1 is turned on and inductor current i_L and capacitor voltage u_{C_a} follow sinusoidal waveforms according to the following equations:

$$i_L(t) = \frac{U_g + U_o}{Z_r} \sin(\omega_r t) \quad (1.a)$$

$$u_{C_a}(t) = U_g - (U_g + U_o) \cos(\omega_r t) \quad (1.b)$$

where $\omega_r = \frac{1}{\sqrt{LC_a}}$ and $Z_r = \sqrt{\frac{L}{C_a}}$ are the resonant angular frequency and the characteristic impedance respectively.

When, at instant T_1 , the auxiliary capacitor voltage u_{Ca} reaches the output voltage value, diode D starts its conduction. The duration of interval T_1 is given by:

$$u_{Ca}(T_1) = U_o \Rightarrow T_1 = \frac{1}{\omega_r} \cos^{-1} \left(-\frac{M-1}{M+1} \right) \quad (2)$$

where $M = U_o/U_g$ is the voltage conversion ratio. Since $\pi/2 < \omega_r T_1 < \pi$, from (2) the voltage conversion ratio M must be greater than one, thus revealing boost operation. The inductor current i_L at the end of interval T_1 is given by:

$$i_L(T_1) = I_1 = \frac{U_g}{Z_r} (1+M) \sin(\omega_r T_1) = \frac{2U_g}{Z_r} \sqrt{M} \quad (3)$$

B. Powering Phase $T_1 < t < T_1 + T_2$

When diode D starts conducting, the source and the inductor deliver energy to the output. The auxiliary capacitor voltage u_{Ca} remains clamped to the output voltage value U_o , while the inductor current i_L decreases linearly to zero, i.e.:

$$i_L(t) = I_1 - \frac{U_o - U_g}{L} (t - T_1) \quad (4)$$

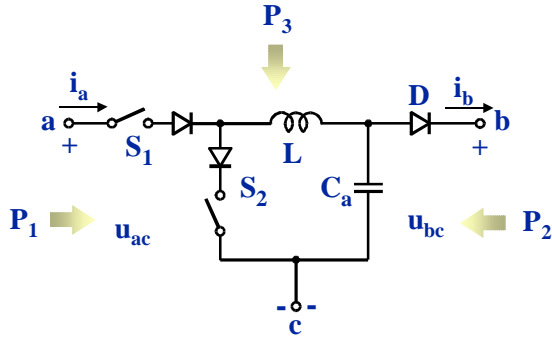


Fig. 1 - Basic switching cell of the new family of ZCS-VF dc-dc converters

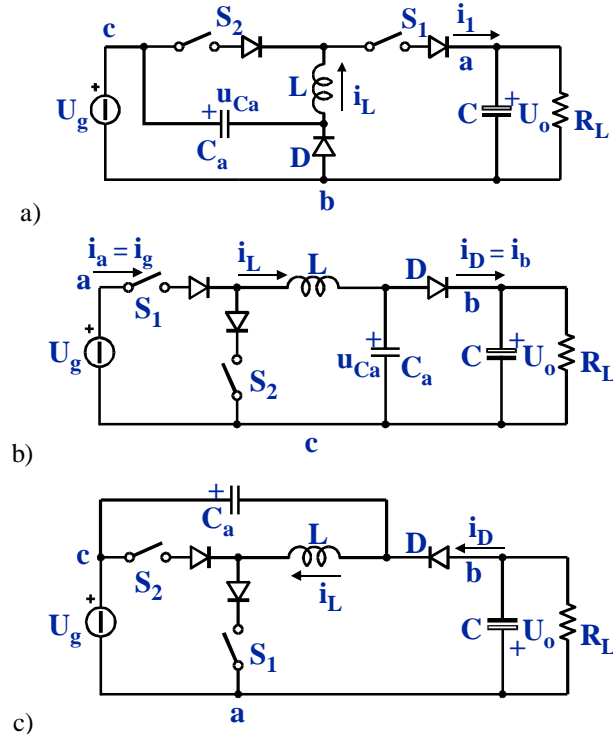


Fig. 2 - The new family of ZCS-VF dc-dc converters: a) buck; b) boost; c) buck-boost

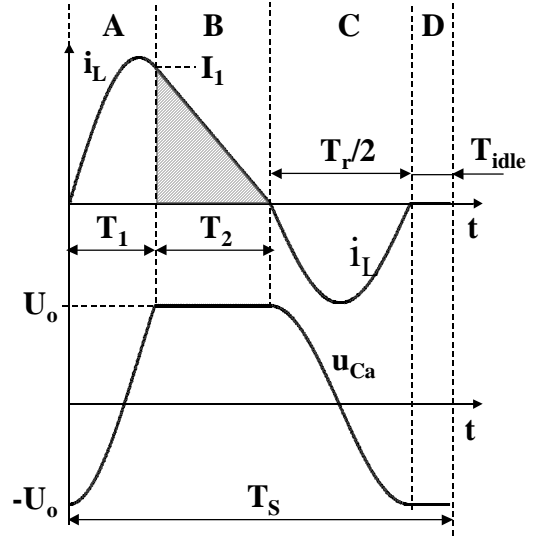


Fig. 3 - Main converter waveforms during a switching period. A) Charging Phase; B) powering phase; C) discharging phase; D) Idling phase

After a time T_2 , the inductor current i_L goes to zero, thus determining the end of subinterval T_2 . Its duration can be found by:

$$i_L(T_1 + T_2) = 0 \Rightarrow T_2 = \frac{2}{\omega_r} \frac{\sqrt{M}}{M-1} \quad (5)$$

C. Discharging Phase $T_1 + T_2 < t < T_1 + T_2 + T_r/2$

During this interval, which can be allocated anytime between the end of the powering phase and the beginning of the subsequent switching interval, switch S_2 is turned on causing a half period oscillation between L and C_a and bringing the capacitor voltage u_{Ca} from the value U_o to the value $-U_o$ (see Fig. 3). The inductor current and capacitor voltage waveforms during this interval are given by the following relations:

$$i_L(t) = -\frac{U_o}{Z_r} \sin(\omega_r (t - T_1 - T_2)) \quad (6.a)$$

$$u_{Ca}(t) = U_o \cos(\omega_r (t - T_1 - T_2)) \quad (6.b)$$

D. Idling Phase

At the end of the discharging phase, there is an idling interval T_{idle} whose duration depends on the output voltage regulator. The converter regulation is thus achieved by switching frequency variations.

The voltage conversion ratio can be derived by observing that the current delivered to the output coincides with the inductor current during the powering interval T_2 (see the shaded area highlighted in Fig. 3) which represents also the diode current. By equating the output current with the diode average current, the expression for voltage conversion ratio M as a function of the switching frequency f_s is derived as:

$$I_D = \frac{I_1 T_2}{2T_s} = I_o \Rightarrow M = 1 + 2C_a R_L f_s \quad (7.a)$$

By using normalized load resistance $R_{LN} = R_L/Z_r$ and normalized switching frequency $f_{sN} = f_s/f_r$, (7.a) can be written as:

$$M = 1 + \frac{R_{LN}}{\pi} f_{sN} \quad (7.b)$$

It is interesting to derive the maximum switching frequency, which is obtained imposing $T_{idle}=0$, as a function of voltage conversion ratio:

$$f_{sNmax} = \frac{f_{smax}}{f_r} = \frac{T_r}{\frac{T_r}{2} + T_1 + T_2} = \frac{1}{F(M)} \quad (8)$$

where, by using (2) and (5), function $F(M)$ is given by:

$$F(M) = 1 - \frac{1}{2\pi} \cos^{-1} \left(\frac{M-1}{M+1} \right) + \frac{\sqrt{M}}{\pi(M-1)} \quad (9)$$

By substituting (8) into (7.b), the maximum voltage conversion ratio M_{max} for a given load resistance is obtained solving the following implicit equation:

$$F(M_{max})(M_{max} - 1) = \frac{R_{LN}}{\pi} \quad (10)$$

Fig. 4a shows the voltage conversion ratio M as a function of the normalized switching frequency f_{sN} for different values of normalized load resistance R_{LN} . As predicted by (7.b), a linear relation exists between output and control variables, thus simplifying the control design. All diagrams terminate on the maximum switching frequency curve given by (8). Fig. 4b, instead, reports the maximum voltage conversion ratio M_{max} as a function of the normalized load resistance R_{LN} . Note that for the boost converter M_{max} varies almost linearly with the normalized load resistance R_{LN} . This implies that for high voltage conversion ratios low characteristic impedances Z_r are required.

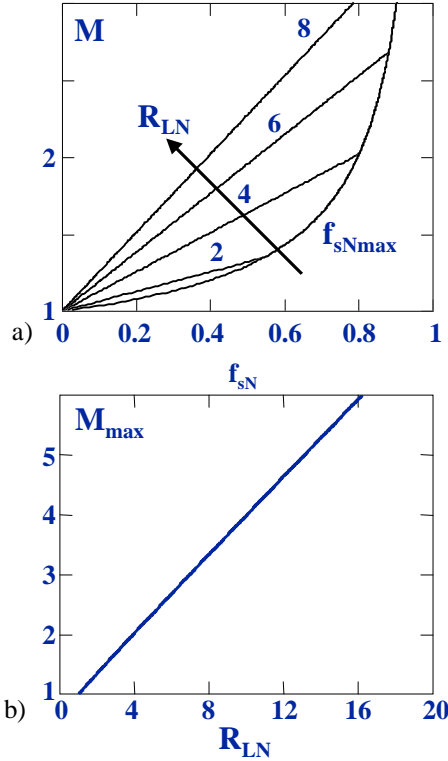


Fig. 4 – a) Voltage conversion ratio for the boost ZCS-VF converter at different normalized load resistance R_{LN} values; b) maximum voltage conversion ratio achievable as a function of the normalized load resistance

III. EXTENSION TO OTHER BASIC CONVERTER TOPOLOGIES

Voltage conversion ratio for the other two basic topologies (buck and buck-boost) can be derived with the same methodology used for the boost converter, since the main converter waveforms are the same for all topologies. However, since each topology is simply obtained by rotation of the basic switching cell of Fig. 1, it is convenient to express the fundamental equations (2), (3) and (5) in a generalized form by using the notation of voltages and currents reported in Fig. 1. Comparing Fig. 1 with Fig. 2b, the following relations hold:

$$U_{ac} = U_g, U_{bc} = U_o, I_a = I_g, I_b = I_o \quad (11)$$

Thus all equations from (1) to (6) plus (8) and (9) can be first rewritten in the generalized form using (11). Then, they can be applied to the specific topology. Moreover, the average input and output currents of the generalized switching cell can be expressed as follows:

$$I_b = \frac{I_1 T_2}{2T_s} = 2C_a f_s \frac{U_{bc} U_{ac}}{U_{bc} - U_{ac}} \quad (12)$$

$$I_a = \frac{U_{bc}}{U_{ac}} I_b = 2C_a f_s \frac{U_{bc}^2}{U_{bc} - U_{ac}} \quad (13)$$

A. Buck ZCS-VF Converter

From Fig. 2a, we note that:

$$U_{ac} = U_o - U_g, U_{bc} = -U_g, I_a = -I_o, I_b = I_g - I_o \quad (14)$$

The key equations for the buck converter result:

$$T_1 = \frac{1}{\omega_r} \cos^{-1} \left(-\frac{M}{2-M} \right) \quad (15)$$

$$I_1 = -\frac{2U_g}{Z_r} \sqrt{1-M} \quad (16)$$

$$T_2 = \frac{2}{\omega_r} \frac{\sqrt{1-M}}{M} \quad (17)$$

$$F(M) = 1 - \frac{1}{2\pi} \cos^{-1} \left(\frac{M}{2-M} \right) + \frac{\sqrt{1-M}}{\pi M} \quad (18)$$

Note that the negative value for I_1 results because of the reversed current in the buck converter respect to the directions used in the switching cell definition. The voltage conversion ratio, which is derived from $I_o = -I_a$ and (13), is given by:

$$M^2 = \frac{R_{LN}}{\pi} f_{sN} \quad (19)$$

The plot of M versus the normalized switching frequency f_{sN} for different values of normalized load resistance R_{LN} is shown in Fig. 5. Again, all curves terminate on the maximum switching frequency curve given by (8) and (18). It is interesting to note that, since the voltage conversion ratio is proportional to the square root of the load resistance, the buck topology achieves an “automatic” unity power factor when used as ac/dc rectifiers, so that the input current is proportional to input voltage without any frequency modulation [7].

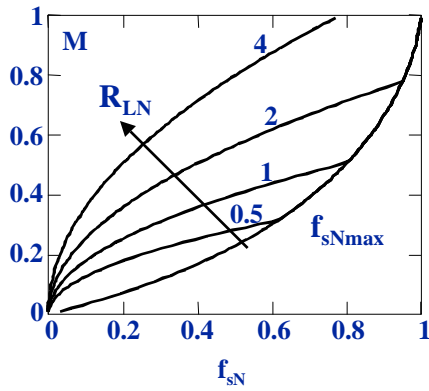


Fig. 5 - Voltage conversion ratio for the buck ZCS-VF converter at different normalized load resistance R_{LN} values

B. Buck-Boost ZCS-VF Converter

From Fig. 2c, we note that:

$$U_{ac} = -U_g, U_{bc} = -U_o - U_g, I_a = -I_g - I_o, I_b = -I_o \quad (20)$$

Thus, the fundamental relations for the buck-boost converter are derived as:

$$T_1 = \frac{1}{\omega_r} \cos^{-1} \left(-\frac{M}{2+M} \right) \quad (21)$$

$$I_1 = -\frac{2U_g}{Z_r} \sqrt{1+M} \quad (22)$$

$$T_2 = \frac{2}{\omega_r} \frac{\sqrt{1+M}}{M} \quad (23)$$

$$F(M) = 1 - \frac{1}{2\pi} \cos^{-1} \left(\frac{M}{2+M} \right) + \frac{\sqrt{1+M}}{\pi M} \quad (24)$$

Also for this topology the current direction is reversed, thus justifying the minus sign in (22). The voltage conversion ratio, which is derived from $I_o = -I_b$ and (12), is given by:

$$\frac{M^2}{1+M} = \frac{R_{LN}}{\pi} f_{sN} \quad (25)$$

The control curves, i.e the plot of M versus the normalized switching frequency f_{sN} for different value of normalized load resistance R_{LN} , are reported in Fig. 6 together with the maximum switching frequency curve given by (8) and (24). Except for very low values of the normalized switching frequency, the voltage conversion ratio varies almost linearly with the switching frequency.

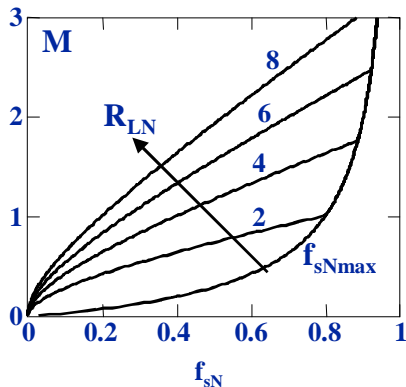


Fig. 6 - Voltage conversion ratio for the buck-boost ZCS-VF converter at different normalized load resistance R_{LN} values

It is interesting to observe that the resonant capacitor C_a can have different connections without changing the converter behavior. For example, as far as the buck-boost converter is concerned, if the connection of C_a in the point **c** is moved to point **a**, the resulting topology becomes the same as that of the boost one with the exception of the output diode, which is inverted, and with the swap of the driving signals between switches S_1 and S_2 .

IV. DEVICE STRESSES

This section describes device voltage and current stresses of the proposed ZCS-VF converter topologies. From the analysis of the boost converter reported in section II, we can observe that:

- the maximum S_1 voltage stress occurs at the end of the discharging phase for the switch and at the end of the powering phase for the series blocking diode;
- the maximum S_2 voltage stress occurs at the end of the powering phase for the switch and at the end of the discharging phase for the series blocking diode;
- the maximum D voltage stress occurs at the end of the discharging phase;
- the switch current stresses are proportional to the corresponding switch voltage stresses (through the characteristic impedance of the resonant tank);
- the diode current stress is given by the inductor current value at the end of the charging phase (current I_1).

From the above information, voltage and current stresses for all topologies has been derived and summarized in Table I. Note that current stresses are proportional to the inverse of Z_r . This means that high voltage conversion ratios, which require low characteristic impedances Z_r (Fig. 4b), imply high switch current stresses.

Unfortunately, the calculated voltage stresses are only theoretical values, since the parasitic oscillations, that occur in a real converter between the resonant inductance L and the switch parasitic capacitance during the idle phase, increase the actual voltage stress and require a proper damping snubber.

TABLE I
DEVICE VOLTAGE AND CURRENT STRESSES

	Topology	Voltage Stress		Current Stress
		\hat{U}_S	\hat{U}_D	
S_1	Buck	$2 \cdot U_g - U_o$	U_o	$(2 \cdot U_g - U_o) / Z_r$
	Boost	$U_g + U_o$	$U_o - U_g$	$(U_g + U_o) / Z_r$
	Buck-boost	$2 \cdot U_g + U_o$	U_o	$(2 \cdot U_g + U_o) / Z_r$
S_2	Buck	U_g	U_g	U_g / Z_r
	Boost	U_o	U_o	U_o / Z_r
	Buck-boost	$U_g + U_o$	$U_g + U_o$	$(U_g + U_o) / Z_r$
D	Buck	$2 \cdot U_g$		$ I_1 $ (see (16))
	Boost	$2 \cdot U_o$		$ I_1 $ (see (3))
	Buck-boost	$2 \cdot (U_g + U_o)$		$ I_1 $ (see (22))

V. SMALL SIGNAL MODEL

Control design for the proposed ZCS-VF converter family requires the knowledge of its dynamic behavior. To this purpose, a small-signal model is here derived starting from the general switching cell of Fig. 1. Perturbing the input and output average currents (12)-(13) under small-signal assumptions, the following equations have been derived:

$$\hat{i}_b = \frac{\partial I_b}{\partial U_{bc}} \hat{u}_{bc} + \frac{\partial I_b}{\partial f_s} \hat{f}_s + \frac{\partial I_b}{\partial U_{ac}} \hat{u}_{ac} \quad (26.a)$$

$$= -g_o \hat{u}_{bc} + k_o \hat{f}_s + g_f \hat{u}_{ac}$$

$$\hat{i}_a = \frac{\partial I_a}{\partial U_{ac}} \hat{u}_{ac} + \frac{\partial I_a}{\partial f_s} \hat{f}_s + \frac{\partial I_a}{\partial U_{bc}} \hat{u}_{bc} \quad (26.b)$$

$$= g_i \hat{u}_{ac} + k_i \hat{f}_s + g_r \hat{u}_{bc}$$

which correspond to the circuit model shown in Fig. 7.

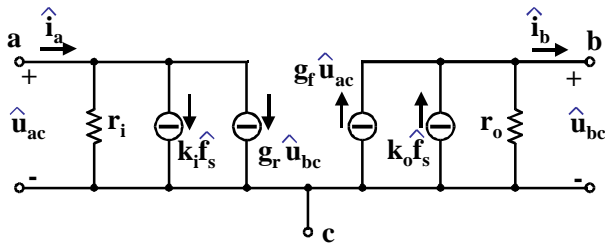


Fig. 7 – Small-signal model of the basic switching cell

The parameter expressions of model (26.a)-(26.b) are given by:

$$g_o = \frac{1}{r_o} = -\frac{\partial I_b}{\partial U_{bc}} = 2C_a f_s \left(\frac{U_{ac}}{U_{bc} - U_{ac}} \right)^2 \quad (27.a)$$

$$g_f = \frac{\partial I_b}{\partial U_{ac}} = 2C_a f_s \left(\frac{U_{bc}}{U_{bc} - U_{ac}} \right)^2 \quad (27.b)$$

$$k_o = \frac{\partial I_b}{\partial f_s} = 2C_a \left(\frac{U_{ac} U_{bc}}{U_{bc} - U_{ac}} \right) \quad (27.c)$$

$$g_i = \frac{1}{r_i} = \frac{\partial I_a}{\partial U_{ac}} = 2C_a f_s \left(\frac{U_{bc}}{U_{bc} - U_{ac}} \right)^2 \quad (28.a)$$

$$g_r = \frac{\partial I_a}{\partial U_{bc}} = 2C_a f_s U_{bc} \frac{U_{bc} - 2U_{ac}}{(U_{bc} - U_{ac})^2} \quad (28.b)$$

$$k_i = \frac{\partial I_a}{\partial f_s} = 2C_a \left(\frac{U_{bc}^2}{U_{bc} - U_{ac}} \right) \quad (28.c)$$

These relations can than be applied to any of the basic topologies. For example, by applying the small-signal model to the boost converter of Fig. 2b, the parameters reported in Table II and the equivalent circuit of the output stage of Fig. 8 have been obtained. From Fig. 8, the transfer function between the control variable f_s and the output voltage has been derived as follows:

$$G_c(s) = \frac{\hat{u}_o(s)}{\hat{f}(s)} = k_o \frac{R_p}{1 + sR_p C} \quad (29)$$

where $R_p = \frac{r_o R_L}{r_o + R_L} = R_L \frac{M-1}{M}$. Using the expressions reported in Table II we have obtained:

$$G_c(s) = \frac{\hat{u}_o(s)}{\hat{f}(s)} = \frac{2C_a R_L U_g}{1 + sR_L C \frac{M-1}{M}} \quad (31)$$

which is a simple first order transfer function, as usually obtained in converters operating in discontinuous mode.

TABLE II
SMALL-SIGNAL MODEL PARAMETERS OF THE BOOST CONVERTER

Input section	Output section
$g_i = \frac{1}{R_L} \frac{M^2}{M-1}$	$g_o = \frac{1}{R_L} \frac{1}{M-1}$
$g_f = \frac{M}{R_L} \frac{M-2}{M-1}$	$g_r = \frac{1}{R_L} \frac{M^2}{M-1}$
$k_i = 2C_a U_g \frac{M^2}{M-1}$	$k_o = 2C_a U_g \frac{M}{M-1}$

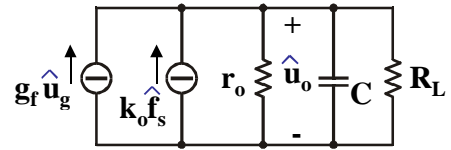


Fig. 8 – Output section of the boost small-signal model

V. DESIGN OUTLINE

As an example, let us consider boost ZCS-VF converter described in the section II with the following specifications: minimum input voltage (U_{gmin}), maximum input voltage (U_{gmax}), output voltage (U_o), minimum load resistance (R_{Lmin}), and maximum switching frequency (f_{smax}).

By using the specified maximum voltage conversion ratio and the minimum load resistance, the characteristic impedance Z_r is calculated from (10). Then, from (7.b), the resonance frequency f_r is found at minimum input voltage and load resistance. This choice allows to design the converter so that at the minimum input voltage and at the maximum output power it works at the limit between discontinuous and continuous mode. A small margin is needed in order to cope with the converter losses and in order to ensure enough dynamic capability during step load variations. From the definition of $\omega_r = 2\pi f_r$ and Z_r , the values of the resonant components L and C_a are easily derived. Finally, the output filter capacitor value is calculated in the usual manner by imposing the desired output voltage ripple at the switching frequency.

VI. EXPERIMENTAL RESULTS

An experimental prototype was built and tested in order to verify the theoretical analysis. The converter specifications were:

minimum input voltage:	$U_{gmin} = 24V$
maximum input voltage:	$U_{gmax} = 36V$
output voltage:	$U_o = 48V$
minimum load resistance:	$R_{Lmin} = 50\Omega$
maximum switching frequency:	$f_{smax} = 125kHz$

The major converter parameters used in the prototype are: $L=7.18\mu\text{H}$, $C_a =141\text{nF}$, $C=100\mu\text{F}$. These values has been obtained using the procedure outlined in section V; however, due to the low input voltage, a low efficiency is expected, so that a big safety margin was taken in order to meet the desired specifications.

Fig. 9 shows the resonant inductor current i_L , the resonant capacitor voltage u_{Cr} and S_2 drain-source voltage during a switching period for the minimum input voltage and the nominal output power. Note that, the discharging phase when the inductor current is negative, was allocated just before the charging phase: this allowed to remove the series blocking diode of S_2 , thus reducing the power loss during the discharging phase. The experimental waveforms agree quite well with the predicted ones except for the parasitic oscillations, already mentioned, during the idle phase: a R_d - C_d snubber was used ($R_d = 120\Omega$, $C_d = 2\text{nF}$) in parallel to switch S_2 in order to limit its voltage stress and damp the oscillations (the snubber dissipation is below 1W).

In Fig. 10 is reported the voltage conversion ratio M as a function of the switching frequency for three different load resistances. Note that the expected linear behavior is almost satisfied.

VII. CONCLUSIONS

In this paper a new family of zero-current-switching variable-frequency dc-dc converters are presented. The zero current turn-on and turn-off reduce both switching losses and the electromagnetic noise emission. Compared to zero current-switching quasi-resonant converter family (ZCS-QRC), the proposed solution ensures soft-switching condition independently on load or input voltage variation at the expense of a large number of switches. The discontinuous operating mode and the variable switching frequency make the presented topology suitable for low-power applications or for high-power low-frequency applications where SCR's can be profitably used. Experimental results of a prototype based on the boost ZCS-VF topology confirm the theoretical expectations.

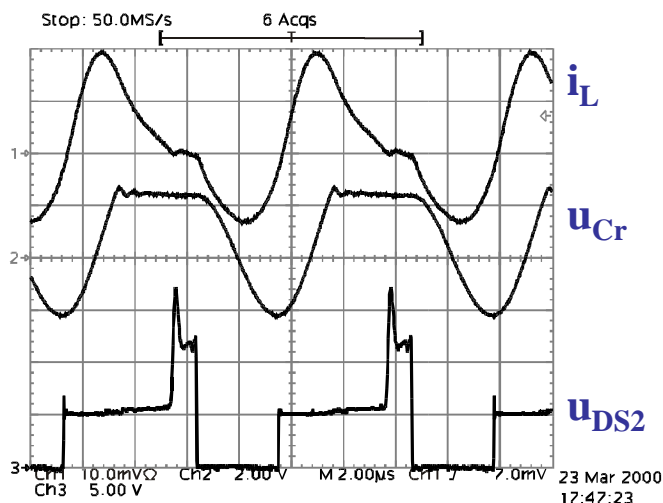


Fig. 9 – Main converter waveforms in a switching period. From top to bottom: inductor current i_L (5A/div), resonant capacitor voltage u_{Cr} (40V/div), drain-source voltage of switch S_2 (20V/div)

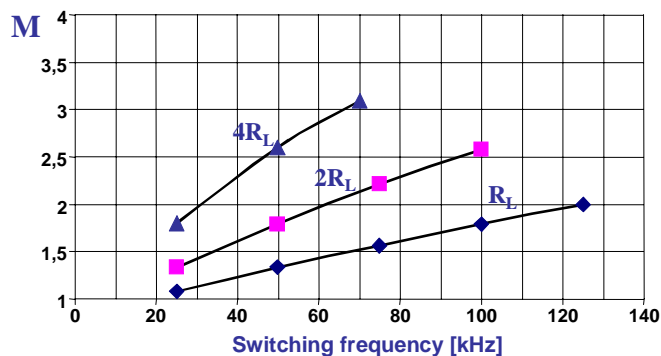


Fig. 10 – Measured voltage conversion ratio as a function of the switching frequency for three different load resistances

ACKNOWLEDGMENTS

The authors thank Mr. Antonio Trevisan for his contribution in the experimental activity.

REFERENCES

1. K. H. Liu, R. Oruganti, F. C. Lee, "Resonant Switches - Topologies and Characteristics," IEEE Power Electronics Specialists Conf. Proc., June 1985, pp.106-116.
2. K. H. Liu, R. Oruganti, F. C. Lee, "Zero-Voltage Switching Technique in DC/DC Converters," IEEE Power Electronics Specialists Conf. Proc., 1986, pp.58-70.
3. A. W. Lofti, V. Volperian, F. C. Lee, "Comparison of stresses in Quasi-resonant and Pulse-Width-Modulated Converters," IEEE Power Electronics Specialists Conf. Proc., April 1988, pp.591-598.
4. T. Zheng, D.Y. Chen, F.C. Lee, "Variations of quasi-resonant dc/dc converter topologies", IEEE PESC Conf. Proc., 1997
5. R. Oruganti and F.C. Lee "Resonant Power Processors, Part 1: State Plane Analysis", IEEE Trans on Industry Applications, Nov./Dec. 1985.
6. R. Oruganti and F.C. Lee "Resonant Power Processors, Part 2: Methods of Control ", IEEE Trans on Industry Applications, Nov./Dec. 1985.
7. S.D. Freeland, *Input-current shaping for single-phase ac/dc power converters*, Ph. Thesis, part II, Caltech, 1988.