A Low-Loss High-Power-Factor Flyback Rectifier Suitable for Smart Power Integration

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Abstract. **A low-loss, high-power-factor flyback rectifier is presented, which is designed as a possible application for a new type of *smart power* integrated circuit. This is going to be manufactured by ST Microelectronics using the VIPower© M3 technology and will include on the same silicon chip both control circuitry and an *emitter switching* power device. In order to avoid dangerous interactions between power and control part of the integrated circuit, it is necessary to control the rate of change of the power device voltage at turn-off. Accordingly, a lossless passive snubber was added to the conventional converter topology. The snubber also limits the voltage spikes across the power device, due to the transformer leakage inductance, and reduces the electromagnetic noise generation.**

A modified non-linear carrier control is considered which, thanks to the integration of the switch current signal, ensures high power factor and inherent noise immunity together with a simple control implementation (no need of input voltage sensing, multiplier and current error amplifier).

A 200 W converter prototype was tested in order to evaluate the achievable performance.

I. Introduction

Smart power integration, i.e. the integration on a single chip of a power switch and a given control circuit, may represent, especially for low power applications, an effective way of reducing cost and size of a power converter, while increasing its reliability and power density. However, the coexistence in a single integrated circuit (IC) of power and signal circuitry poses several design problems. An important one is the minimisation of the interaction between the two parts of the circuit, that can adversely affect the overall IC reliability. In some cases, its solution may require a careful control of current and voltage waveforms across the power device and may constrain the selection of the converter topology and its design.

This paper discusses the design of a high-power-factor flyback rectifier, which is meant to be a possible application for a new type of smart-power IC's. These new chips are going to be manufactured by ST Microelectronics in the VIPower© M3 technology, and are aimed to allow a cheap and rapid development of low-power high-power-factor rectifiers.

As mentioned above, this type of integration technology requires the voltage rate of change across the power device at turn off to be kept below a known maximum level. This is necessary to avoid the injection of high currents, through parasitic capacitances, into the control and driver parts of the integrated circuit [1-3], which could cause fatal control failures.

As a consequence, the conventional flyback topology has been modified adding a lossless passive snubber [4-7], which helps to control the switch dv/dt at turn-off as well as to reduce the switching losses, thus improving the converter's efficiency. Besides, by adopting this solution, the transformer leakage inductance is exploited to reduce the switch di/dt at turn-on and its energy is recovered to the input through the snubber itself.

As far as the control strategy is concerned, a modified non-linear carrier control [8-11] is considered, which ensures high power factor and inherent noise immunity, thanks to the integration of the switch current signal. Moreover, the control complexity is reduced, as compared to standard approaches (no need of input voltage sensing, multiplier and current error amplifier), which makes it particularly suitable, in terms of ruggedness and simplicity, for smart power integration [11].

Experimental results, referring to a 200 W prototype where a VIPower emitter switching device is used as the switch, are reported and discussed.

II. Converter Operation

The proposed low-loss flyback rectifier is shown in Fig. 1. It employs a lossless passive snubber which is made up of the snubber capacitor C_{sn}, inductance L_{sn}, and diodes D_1-D_2-D_3. In particular, diode D_3 is initially considered to simplify the converter analysis. However, as it will be explained in part H of this section, it can be removed with a careful snubber design, improving the converter efficiency. The transformer leakage inductance is represented by L_d. The input capacitor C_{in} allows the use of slow diodes in the rectifier bridge and keeps the parasitic inductance in the loop containing the emitter switching device and the snubber capacitor at minimum. In the following converter operation description, a constant input voltage U_g is considered due to the high ratio between switching and line frequencies. The main converter waveforms during a switching period are reported in Fig. 2, while the different circuit subtopologies are shown in Fig. 3. The converter analysis starts at the generic instant T_0, when the switch is turned on. In order to keep the notation simple, the beginning of each subinterval is considered as time "zero". Moreover, the approximation $L_d << L_\mu$ is used.

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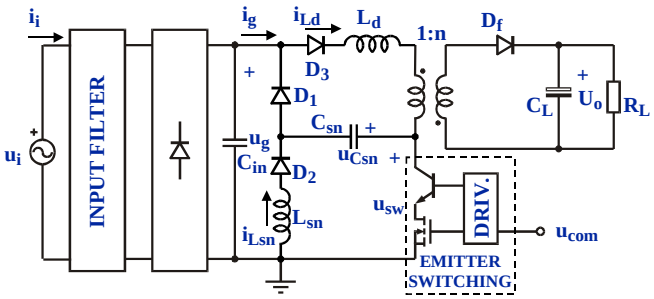


Fig. 1 - Flyback rectifier with the lossless passive snubber

A. Interval [T_0, T_1]

At the instant T_0 the switch is turned on, while diode D_f is still on. The voltage across the leakage inductance equals the sum of the input voltage and of the reflected output voltage (see Fig. 3a) and causes a linear increase of current i_{Ld} until this reaches the value of the magnetising current (instant T_1):

$$i_{Ld}(t) = \frac{U_g + U_{op}}{L_d} t, \qquad (1)$$

$$T_{01} = \frac{L_d I_{\mu v}}{U_g + U_{op}}, \qquad (2)$$

where $T_{01} = T_1 - T_0$ is the duration of this subinterval, $U_{op} = U_o/n$ is the output voltage reflected to the primary side, and $I_{\mu v}$ is the magnetising current valley value. Note that, being interval T_{01} very small as compared to the switching period, i_{Ld} can be set equal to the magnetising current value at the end of the switch off-time $I_{\mu v}$.

The turn-on of the switch also starts a resonance between C_{sn} and L_{sn} (see Fig. 3b), whose voltage and current are given by:

$$u_{Csn}(t) = U_1 \cos(\omega_{sn} t), \qquad (3.a)$$

$$i_{Lsn}(t) = \frac{U_1}{Z_{sn}} \sin(\omega_{sn} t), \qquad (3.b)$$

where U_1 is the initial voltage across the snubber capacitor C_{sn}, while $\omega_{sn} = \frac{1}{\sqrt{L_{sn} C_{sn}}}$ and $Z_{sn} = \sqrt{\frac{L_{sn}}{C_{sn}}}$ are respectively the resonance angular frequency and the snubber characteristic impedance.

B. Interval [T_1,T_2]

During this interval energy is stored in the transformer, as in the normal flyback operation, while the resonance between C_{sn} and L_{sn} continues until the capacitor voltage u_{Csn} reaches the magnitude of the input voltage (in the hypothesis that the initial capacitor voltage U_1 is higher than the input voltage U_g). The magnetising current is given by (see Fig 3c):

$$i_{Ld}(t) = i_\mu(t) = I_{\mu v} + \frac{U_g}{L_d + L_\mu} t \approx I_{\mu v} + \frac{U_g}{L_\mu} t, \qquad (4)$$

while (3) holds also in this subinterval. The duration of this subinterval is given by:

$$T_{12} = \frac{1}{\omega_{sn}} \cos^{-1}\left(-\frac{U_g}{U_1}\right) - T_{01}, \qquad (5)$$

while the value of current i_{Lsn} at instant T_2 is given by:

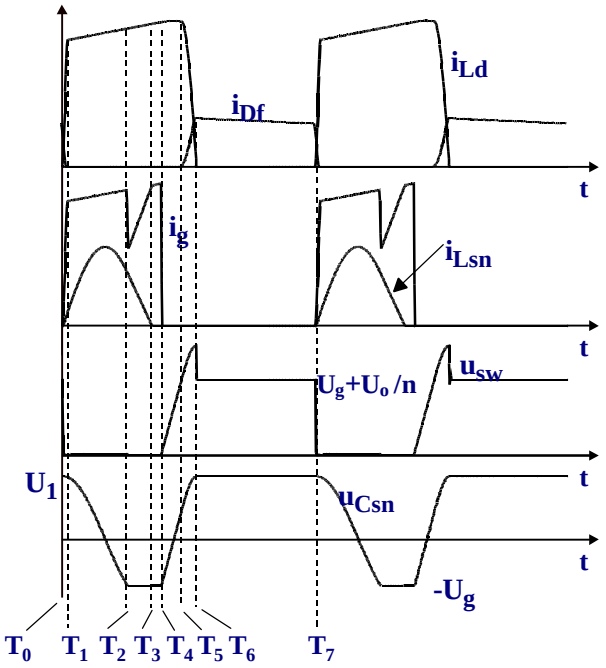


Fig. 2 - Main converter waveforms in a switching period

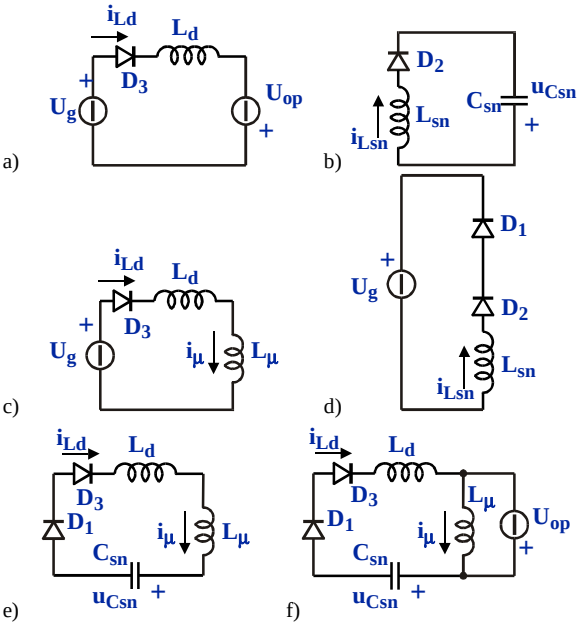


Fig. 3 – Topological states of the proposed converter in a switching period: a) interval T_{01}; b) interval T_{01}+T_{12}; c) interval T_{12}+T_{23}+T_{34}; d) interval T_{23}; e) interval T_{45}; f) interval T_{56}

$$i_{Lsn}(T_{02}) = \frac{U_1}{Z_{sn}} \sin(\omega_{sn} T_{02}) = \frac{U_1}{Z_{sn}} \sqrt{1 - \left(\frac{U_g}{U_1}\right)^2}. \qquad (6)$$

C. Interval [T_2, T_3]

At T_2, diode D_1 turns on clamping the voltage across capacitor C_{sn} to the value $-U_g$ and allowing the discharge of the auxiliary inductor L_{sn} to the input (see Fig 3d). This interval ends in T_3 when i_{Lsn} goes to zero.

$$i_{Lsn}(t) = i_{Lsn}(T_{02}) - \frac{U_g}{L_{sn}} t. \qquad (7)$$

Note that, during this interval, the input current i_g equals the

difference between i_μ and i_{Lsn}. The subinterval duration is given by:

$$T_{23} = \frac{L_{sn} i_{Lsn}(T_{02})}{U_g}. \quad (8)$$

D. Interval [T_3, T_4]

This interval completes the switch on-phase (the snubber is inactive) and its duration is given by:

$$T_{34} = T_{on} - T_{01} - T_{12} - T_{23}. \quad (9)$$

E. Interval[T_4, T_5]

At instant T_4, the switch is turned off and the total transformer inductance resonates with the snubber capacitor C_{sn} rising its voltage in an almost linear way (a constant magnetising current value $I_{\mu p}$ is assumed in this interval), while diode D_f is still off (see Fig. 3e). Voltage waveforms and interval duration are given by:

$$u_{Csn}(t) = -U_g + \frac{I_{\mu p}}{C_{sn}} t, \quad (10)$$

$$u_{SW}(t) = U_g + u_{Csn}(t) = \frac{I_{\mu p}}{C_{sn}} t, \quad (11)$$

$$T_{45} = \frac{C_{sn}}{I_{\mu p}}\left(\left(1 + \frac{L_d}{L_\mu}\right)U_{op} + U_g\right) \approx \frac{C_{sn}}{I_{\mu p}}\left(U_{op} + U_g\right). \quad (12)$$

Note that the voltage across the switch rises with a slope which is controlled by the snubber capacitor value.

F. Interval [T_5, T_6]

The previous subinterval ends at instant T_5 when diode D_f is turned on, causing the magnetising current to discharge to the output while the transformer leakage inductance L_d continues to resonate with C_{sn} (through D_1 and D_3) until its current goes to zero (see Fig. 3f). At the end of this interval, voltage u_{Csn} is equal to U_1 and the voltage across the switch reaches the maximum value U_g+U_1. The converter waveforms are expressed by the following equations:

$$i_\mu(t) = I_{\mu p} - \frac{U_{op}}{L_\mu} t, \quad (13)$$

$$i_{Ld}(t) = I_{\mu p} \cos(\omega_d t), \quad (14.a)$$

$$u_{Csn}(t) = U_{op} + Z_d I_{\mu p} \sin(\omega_d t), \quad (14.b)$$

where $\omega_d = \frac{1}{\sqrt{L_d C_{sn}}}$ and $Z_d = \sqrt{\frac{L_d}{C_{sn}}}$;

$$i_{Df}(t) = \frac{i_\mu(t) - i_{Ld}(t)}{n}. \quad (15)$$

The interval length is a quarter of the resonant period, i.e.

$$T_{56} = \frac{\pi}{2\omega_d} \quad (16)$$

and the voltage across C_{sn} is

$$u_{Csn}(T_{56}) = U_1 = U_{op} + Z_d I_{\mu p} \sin(\omega_d T_{56}) = U_{op} + Z_d I_{\mu p}. \quad (17)$$

Consequently, the *soft-switching condition* is given by:

$$U_1 > U_g \quad \Rightarrow \quad U_{op} + Z_d I_{\mu p} > U_g. \quad (18)$$

G. Interval [T_6, T_7]

During this period, the transformer energy is delivered to the output until the beginning of the next switching period.

$$T_{67} = T_S - T_{on} - T_{45} - T_{56}. \quad (19)$$

H. Diode D_3

Diode D_3 prevents a current inversion through L_d, C_{in}, L_{sn}, D_2, C_{sn} and the transformer primary winding that, in general, could occur at the end of interval [T_5, T_6]. Anyway, being connected in series to the power switch, diode D_3 significantly worsens the converter's efficiency. Therefore, it is important to verify if it is possible to eliminate it without adversely affecting the snubber behaviour. The discharge of capacitor C_{sn} takes place only if diode D_2 is turned on, which implies:

$$Z_d I_{\mu p} > U_g \quad (20)$$

The inequality (20) depends on the transformer design and, in general, could be satisfied in certain operating conditions. If this happens, the voltage across C_{sn} will tend to sinusoidally oscillate around the U_g+U_{op} value. The oscillation will stop after half a resonant period, i.e. when diode D_2 again turns off, provided that enough time during interval [T_6, T_7] is available. A fundamental point is that the minimum voltage reached by C_{sn} during the oscillation must be greater than U_g, in order to maintain the soft-switching condition (18). This implies the following inequality:

$$Z_d I_{\mu p} < U_g + U_{op} \quad (21)$$

If the transformer design is such that (21) is satisfied, the presence of diode D_3 is not necessary. It is worth noting that, in practice, the oscillation of C_{sn} voltage will always be damped to some extent, making condition (21) slightly conservative. D_3 was not used in our prototype. With our design, the soft-switching condition is, in fact, always maintained, as the experimental results will illustrate.

In conclusion, the use of the lossless snubber gives the following advantages:

- low switching losses at turn-off. In fact, provided that condition (18) holds, then the switch turns off at zero voltage (see Fig. 2 at instant T_4);
- reduced di/dt in the rectifier diode D_f at turn-off, depending on the value of the leakage inductor L_d (in any case less recovery problems);
- limited dv/dt across the switch at turn-off, as stated by (11) (less interaction with the integrated control circuit in the smart power chip);
- recovery of the leakage inductor energy;
- predictable and controlled switch voltage stress.

The disadvantages are:

- increased switch current RMS value (the resonant current i_{Lsn} during interval T_0-T_2 adds to the magnetising inductor current in the switch), with the consequent increase of the conduction losses;
- limitation of the minimum switch on-time in order to allow the discharge of the passive snubber;
- increased cost (more fast diodes and a snubber inductor needed).

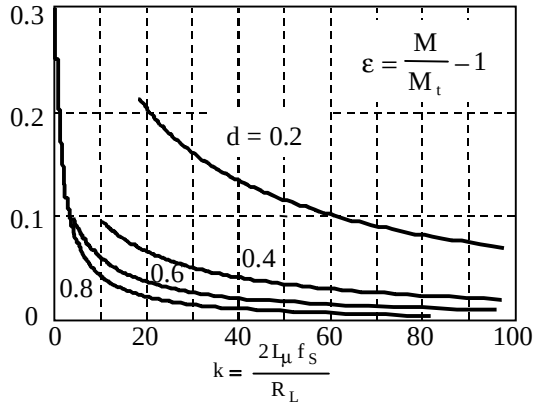


Fig. 4 – Voltage conversion ratio relative deviation ε as a function of parameter $k=2L_\mu f_S/R_L$ for different duty-cycle values.

In the following sections the operation of the converter as a rectifier is investigated.

III. DC Analysis

As we can see from the previous analysis, the use of the lossless passive snubber changes to some extent the converter behaviour, as compared to the standard flyback operation. In this section we want to quantify this deviation by finding the converter voltage conversion ratio $M = U_{op}/U_g$ as a function of the duty-cycle and of the operating point. The details of such derivation are reported in the Appendix; here, we simply show the result in Fig. 4, which reports the voltage conversion ratio relative deviation $\varepsilon = M/M_t-1$ as a function of parameter $k = 2L_\mu f_S/R_L$ for different values of the duty-cycle ($M_t = d/(1-d)$ is the theoretical voltage conversion ratio for a flyback converter working in CCM). The parameter values used to derive these curves are listed in Table I, at the beginning of section VI. As we can see, the actual voltage conversion ratio is always higher than the theoretical one, but the difference becomes appreciable only at operating points close to the discontinuous conduction mode (DCM). This consideration allows us to use the much simpler relations of the standard flyback converter, derived for the operation as a high power factor rectifier, for the design of the power stage.

IV. Power Stage Design

A. Loss-less snubber design

The design of the lossless snubber requires the choice of the snubber capacitor and inductor values as well as the selection of the auxiliary diodes D_1 and D_2. As far as capacitor C_{sn} value is concerned, its main objective is to set the maximum voltage rate of change across the emitter switching at turn-off, i.e.:

$$\max \frac{du_{SW}}{dt} = \frac{i_{\mu p}\left(\frac{\pi}{2}\right)}{C_{sn}} \qquad (22)$$

By imposing a maximum voltage rate of change equal to 1.5V/ns at nominal power and minimum input voltage, the value of C_{sn} results of 4 nF. In practice, using this capacitor value, a slightly lower voltage rate of change has been achieved, basically because of parasitic capacitances (e.g. switch output capacitance, transformer winding capacitance etc.) that have been neglected in the analysis.

For the selection of the inductor L_{sn} value, we have to take into account both the increased switch current stress as well as the soft switching condition. Assuming the maximum switch current during interval T_{02} occurs at the peak of current i_{Lsn} (this is not strictly true being the switch current made up of the sum of a linearly varying magnetising current and a sinusoidally varying snubber current), we can impose the following condition evaluated for $\theta = \pi/2$ (θ being the line angle i.e. $\omega_{line}\cdot t$):

$$i_{\mu v}(\theta) + \frac{u_g(\theta)}{L_\mu}\frac{\pi}{2\omega_{sn}} + \frac{u_1(\theta)}{Z_{sn}} \le i_{\mu p}(\theta). \qquad (23)$$

In this way, the snubber action does not increase the switch current stress as compared to that of the standard flyback. In (23) L_{sn} appears as argument of both ω_{sn} and Z_{sn}.

On the other hand, the soft switching condition requires that interval T_{02} must be lower than the minimum switch on-time in order to allow a complete inversion of the voltage across the snubber capacitor C_{sn}. In this case, the worst condition occurs at the maximum input voltage, for $\theta = \pi/2$:

$$\frac{1}{\omega_{sn}}\cos^{-1}\left(-\frac{u_g(\theta)}{u_1(\theta)}\right) \le T_{on\_min} \qquad (24)$$

Other criteria, e.g. the inductor volume, could be taken into account to guide the snubber design. These could determine a different choice for the inductor value as compared to that calculated from (23) and (24).

B. Transformer design

The transformer is another key point of the converter design. In our prototype we had the necessity of limiting the primary side current to less than 6 A, not to exceed the power switch current capability. This fact compelled to accept a significant voltage stress for the device (1000 V @ $U_i = 230\ V_{RMS}$), and led to the determination of the transformer turns ratio (0.165). Of course, the value of the magnetising inductance was also selected to be quite high (1 mH), in order to limit the current ripple and so the switch peak current.

V. Control Scheme

A high power factor rectifier requires a control approach which allows to draw an input current as much proportional to the input voltage as possible. On the other hand, a reliable smart power integration requires the choice of a simple and robust control circuit as much immune to the switching noise as possible. For these reasons, a modified non-linear carrier control [8-10] is proposed here, which allows a simple implementation without excessively worsening the input power factor. All the details concerning the control implementation can be found in [11]. Actually, because of the snubber presence, in the converter we are analysing the switch current waveform in a modulation period is different from the typical one, considered in [11]. Nevertheless, the PFC operation of the circuit is not significantly affected, and the resulting line current maintains an almost sinusoidal waveform.

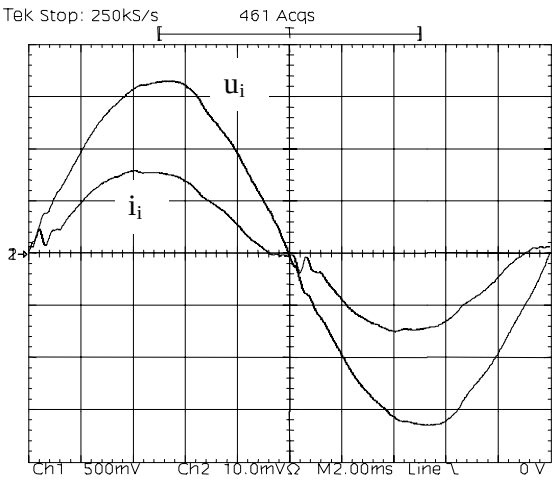


Fig. 5 - Input voltage [100V/div] and filtered line current [1A/div] waveforms (U_i = 230V_{RMS}; P_o = 200 W).

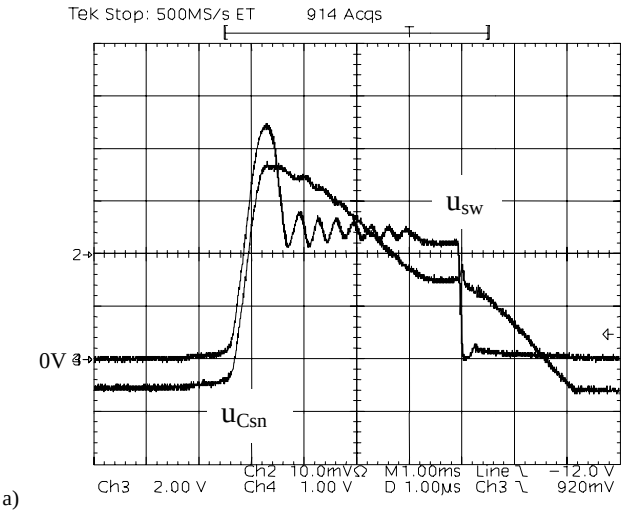
VI. Experimental Results

A 200 W flyback rectifier, whose parameters are listed in Table I, was built and tested. The power device used in the prototype is an emitter-switching in VIPower© M3 technology, the same device which will be integrated in the final smart power circuit. A Magnetics Kool-Mμ© core of the 77439-A7 type was used to build the transformer (L_d in Fig. 1 represents its leakage inductance); the snubber inductor was instead built using a 77930-A7 core from the same manufacturer. As already mentioned in Section II, diode D_3 was not mounted in the prototype board; instead a small saturable core (A_L = 5110 nH, T38) was used in order to damp the parasitic oscillations occurring at the end of interval [T_5, T_6] when diode D_1 turns off. Moreover a small R-C (4.7 kΩ, 10 nF) snubber was put in parallel to diode D_f. The control circuit is instead implemented by means of discrete components, basically as described in [11]. The resulting filtered input current waveform at nominal power and 230 V_{RMS} input voltage is shown in Fig. 5, together with the input voltage: as we can see, the deviation from the ideal sinusoidal waveform is modest and the resulting harmonic content is quite low.

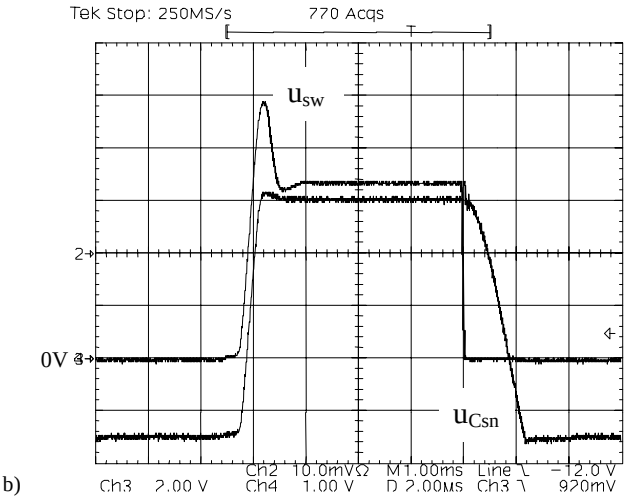
TABLE I
CONVERTER PARAMETERS

Input voltage	U_i	90-230 V_{RMS}
Output voltage	U_o	48 V
Output power	P_o	200 W
Transformer turns ratio	$n=n_2/n_1$	0.165
Switching frequency	f_s	60 kHz
Output capacitor	C_L	2200 μF
Magnetising inductance	L_μ	1 mH
Leakage inductance	L_d	15 μH
Snubber inductor	L_{sn}	300 μH
Snubber capacitor	C_{sn}	4 nF

Considering the IEC 1000-3-2 harmonic standards, Table II shows the harmonic content of the line current at 230 V_{RMS} input voltage and nominal output power. The measured converter efficiency, in these conditions, is η = 86%. As can be seen, each harmonic is kept well below the standard limits.



a)



b)

Fig. 6- Switch collector-to-source voltage u_{sw} [200 V/div] and voltage across the snubber capacitor u_{Csn} [200 V/div] in a switching period recorded at the peak of the line voltage: a) @ U_g = 90 V_{RMS}, b) @ U_g = 230 V_{RMS}

The current total harmonic distortion (THD_I) is about 13%, being the input voltage distortion (THD_V) about 1.7%. Fig. 6 reports the switch and snubber capacitor voltage in a

TABLE II
HARMONIC ANALYSIS OF INPUT CURRENT I_i @ U_i = 230 V_{RMS}, P_o = 200 W

Harmonic order	Measured value [mA_{RMS}]	IEC 1000-3-2 limit [mA_{RMS}]
1	1000	
3	117.5	2300
5	52.5	1140
7	22.9	770
9	5.5	400
11	15.8	330
13	4.9	210
15	4.2	150
17	8.9	132
19	4.7	118
21	7.8	107
23	7.6	98
25	3.1	90
27	6.8	83
29	6.0	77
31	6.9	73
33	8.3	68
35	7.1	64
37	7.1	61
39	6.2	58

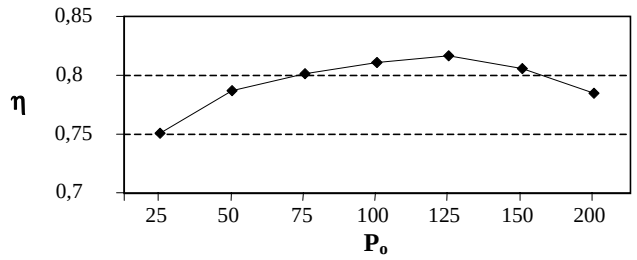


Fig. 7- Measured converter efficiency as a function of the output power P @ U_i = 90 V_{RMS}

switching period, measured at the peak of the input voltage U_i. The dv/dt across the switch at turn-off is limited to about 1.4 V/ns. It is important to notice that, when the input voltage U_i is minimum (90 V_{RMS}), the snubber capacitor discharges through diode D_2 during interval [T_6, T_7], as previously explained. Being the final voltage value still higher than U_g, this discharge process doesn't imply the loss of the soft-switching condition, as it was expected.

Lastly, Fig. 7 shows the measured efficiency of the flyback rectifier as a function of the output power P_o, measured at U_g = 90 V_{RMS}. As can be seen, the efficiency always remains greater than 75%, even at the minimum load condition, with a peak value close to 82%.

VI. Conclusions

The paper discusses the design of a flyback rectifier characterised by high power factor and efficiency. The rectifier employs a lossless snubber circuit to achieve soft-switching and to limit the voltage dv/dt across the power switch. This is an emitter switching device that is going to be integrated on a smart power chip together with the control circuit. Experimental results are presented to validate the design procedure.

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Appendix

DC voltage conversion ratio

In order to find an approximated expression for the voltage conversion ratio $M=U_{op}/U_g$ as a function of the duty-cycle and of the operating point, let's neglect interval T_{01} as compared to the switching period so that we can assume $T_{on}\approx T_{04}$. Starting from the volt·second balance across the magnetising inductance, from Fig. 2 we can write:

$$\frac{1}{T_S}\left(U_g + U_{op}\right)\left(T_{14} + \frac{T_{45}}{2}\right) - U_{op} = 0 \quad \Rightarrow \quad \frac{M}{1+M} \approx d + \frac{T_{45}}{2T_S} \tag{A.1}$$

where the right-hand side highlights the corrective term $T_{45}/2T_S$ caused by the snubber operation. This can be found from (12), i.e.:

$$\frac{T_{45}}{2T_S} = \frac{C_{sn}}{2T_S} U_{op}\left(\frac{1+M}{M}\right)\frac{1}{I_\mu + \frac{U_g d T_S}{2L_\mu}}, \tag{A.2}$$

where a simplified expression for $I_{\mu p}$ was used and I_μ stands for the average magnetising current. Substituting (A.2) into (A.1) we can write:

$$I_\mu = \frac{U_g}{2L_\mu f_S}\left(\frac{(1+M)^2}{M(1-d)-d}\frac{C_{sn}L_\mu}{T_S^2} - d\right) \tag{A.3}$$

The average input current I_g, from Fig. 2, can be expressed as:

$$I_g = d\, I_\mu - \frac{T_{23}}{2T_S} i_{Lsn}(T_{02}) \tag{A.4}$$

By using (6) and (8) and taking into account the power balance $I_gU_g=U_oI_o$, we can write:

$$I_g = d\, I_\mu - \frac{C_{sn}}{2T_S}\frac{1}{U_g}\left(U_1^2 - U_g^2\right) = \frac{U_{op}^2}{R_L} n^2 \frac{1}{U_g}. \tag{A.5}$$

Now, by using (A.3), (A.5) and (17) we can find an approximated expression of the voltage conversion ratio M as a function of the duty-cycle and the load resistance. Before doing that it is worth normalising voltages and currents by using the following base quantities:

Base impedance: $Z_N = 2L_\mu f_S$ (A.6a)

Base voltage: $U_N = U_g$ (A.6b)

Base current: $I_N = \frac{U_N}{Z_N}$ (A.6c)

Using (A.6) into (A.3) gives:

$$I_{\mu N} = \frac{\alpha(1+M)^2}{M(1-d)-d} - d \tag{A.7}$$

where $\alpha = \frac{C_{sn}L_\mu}{T_S^2}$. Note that the condition for continuous conduction mode of operation (CCM) becomes:

$$I_\mu > \frac{U_g d}{2L_\mu f_S} \quad \Rightarrow \quad I_{\mu N} > d \tag{A.8}$$

Finally, substituting (17) into (A.5) and using (A.6) we obtain:

$$k = \frac{1}{(nM)^2}\left[d\, I_{\mu N} - \alpha\left(M^2 - 1 + 2MZ_{dN}(I_{\mu N} + d) + Z_{dN}^2(I_{\mu N} + d)^2\right)\right] \tag{A.9}$$

where $k = \frac{2L_\mu f_S}{R_L} = \frac{1}{R_{LN}}$. Equations (A.7) and (A.9) can be used together to plot M as a function of d and k (a MathCad© program was used to do that, thus generating Fig. 4).