Improved Three-Phase High-Quality Rectifier With Line-Commutated Switches

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***Abstract*—The paper presents a three-phase diode rectifier with an add-on simple cell with line-frequency commutated ac switches that is able to greatly improve both power factor and output voltage regulation of rectifiers with passive L–C filters. The boost action introduced by the commutation cell allows for a complete compensation of the voltage drop across the input inductors, so as output voltage regulation can be maintained from no-load to full-load. Moreover, as compared to other line-frequency commutated rectifiers, the proposed circuit allows compliance with the low-frequency harmonic limits defined in the technical report IEC 61000-3-4 for any power range. High-efficiency and minimum EMI are obtained due to the low-frequency commutations. A converter prototype was built and tested. The results confirm the theoretical analysis.**

***Index Terms*—Power electronics, power quality, rectifiers.**

I. Introduction

THREE-PHASE diode bridge rectifier utility interfaces, which are extensively used in many high-power low-cost applications that do not require bidirectional power flow like adjustable speed drives, draws highly distorted line currents from the utility grid, which leads to an unacceptable degradation in the power quality. In the attempt to reduce their effects, various standard and recommendations have been introduced in order to limit the harmonics that an individual load can inject into the utility. Recently, the Technical Report IEC 61 000-3-4 was issued with the intent to extend the field of application of standard IEC 61 000-3-2 for electrical and electronic equipment with a rated input current exceeding 16-A per phase [1]. Thus, to improve the power quality of these utility interfaces is becoming mandatory.

In the last decade, a number of new techniques have been proposed for improving the harmonic content of the current drawn by three-phase diode rectifiers. One popular technique exploits the injection, into the ac line, of a third harmonic current, which, summed to the current drawn by the rectifier gives almost sinusoidal input currents, with a total distortion around 5%. In [2]–[6] the third harmonic current is generated in the dc side of the rectifier by using two boost converters which modulate the dc link current, while in [7] a low-frequency transformer and a single boost converter is used. Then, the third harmonic current is injected in the ac side by using either tuned L–C branches [2], [3] or special three-phase transformer (wye-delta, zigzag) [4]–[7]. In [8], the same third harmonic injection approach was used in a completely passive implementation, just using a wye-delta transformer and an inductance connected to a dc midpoint voltage. However, all these techniques suffer for some limitations at high power levels, mainly for the VA rating of the magnetic components, which increases cost, volume and weight of the overall utility interface.

A different approach is proposed in [9], where three low-power line-frequency commutated switches and three line inductors are employed in order to reduce the input current distortion of three-phase diode rectifiers with a capacitive filter. The circuit feature low-cost, simplicity, high efficiency and low EMI, and is particularly appropriate for high-power applications. However, the proposed circuit does not fully exploit its potentiality.

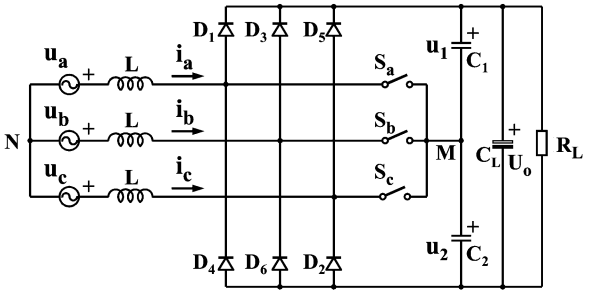

Fig. 1. Scheme of the proposed three-phase high-quality rectifier.

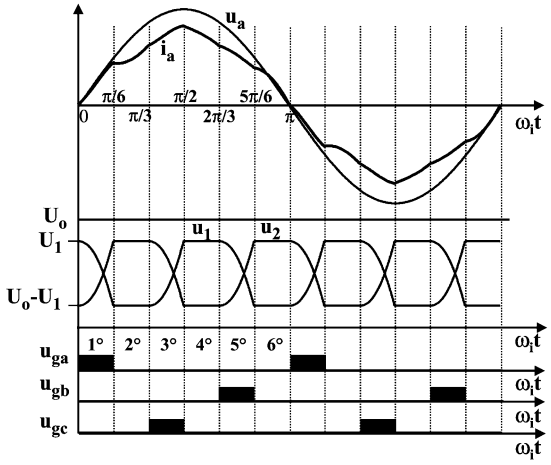

Fig. 2. Main converter waveforms in a line period. From top to bottom: phase a voltage and current, output voltage U_o, capacitor voltages u_1 and u_2, and drive signal patterns.

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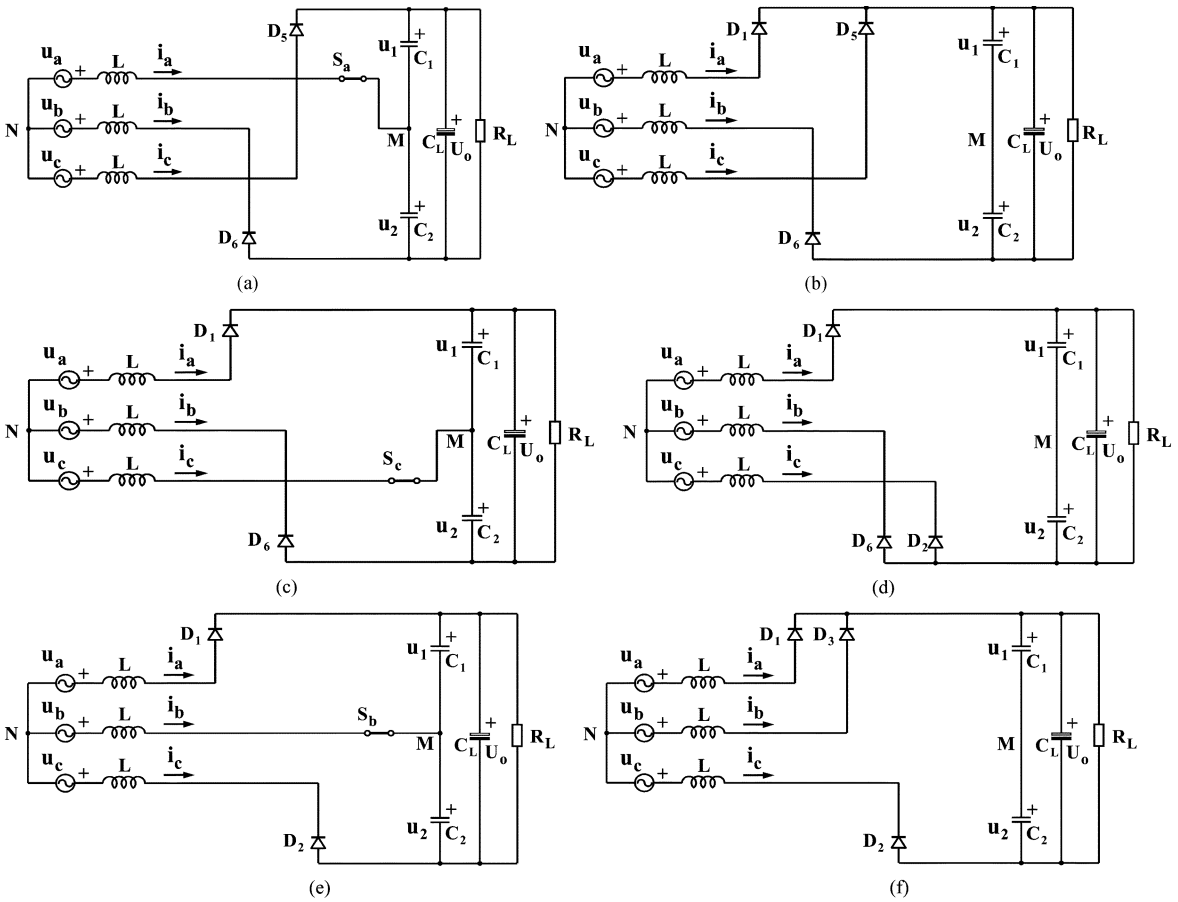

Fig. 3. Subtopologies corresponding to different intervals during the line half period: (a) $0 \leq \theta \leq \pi/6$, (b) $\pi/6 \leq \theta \leq \pi/3$, (c) $\pi/3 \leq \theta \leq \pi/2$, (d) $\pi/2 \leq \theta \leq 2\pi/6$, (e) $2\pi/2 \leq \theta \leq 5\pi/6$, and (f) $5\pi/6 \leq \theta \leq \pi$.

In this paper a similar structure is proposed in which the input inductors are allowed to resonate with dc link capacitors, thus adding the following feature to the original converter [9]:

1) increased boost action, which allows for a complete compensation of the voltage drop across the input inductors, from no-load to full-load;
2) reduced input current harmonic content, thus complying with limits IEC 61 000-3-4 at any power level.

In Section II, the converter behavior is analyzed in detail and expressions for input current waveforms are derived, in Section III the input current harmonic content is calculated while in Section IV suitable design criteria are given. Measurements on an experimental prototype are reported in Section V, showing a good agreement with the theoretical analysis.

II. Converter Analysis

The proposed three-phase high-quality rectifier is shown in Fig. 1. As we can see, it is topologically similar to the Vienna rectifier (but in this case the switches commutate at low frequency) and to the rectifier presented in [9], the main difference being the reduced value of the output capacitors C_1 and C_2, which allows for the resonance between input inductor and these capacitors to occur during each switch turn-on interval. This resonance, substantially improves the input current waveforms, and introduces a new degree of freedom in the converter design, as compared to the original topology. Switches S_a, S_b, S_c are bidirectional switches that can be built by using one switch and a diode bridge rectifier each. All these components are commutated at line frequency, which reduces EMI and losses and allows for the utilization of slow devices, thus saving cost and improving converter reliability. Moreover, the input inductors are standard line-frequency iron-core low-cost inductors.

In the following, the input current and capacitor voltage waveforms are calculated in the line half period, assuming the following conditions:

1) balanced three-phase input voltages ($u_a = U_{pk}\sin(\omega_i t)$, $u_b = U_{pk}\sin(\omega_i t - 2\pi/3)$, $u_c = U_{pk}\sin(\omega_i t + 2\pi/3)$);
2) voltages u_1 and u_2 across the two resonant capacitors C_1 and C_2 satisfying the following inequality: $0 < u_1, u_2 < U_o$;
3) constant output voltage U_o;
4) syncronized switch turn on with zero crossing of the corresponding phase voltage;
5) switch turn on interval equal to $T_i/12$ (T_i is the line period) at nominal output power.

The gate signals sequence is shown in Fig. 2, together with phase voltage u_a, phase current i_a, output voltage U_o and capacitor voltages u_1 and u_2. The line half period is subdivided into six intervals which are indicated by the value of the line angle $\theta = \omega_i t$, as shown in Fig. 2. The topological sequence, starting from $\theta = 0$ up to $\theta = \pi$, is described by the six subtopologies shown in Fig. 3, while the equations describing

TABLE I
EQUATIONS DESCRIBING PHASE CURRENT i_a AND CAPACITOR VOLTAGE u_2 IN A LINE HALF PERIOD

Interval	Fundamental equations
	$i_{aN}(\theta)=\frac{1}{\alpha^2-1}[\cos(\theta)-\cos(\alpha\theta)+K(\alpha)\sin(\alpha\theta)]$, $u_{2N}(\theta)=\frac{M(\alpha)}{2}+\frac{3}{2}\frac{\alpha}{\alpha^2-1}[\alpha\sin(\theta)-\sin(\alpha\theta)-K(\alpha)\cos(\alpha\theta)]$
$0 \le \theta \le 30°$	$I_{a1N}=\frac{1}{\alpha^2-1}\left[\frac{\sqrt{3}}{2}-\cos\left(\alpha\frac{\pi}{6}\right)+K(\alpha)\sin\left(\alpha\frac{\pi}{6}\right)\right]$
$30° \le \theta \le 60°$	$i_{aN}(\theta)=I_{a1N}+\frac{\sqrt{3}}{2}-\cos(\theta)-\frac{M(\alpha)}{3}\left(\theta-\frac{\pi}{6}\right)$, $u_{2N}(\theta)=U_{1N}$, $I_{a2N}=I_{a1N}+\frac{\sqrt{3}-1}{2}-M(\alpha)\frac{\pi}{18}$
$60° \le \theta \le 90°$	$i_{aN}(\theta)=I_{a2N}+\frac{\alpha^2}{2(\alpha^2-1)}\cos\left(\theta-\frac{\pi}{3}\right)-\cos(\theta)-\frac{M(\alpha)}{2}\left(\theta-\frac{\pi}{3}\right)-\frac{1}{2(\alpha^2-1)}\left[\cos\left(\alpha\left(\theta-\frac{\pi}{3}\right)\right)-K(\alpha)\sin\left(\alpha\left(\theta-\frac{\pi}{3}\right)\right)\right]$ $u_{2N}(\theta)=\frac{M(\alpha)}{2}-\frac{3}{2}\frac{\alpha}{\alpha^2-1}\left[\alpha\sin\left(\theta-\frac{\pi}{3}\right)-\sin\left(\alpha\left(\theta-\frac{\pi}{3}\right)\right)-K(\alpha)\cos\left(\alpha\left(\theta-\frac{\pi}{3}\right)\right)\right]$ $I_{a3N}=I_{a2N}-M(\alpha)\frac{\pi}{12}-\frac{1}{2(\alpha^2-1)}\left[\cos\left(\alpha\frac{\pi}{6}\right)-K(\alpha)\sin\left(\alpha\frac{\pi}{6}\right)-\alpha^2\frac{\sqrt{3}}{2}\right]$
$90° \le \theta \le 120°$	$i_{aN}(\theta)=I_{a3N}-\cos(\theta)-\frac{2}{3}M(\alpha)\left(\theta-\frac{\pi}{2}\right)$, $u_{2N}(\theta)=U_{oN}-U_{1N}$, $I_{a4N}=I_{a3N}+\frac{1}{2}-M(\alpha)\frac{\pi}{9}$
$120° \le \theta \le 150°$	$i_{aN}(\theta)=I_{a4N}-\frac{\alpha^2}{2(\alpha^2-1)}\cos\left(\theta-\frac{2\pi}{3}\right)-\cos(\theta)-\frac{M(\alpha)}{2}\left(\theta-\frac{2\pi}{3}\right)+\frac{1}{2(\alpha^2-1)}\left[\cos\left(\alpha\left(\theta-\frac{2\pi}{3}\right)\right)-K(\alpha)\sin\left(\alpha\left(\theta-\frac{2\pi}{3}\right)\right)\right]$ $u_{2N}(\theta)=\frac{M(\alpha)}{2}+\frac{3}{2}\frac{\alpha}{\alpha^2-1}\left[\alpha\sin\left(\theta-\frac{2\pi}{3}\right)-\sin\left(\alpha\left(\theta-\frac{2\pi}{3}\right)\right)-K(\alpha)\cos\left(\alpha\left(\theta-\frac{2\pi}{3}\right)\right)\right]$
$150° \le \theta \le 180°$	$i_{aN}(\theta)=I_{a5N}-\frac{\sqrt{3}}{2}-\cos(\theta)-\frac{M(\alpha)}{3}\left(\theta-\frac{5\pi}{6}\right)$, $u_{2N}(\theta)=U_{1N}$, $I_{a6N}=0$ $I_{a5N}=I_{a4N}-M(\alpha)\frac{\pi}{12}+\frac{1}{2(\alpha^2-1)}\left[\cos\left(\alpha\frac{\pi}{6}\right)-K(\alpha)\sin\left(\alpha\frac{\pi}{6}\right)+(\alpha^2-2)\frac{\sqrt{3}}{2}\right]$

normalized phase current i_{aN} and capacitor voltage u_{2N} are reported in Table I. The following base variables have been used for normalization:

$$\text{Base voltage: } U_N = U_{pk} \tag{1.a}$$

$$\text{Base current: } I_N = \frac{U_{pk}}{\omega_i L} \tag{1.b}$$

$$\text{Basepower: } P_N = U_N I_N = \frac{U_{pk}^2}{\omega_i L}. \tag{1.c}$$

The other parameters used in the equations are ($C = C_1 = C_2$)

$$\text{Resonant angular frequency: } \omega_o = \frac{1}{\sqrt{3LC}}$$

$$\text{Normalized resonant frequency: } \alpha = \frac{\omega_o}{\omega_i}$$

$$\text{Adimensional parameter: } K(\alpha) = \frac{\frac{\alpha}{2} - \sin\left(\alpha\frac{\pi}{6}\right)}{1+\cos\left(\alpha\frac{\pi}{6}\right)}$$

$$\text{Voltage conversion ratio: } M(\alpha) = \frac{U_o}{U_{pk}}.$$

Note that the other phase currents have similar expressions as i_{aN} simply shifted by $T_i/3$, as respect to current i_a, while voltage u_1 is simply given by the difference between output voltage U_o and voltage u_2.

The expression for the voltage conversion ratio $M(\alpha)$ used in these equations is derived by imposing a zero value for the current at the end of the line half period (see I_{a6N} in the last row of Table I). The result is the following relation:

$$M(\alpha) = \frac{18}{7\pi}\left\{1+\frac{\sqrt{3}}{2}\frac{\alpha^2}{\alpha^2-1}-\frac{1}{\alpha^2-1} \times \left[\cos\left(\alpha\frac{\pi}{6}\right)-K(\alpha)\sin\left(\alpha\frac{\pi}{6}\right)\right]\right\} \tag{2}$$

while the expression for the initial voltage value across C_1, denoted U_1 in Fig. 2, derived by letting $u_1(\pi/6) = U_o - U_1$, is given by

$$U_{1N} = \frac{M(\alpha)}{2} + \frac{3}{2}\frac{\alpha}{\alpha^2-1}K(\alpha). \tag{3}$$

As we can see, the voltage conversion ratio together with the phase current waveforms, depend only on the normalized resonant frequency α.

Fig. 4, reports the voltage conversion ratio M and the initial capacitor voltage U_1 normalized to the output voltage U_o

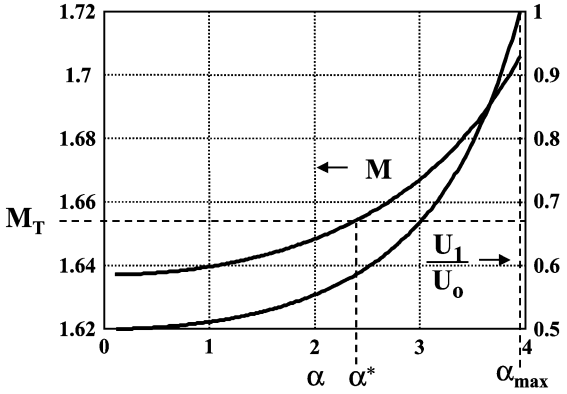

Fig. 4. Voltage conversion ratio M and initial capacitor voltage $\mathrm{U_1}$ normalized to the output voltage $\mathrm{U_o}$ as a function of normalized resonant frequency α.

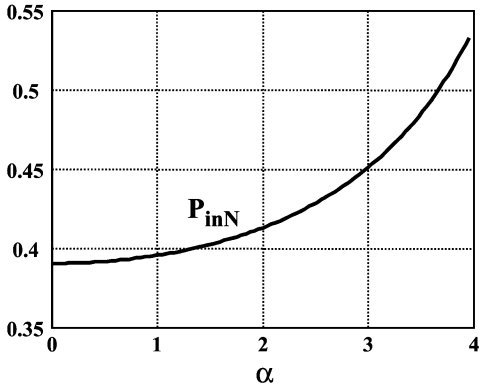

Fig. 5. Normalized average input power as a function of parameter α.

as a function of parameter α (note that $\mathrm{U_1/U_o = U_{1N}/M}$). The same figure reports also the value of the theoretic voltage conversion ratio of a standard three-phase diode bridge rectifier without input inductances given by

$$\mathrm{M_T} = \frac{\mathrm{U_{oT}}}{\mathrm{U_{gpk}}} = \frac{3}{\pi}\sqrt{3} = 1.654.$$

To the purpose of comparison, the original converter [9] was able to achieve a voltage conversion ratio equal to 1.637 only, that corresponds exactly to the value which tends expression (2) for α approaching zero. In fact, when the value of capacitors $\mathrm{C_1}$ and $\mathrm{C_2}$ is chosen high enough so as to keep their voltage constant and equal to $\mathrm{U_o}/2$, the converter behaves in the same manner as the original one, and the resonant frequency becomes very low (see also in Fig. 4 the voltage $\mathrm{U_1}$ tends to $\mathrm{U_o}/2$ at low α values). Thus, the proposed converter provides enough boost action so as to completely compensate for the voltage drop across the input inductors. This means that it is possible to maintain the output voltage constant from zero output current to the nominal load simply reducing the on-time of switches $\mathrm{S_a}, \mathrm{S_b}$, and $\mathrm{S_c}$, provided that a value of α greater than $\alpha^* = 2.385$ is chosen (see Fig. 4).

From Fig. 4 we can also see that the maximum voltage conversion ratio is limited by the value of parameter α that causes a complete swing of voltages $\mathrm{u_1}$ and $\mathrm{u_2}$ from zero to $\mathrm{U_o}$. Such value can be derived by setting $\mathrm{U_{1N}} = \mathrm{M}$ in (3). The result is $\alpha_{\max} = 3.952$ (see Fig. 4). The maximum voltage conversion ratio results $\mathrm{M_{max}} = 1.706$. For a higher value of parameter α the current distortion increases, so as a good design should select $\alpha < \alpha_{\max}$.

Since the input current waveform at nominal power depends only on parameter α, we can choose the input inductance value based only on the desired output power. In fact, the three-phase average input power is

$$\mathrm{P_{in}} = \frac{3}{\pi}\int_0^{\pi} \mathrm{u_a}(\theta)\mathrm{i_a}(\theta)\,\mathrm{d}\theta = \frac{\mathrm{U_{pk}^2}}{\omega_\mathrm{i}\mathrm{L}}\frac{3}{\pi}\int_0^{\pi} \mathrm{u_{aN}}(\theta)\mathrm{i_{aN}}(\theta)\,\mathrm{d}\theta = \frac{\mathrm{U_{pk}^2}}{\omega_\mathrm{i}\mathrm{L}}\,\mathrm{P_{inN}} \qquad (4)$$

where $\mathrm{P_{inN}}$ is the normalized average input power, which is shown in Fig. 5 as a function of parameter α. This diagram was obtained by using the MathCad software to evaluate (4) with the phase current waveform definition reported in Table I. As we can see, the resonant intervals give a power gain, as compared to the original solution with constant capacitor voltages, which can be as high as 36.4% ($\mathrm{P_{in}}(0) = 0.391, \mathrm{P_{in}}(\alpha_{\max}) = 0.533$).

TABLE II
LIMITS OF TECHNICAL REPORT IEC 61 000-3-4: "STAGE1: CURRENT EMISSION VALUES FOR SIMPLIFIED CONNECTION OF EQUIPMENT ($\mathrm{S_{EQU}} \le \mathrm{S_{SC}}/33$)"

Harmonic number n	Admissible harmonic current $\mathrm{I_n/I_1}^*$ %	Harmonic number n	Admissible harmonic current $\mathrm{I_n/I_1}^*$ %
3	21.6	21	≤ 0.6
5	10.7	23	0.9
7	7.2	25	0.8
9	3.8	27	≤ 0.6
11	3.1	29	0.7
13	2	31	0.7
15	0.7	≥ 33	≤ 0.6
17	1.2		
19	1.1	Even	≤ 8/n or ≤ 0.6

III. INPUT CURRENT ANALYSIS

The major claimed benefit of the proposed converter, as compared to the original one, is the reduction of the input current harmonic content. Since the proposed converter is suitable for high power applications, we will take as reference the harmonic limits described in the technical report IEC 61 000-3-4: *"Limitation of emission of harmonic currents in low-voltage power supply systems for equipment with rated current greater than 16 A per phase"*.

In particular, the limits are those called "stage 1: current emission values for simplified connection of equipment ($\mathrm{S_{equ}} \le \mathrm{S_{sc}}/33$)," and are reported in Table II. As we can see, each harmonic current limit is specified as a function of the rated fundamental current (up to the 40th harmonic). This fact allows analyzing the converter input current normalized to a unity fundamental current, so as to obtain results that are independent of the input power.

As already observed in the previous sections, the input current waveform, at nominal output power, depends only on the value of the normalized resonant frequency α. Thus, an analysis was performed in order to calculate the current harmonic amplitudes at different α values. The results are reported in Fig. 6

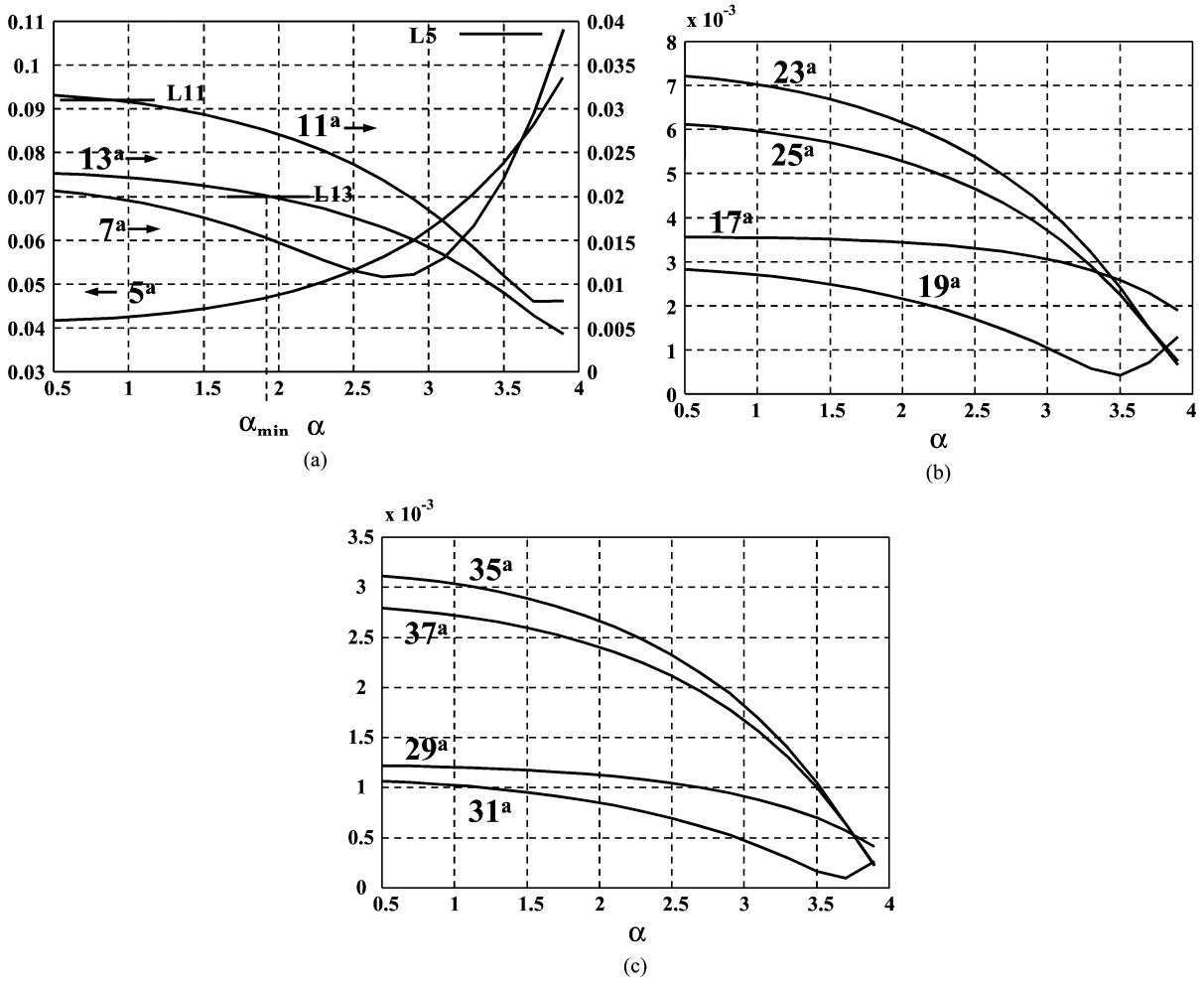

Fig. 6. Simulated input current harmonic amplitudes as a function of normalized resonant frequency α (unity fundamental component): (a) harmonics $5^{a}, 7^{a}, 11^{a}, 13^{a}$, (b) harmonics $17^{a}, 19^{a}, 23^{a}, 25^{a}$, and (c) harmonics $29^{a}, 31^{a}, 35^{a}, 37^{a}$.

(unity fundamental component), together with limit values L5, L11, and L13 corresponding to fifth, 11th, and 13rd harmonic limits (all the others are outside the graph scale). It is worth to remember that, as stated in the technical report, all harmonics having amplitude lower than 0.6% of the rated fundamental component can be disregarded. Thus, the 17th, 19th, and above 25th can be always neglected, no matter the value of α is. Another interesting results is that the original converter does not comply with these limits, at any output power, since 11th and 13th harmonics exceed their limits. The minimum value of $\alpha_{\min}$ needed to comply with the standard is 1.95.

IV. Design Example

In this section we report the design example of a converter having the following specifications:

$$\text{Input voltage: } U_g = 230V_{rms}$$
$$\text{Output power: } P_o = 10\ \text{kW}$$
$$\text{Estimated converter efficiency: } \eta = 1.$$

The efficiency was considered unity to allow a comparison of theoretical expectations with simulation results.

The design procedure is as follows:

TABLE III
Input Current Harmonic Amplitudes at Different Power Levels

	Current (A) for differents power levels					Limits	
Pi (W)	9828	8484	5820	3720	1830	930	IEC1000-3-4
1	25.3	22.3	16.64	10.2	5	2.46	-
3	0.15	0.136	0.12	0.032	0.074	0.082	5.4648
5	2.03	1.51	0.444	0.728	0.678	0.578	2.7071
7	0.432	0.476	1.28	1.252	0.794	0.556	1.8216
9	0.01	0.014	0	0.032	0.024	0.018	0.9614
11	0.33	0.462	0.572	0.528	0.19	0.15	0.7843
13	0.276	0.278	0.204	0.204	0.256	0.196	0.506
17	0.084	0.062	0.156	0.316	0.12	0.084	0.3036
19	0	0.138	0.128	0.23	0.15	0.116	0.2783
23	0.062	0.102	0.016	0.032	0.116	0.046	0.2277
25	0.062	0.068	0.028	0.072	0.08	0.058	0.2024
29	0.022	0.046	0	0.026	0.094	0.032	0.1771
31	0	0.072	0	0.018	0.058	0.04	0.1771
35	0.014	0.036	0.04	0.046	0.048	0.032	0.1518
37	0.026	0.042	0.04	0.022	0.036	0.032	0.1518

1) choose a suitable value of α greater than $\alpha_{\min}$ (this is needed to keep the current harmonic amplitude below the limits stated in the technical report IEC 61 000-3-4 also at a reduced load value, for which the reduction of the switch on-time, necessary to keep the output voltage constant, causes an increase in the input current distortion);

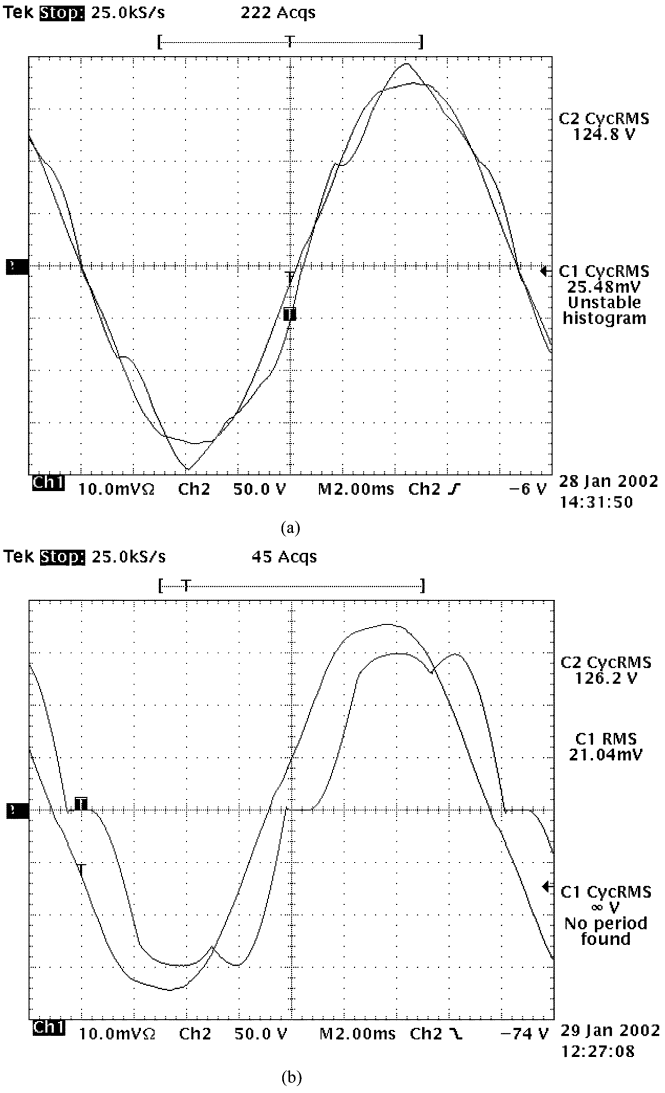

Fig. 7. Measured phase voltage (50 V/div.) and current (10 A/div.) waveforms at nominal output power. (a) Proposed rectifier. (b) Standard rectifier with the same input inductors.

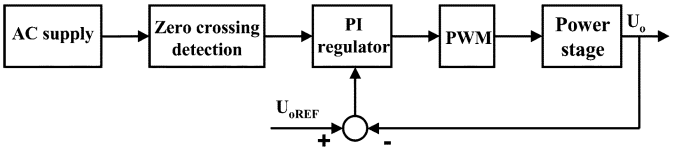

Fig. 8. Control block scheme.

2) calculate the input inductance value needed for the specified input power $\mathrm{P_{in}} = \mathrm{P_o}/\eta$ using (4) and Fig. 5;
3) calculate the output capacitor from the knowledge of parameters α and L, using the definition of α and ω_o;
4) verify the input current harmonic content at lower output power levels.

The last step comes from the need to verify the compliance with the limits stated in the technical report IEC 61 000-3-4 in the worst case condition that does not correspond to the nominal output power for each harmonic. Some of them may, in fact, increase at reduced power levels because of the reduced switch on-time needed to keep constant the output voltage (see, for example, the 11th harmonic in Table III of the experimental results section). We choose $\alpha = 3$, higher than $\alpha_{\min}$ and α^*. From (2) and (3) the output voltage turns out to be 542.3 V, while the initial capacitor voltage $\mathrm{U_1}$ results 362.6 V. From (4), the input inductance value needed to achieve the desired power is $\mathrm{L} = 15.21$ mH, and from the definition of α and ω_o, the output capacitor values result $\mathrm{C} = 24.67\ \mu$F. Note that the minimum value of capacitor C which causes the initial voltage $\mathrm{U_1}$ to be equal to $\mathrm{U_o}$ is $\mathrm{C_{min}} = 14.2\ \mu$F (it corresponds to $\alpha_{\max}$).

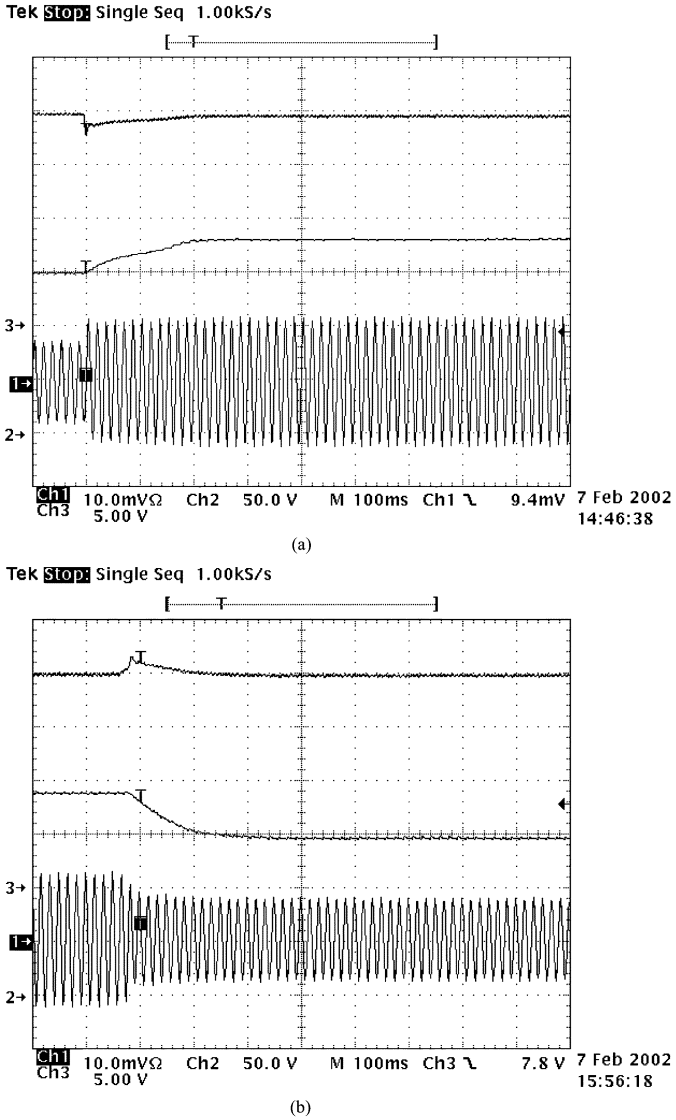

Fig. 9. Step load change from (b) 3.7 kW to 5.8 kW and (b) viceversa. From top to bottom: Output voltage (channel 2—50 V/div), PI control voltage (channel 3—5 V/div) and input current (channel 1—20 A/div), time (100 ms/div).

The simulation, at nominal conditions, gives an average output voltage of 541 V (output filter capacitor $\mathrm{C_L} = 1000\ \mu$F), and the input current spectrum showed a very good agreement with the calculated one. A higher value of α, as compared to the minimum value based on nominal conditions, is necessary to maintain the harmonic amplitudes below the limits from no load to full load.

As a final remark, we can observe that the converter design is not much affected by parameter uncertainties. In fact, as long

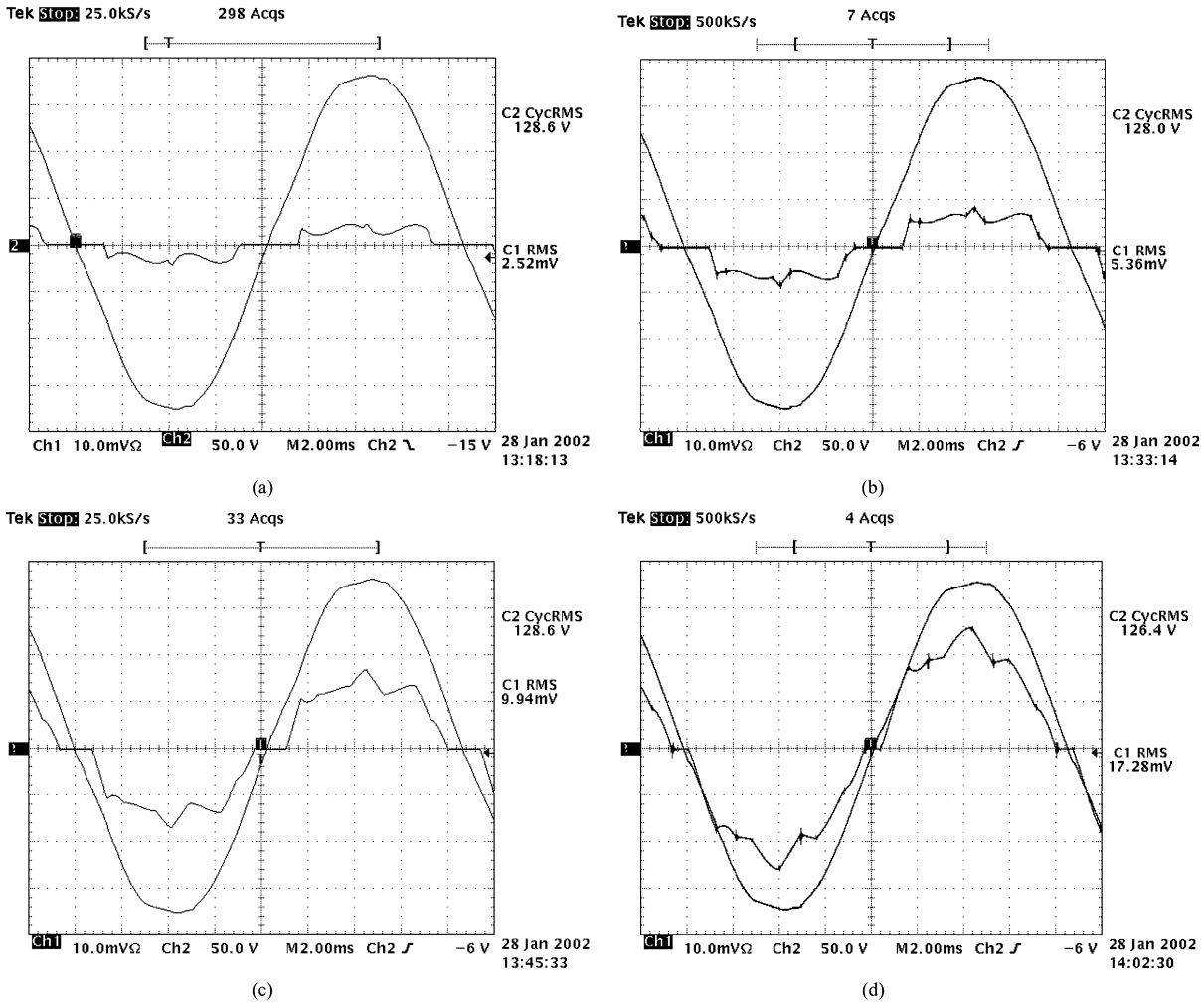

Fig. 10. Phase voltage (50 V/div.) and current (10 A/div.) waveforms at different power levels: (a) 930 W, (b) 1830 W, (c) 3720 W, and (d) 5820 W.

as we choose an α value higher than $\alpha_{\min}$ and α^* we guarantees the output voltage regulation in the whole load range as well as compliance with the standard at least at nominal output power. As far as the input inductor values is concerned, it directly affects the maximum output power, thus it is sufficient to guarantee that its maximum value (taking into account fabrication tolerances) satisfies the output power constraint at minimum input voltage. Moreover, from the control point of view, as the cut-off frequency is low, the circuit parameters do not significantly affect the closed-loop behavior.

V. Experimental Results

A 9.8-kW prototype was built with the following parameters: input voltage 127 $V_{\rm RMS}$, input inductor value 4.2 mH, resonant capacitor value 42.7 μF (corresponding to $\alpha = 3.6$), output voltage 292 V. A simple PI regulator was employed to keep constant the output voltage at reduced power levels.

The measured phase voltage and current waveforms are shown in Fig. 7(a) at nominal output power. The input power factor is 0.994 and the output voltage is 292 V, while the efficiency is 96%. For comparison purposes, Fig. 7(b) shows phase current and voltage for the rectifier without auxiliary circuit (same input inductors): the output voltage decreases to 241 V, thus reducing the available output power to 7.1 kW, and the resulting power factor is 0.91.

Fig. 8 shows the control block scheme: the adopted control strategy delays the switch drive signals (see Fig. 2) with respect to each phase voltage zero crossing, while keeping constant their turn-off instant. This strategy was selected in order to maintain the displacement between each phase voltage and the corresponding current fundamental component close to zero. The synchronization with the phase voltage was made with comparators. A filter was used to avoid the commutation noise.

Since each switch on-time can be varied from zero to a maximum value equal to $1/12$ of the fundamental period, at nominal load the control can accommodate only an increase of the input voltage above the nominal value. In this case, a higher input current distortion is obtained; however, the compliance with the limits is not affected since it must be tested only at the rated input voltage.

Fig. 9 reports the output voltage, the PI control voltage and a phase input current in the case of a step load change from 3.7 kW to 5.8 kW [Fig. 9(a)] and viceversa [Fig. 9(b)]: in both case the control dynamic shows a high phase margin and the settling time is approximately 200 ms.

The phase voltage and current waveforms are shown in Fig. 10 at different power levels, and the corresponding current

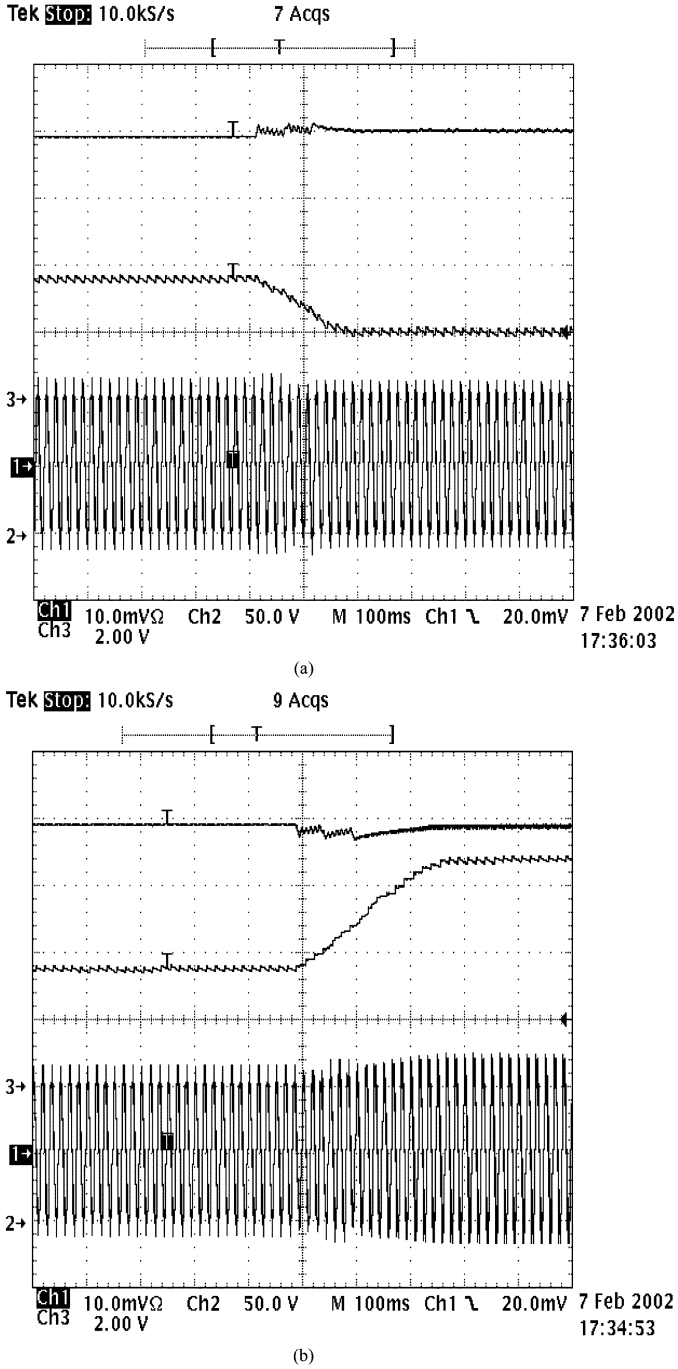

Fig. 11. From top to bottom: Output voltage (channel 2—50 V/div), PI control voltage (channel 3—2 V/div) and input current (channel 1—10 A/div), during an input voltage variation: (a) 127 $V_{RMS} + 5\%$; (b) 127 $V_{RMS} - 5\%$; time (100 ms/div).

harmonics are reported in Table III, together with the limits imposed by the technical report IEC 61 000-3-4. As can be seen, compliance with the limits is achieved in any load condition. Note, also, that each fundamental current component is practically in phase with the corresponding voltage, thanks to the adopted control strategy.

Table IV shows the total harmonic distortion (THD) of each phase current, the power factor and the displacement factor: note that the highest THD occurs at minimum output power, while at nominal power it is below 10%.

TABLE IV
INPUT CURRENT DISTORTION, DISPLACEMENT FACTOR $\cos\varphi_1$ AND POWER FACTOR FOR DIFFERENTS POWER LEVELS

P_i(W)	$I_i(A_{RMS})$	THD (%)	$\cos\varphi_1$	PF
930	2.67	46.2	0.99	0.88
1830	4.97	30.6	0.99	0.94
3720	9.77	17.1	0.99	0.98
5820	15.0	10.8	1	0.99
8400	22.0	8.3	1	0.99
9600	25.2	8.6	1	0.99

Also the power factor presents the highest value at high power levels, and decreases to 0.88 at 10% of nominal power.

Finally, a 4.5 kVA programmable AC power supply was employed to analyze the rectifier dynamic response under transient power supply conditions (127 V $\pm 5\%$). The output voltage, the PI control voltage and a phase current are shown in Fig. 11 during a step increase $(+5\%)$ (Fig. 11(a)) and a step decrease (-5%) of the input voltage [Fig. 11(b)]. In the latter case the control was able to accommodate for the reduction of the input voltage because the test was done at reduced output power. As can be seen, after a settling time of 180 ms in the first case and of 300 ms in the second case, the output voltage returns to the nominal value with a small overshoot or undershoot.

VI. CONCLUSION

The proposed add-on circuit is able to compensate for current distortion produced by diode bridge rectifiers with capacitive filter. The resulting current harmonics are below the limits of IEC61000-3-4 for any power level.It is possible to regulate the output voltage and partially compensate for input voltage variations by adjusting the auxiliary switch signals. The use of a low-frequency commutation minimizes losses, thus increasing the overall efficiency. Moreover, the needed input inductor values are reduced as compared to a purely passive circuit. The experimental results have confirmed the theoretical analysis.

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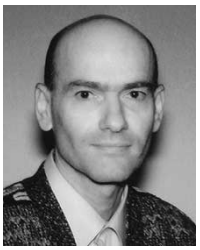

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