Susceptibility of Integrated Circuits to RFI

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Abstract. This paper surveys the results of an extended research activity concerning the effects of radio frequency interference (RFI) on integrated circuits (IC's). Initially, the possible injection methods for conducted and radiated interference are presented, discussing their applicability and limitations. Then, the basic results of the susceptibility analysis of operational amplifiers and smart power integrated circuits are briefly discussed. Finally, experimental data describing some effects of RFI direct injection on switch mode power supply integrated controllers are presented.

I. Introduction

Analog and digital integrated circuits are widely used in equipment operating in electromagnetic polluted environments such as in automotive, aeronautic and industrial systems. The power supplies distribution and signal communication among electronic modules of the equipment are typically realized by cables that couple with environmental electromagnetic fields: cables behave as receiving antennas and collect interference that are superimposed on system signals. In case of modules composed of printed circuit boards (PCB's) with smaller dimensions than the interference wavelength, it can be assumed that the electromagnetic interference collected by PCB tracks and by integrated circuits package frames is negligible if compared to that collected by connecting cables. This paper presents a survey of the results of an extended research activity concerning the effects of conducted RFI on IC's. Initially, some of the possible injection methods for conducted and also radiated interference, that allow to perform the characterization of IC's immunity to EMI, are presented. The workbench Faraday cage method, the direct injection method and the TEM cell method are considered, discussing their applicability and limitations. Then, the susceptibility analysis of some widely used integrated circuits is presented, beginning with operational amplifiers. Smart power IC's immunity is successively discussed. Finally, the paper presents the experimental data describing some effects of conducted EMI on a small group of widely used switch mode power supply integrated controllers.

II. IC's Immunity Test Methods

The characterization of an integrated circuit in terms of susceptibility to conducted RF interference is usually performed referring to two different criteria.

One criterion requires the measurement of RF interference amplitude at which device under test (DUT) failures occur. The measurement has to be performed with continuous wave interference (CW) at several frequencies. Another criterion consists in the measurement of the frequency ranges in which DUT failures occur, if constant amplitude of the interfering signal is taken.

The second criterion comes from those usually adopted in verifying the compliance of electric and/or electronic equipment to EMC standards, while the first one makes possible the evaluation of the DUT functional limits in the presence of interference.

This section presents some possible techniques for the measurement of integrated circuit susceptibility to conducted and radiated RF interference. In particular, the Workbench Faraday Cage method, the direct injection method and the TEM cell method are described.

A. The Workbench Faraday Cage Method

The Workbench Faraday Cage (WBFC) method was proposed to perform immunity and emission tests of IC's or small electronic modules in the frequency range between 150 kHz and 1GHz [1 - 2]. The basic concept of this method is taken from the European standard EN61000-4-6 that regards the immunity of electronic equipment to common mode conducted RF interference [3]. In this case interference is coupled to the equipment under test (EUT) via coupling de-coupling networks (CDNs).

The WBFC method is based on the hypothesis that IC's are mainly reached by interference collected by cables that

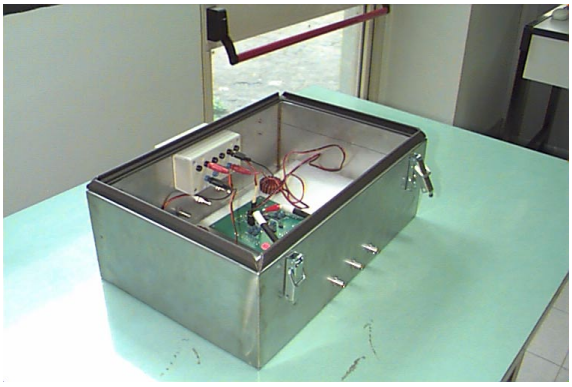

Fig.1 - Photo of the Work Bench Faraday Cage.

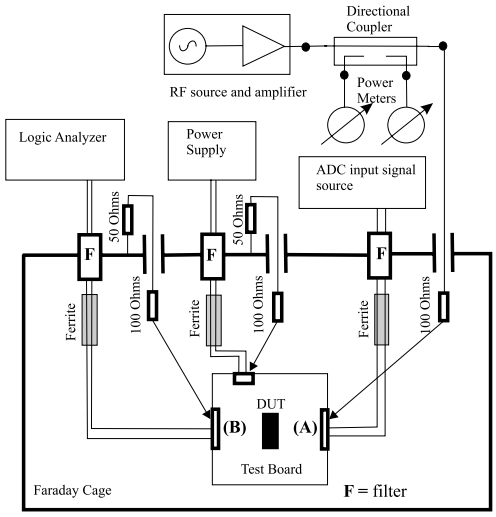

Fig. 2 - Schematic representation of the WBFC for immunity tests.

are directly connected to the PCB. A bundle of cables, i.e. a receiving antenna connected to the DUT, in the WBFC is replaced by the series of an interference source and a radiation resistance $R_g = 150\ \Omega$. In actual equipment the radiation resistance depends on cables lengths and geometry, but its average value is about $150\ \Omega$ with a standard deviation of 7 dB. A test board, with the DUT soldered on, is inserted into a Faraday cage. Immunity measurements are performed into a Faraday cage because most of actual electronic systems require a metal can, in order to have thermal and mechanical stresses reduced. Furthermore, the Faraday cage allows immunity tests with interference confined to the DUT surroundings (see Fig. 1), and the interference with operations of other electronic equipment close to the WBFC can be avoided.

Fig. 2 shows the test setup of the WBFC method. Common mode filters realize links among DUT, power supply and auxiliary instruments in the test bench. Each filter is composed of a π cell that is inserted through a wall of the cage, in series with common mode inductors, that are

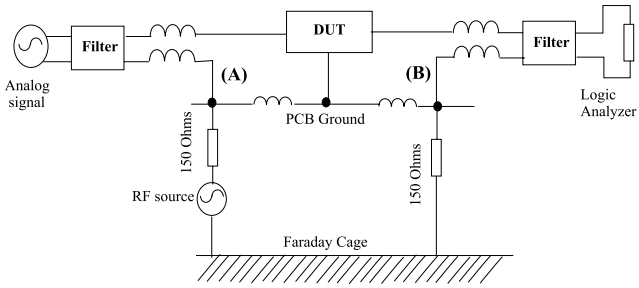

Fig. 3 - Description of the test bench in the case of common mode interference applied to the node of common mode injection (A).

realized by a couple of wires wrapped on a NiZn ferrite core ($\mu_r > 1000$). The common mode resistors $R_{c1} = R_{c2} = 150\ \Omega$, shown in Fig. 3, represent the radiation resistance of two different bundles respectively connected to the node (A) and (B). Since bundles connected to each module come from different directions, the RF voltages induced to bundle terminals are different in amplitude.

This is the reason to inject interference in one common mode node at a time, as shown in Fig.3 [4]. In this test bench, the immunity of IC's to common mode conducted RF interference strongly depends on the PCB design. Since the PCB translates the injected common mode interference in voltages at the DUT pins, it is able to hide or highlight the DUT immunity to RF. Furthermore, the test setup of Fig. 2 shows some weakness for interference frequencies higher than 300 MHz. In fact, the considerations in [4] are valid until the dimensions of the Faraday cage and those of objects placed into the metal cage are negligible if compared with interference wavelength. The Faraday cage, with dimensions *length* = 0.5 m, *width* = 0.35 m, *height* = 0.15 m, behaves as resonant cavity at the frequencies $f_{rn} = 300*n$ [MHz], $f_{rm} = 430*m$ [MHz] with $m,n \in N$.

However, the WBFC method simulates quite well actual applications because it allows performing immunity test of an integrated circuit in the case of overlapping between the spectrum of interfering and system signals.

B. The direct injection method

In the direct injection method the interference is directly applied between a pin of the DUT and the IC ground pin (Fig. 4). The device is soldered on a test board and a bias tee circuit gives, in a DUT pin, the interference superimposed on a system signal. IC immunity test results do not depend on the design of the test board. Each pin of the DUT is characterized in terms of IC immunity to RF power collected by a receiving antenna connected to that pin. A radiation resistance of 50 Ω and a RF voltage source composes the equivalent circuit of the receiving antenna. Amplitude of the RF voltage source is derived from

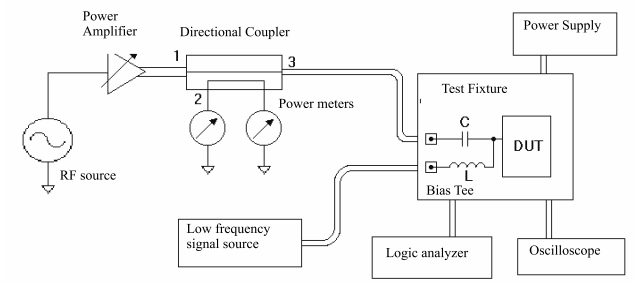

Fig. 4 - Test bench for direct injection.

measurements of the RF available power, which is required to observe failures in the DUT operations.

This method can be used successfully for narrow band interference and in the case of the system signals with spectral components separated from those of the disturbance. For instance, it does not allow the injection of interference on digital signals.

C. The TEM cell method

In previous methods, system signals have been corrupted by conducted RF interference. The method of the TEM cell makes possible the evaluation of IC's immunity to radiated electromagnetic field. TEM cell characteristics and the test board design rules are reported in [5], where the test setup and the procedure to evaluate IC's electromagnetic emission is reported. The TEM cell shows an upper opening with dimensions suitable for the test board in which the DUT can be inserted.

The DUT is placed on the layer that works as a part of the TEM cell walls (see Fig. 5), and it is connected to the other layers by vias. The ground layer realizes a good contact to the wall of the TEM cell, all along the border of the opening. In order to guarantee the communication of the DUT with components and auxiliary instruments, vias interconnections cannot be filtered; therefore the interference generated into the TEM cell will appear outside, in the TEM cell surroundings too.

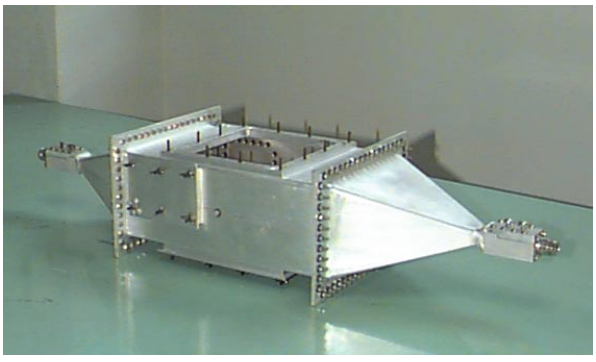

Fig. 5 - TEM cell.

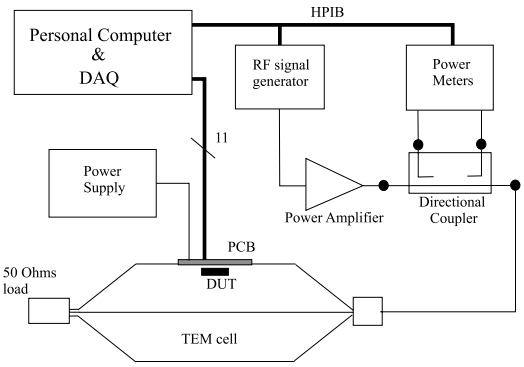

Fig. 6 - Test setup of the TEM cell method.

The immunity tests have to be performed by using a test bench like that shown in Fig. 6. By using the TEM cell described in [5], measurement can be performed in the frequency range 150 kHz - 1 GHz.

The automatic test bench shown in Fig.6 allows the control of DUT and auxiliary instrumentation operations. The amplitude of electric field is stepped until DUT failure occurs, while the interference amplitude, frequency and the DUT status are picked-up [6].

III. Susceptibility of Analog IC's: Operational Amplifiers.

Analog circuits are particularly susceptible to RFI, as they lack the regenerative effect which is typical of digital circuits. Among analog circuits, operational amplifiers (opamps) are extremely susceptible to RF disturbances. They demodulate RFI added on nominal input signals and so the nominal output signal is corrupted by in-band interference. In particular, the presence of CW interference generates an output offset voltage.

This opamp behavior was originally observed in aeronautic electronic systems and subsequently studied performing immunity tests on commercial opamps. In particular, measurements of the output offset voltage induced by RFI conveyed on the input terminals of several feedback opamps were performed varying interference frequency and amplitude [7]. These experimental characterizations are useful in the design of electromagnetic interference (EMI) filters.

This behaviour has been studied by time domain [8 - 10] and frequency domain (harmonic balance) [11] computer simulations: several efforts have been expended on research in order to derive both RFI-oriented numerical models of active devices and opamp macromodels intended to reduce computer simulation time. Although these models allow one to predict efficiently and accurately the RFI-induced offset in opamps, they do not grant a relationship with circuit parameters and parasitics and so they cannot be directly applied to derive design criteria.

More recently, it has been shown that the differential input stage of common operational amplifiers is responsible of the generation of such a DC output offset voltage because it behaves like a mixer, whose input signals are the common mode and the differential mode RF input voltages [12 - 13].

IV. Immunity Considerations on Smartpower IC's

Nowadays, smart power technologies [1] allow the design and realization of complex IC's composed of analog, digital and power blocks (see Fig. 7). In many cases a complete electronic module is collapsed into an IC. In these devices, interference reach active and passive integrated components by metal interconnection routed on the silicon surface, or through parasitic paths. Since 50 - 70 % of a smart power device area consists of power transistors, an effective capacitive coupling with silicon substrate is realized and RF interference, collected by cables, is injected directly into the substrate through the power-transistors isolation diodes. Unfortunately, silicon substrate does not behave as a common ground plane and a part of the interference injected through power transistors reaches other components realized in the same die through reverse polarized p-n junctions.

For instance, the isolation of a lateral pnp transistor is obtained controlling n-type base region potential (see Fig. 8a). If a common emitter configuration is considered, the interference coming from the substrate is directly applied to the base and emitter junction (see Fig. 8b). In the presence of RF interference applied on the transistor b-e junction, emitter current crowding and rectification phenomena appear [14], hence the device quiescent operating point is modified. Furthermore, if a pnp transistor is used in a gain stage, then the base of the device has to be carefully shielded, or connected to a low impedance node. Otherwise the interference in the substrate will be amplified by the gain of the circuit.

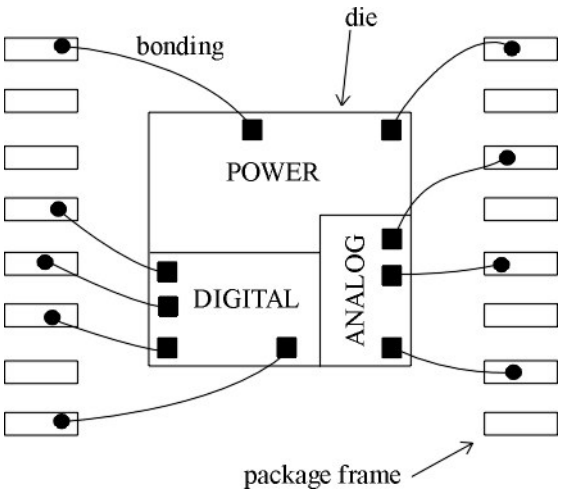

Fig. 7 - Top view of a smart power device.

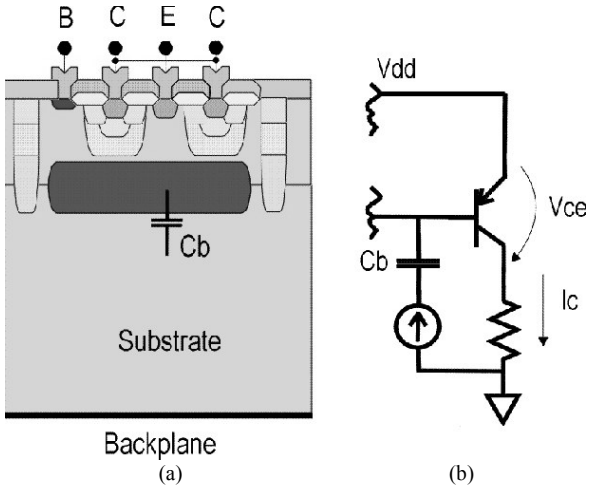

Fig. 8 - (a) Lateral PNP bipolar transistor cross-section. (b) PNP transistor in common emitter configuration with substrate interference (current source) applied to the base terminal by the parasitic capacitor Cb.

A vertical bipolar transistor is instead coupled to the substrate by a reverse polarized diode connected to its collector. In the case of a npn transistor polarized in the active region, interference superimposed on the collector-emitter voltage does not modify the transistor DC quiescent operating point. Despite the good behavior of npn vertical transistors, RF interference injected into the substrate through power-transistor isolation diodes, and collected through vertical-transistor isolation diodes is superimposed on signals of the circuits realized in the die surface. Therefore, interference could induce failures of the overall integrated system.

Finally, MOS transistors show high susceptibility to substrate interference since they exhibit a severe form of substrate interaction due to the body effect [15].

V. Example of RFI Effects on DC/DC Converter Integrated Controllers

This section describes the effects of EMI injection on some very popular dc/dc converter integrated controllers, namely those belonging to the UC3845 family. Four pin to pin compatible implementations of the same device from different manufactures have been taken into account (in the following they will be denoted by a progressive number IC1÷IC4). A suitable PCB was developed to allow replicable injection of RF signals into the more sensitive IC pins. The structure of the implemented circuit is shown in Fig. 9. As can be seen, the minimum number of components is used to get a stable operating point for the device. A switching frequency of 60 kHz was selected and a typical peak current mode configuration was considered, where the current feedback signal is emulated by sending a suitable portion of the synchronizing ramp, obtained by means of the voltage divider R_3-R_4, to the I_{sense} pin. The error amplifier is

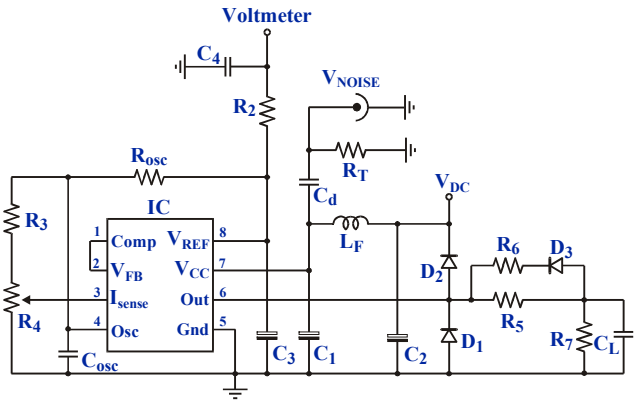

Fig. 9 - Schematic of the measurement setup

connected as a voltage follower, thus allowing duty-cycle regulation. In all the tests discussed in the following, the duty-cycle set-point was fixed to 0.25. A suitable capacitor C_L emulates the power switch gate capacitance and synthesizes the IC load.

In order to properly inject the RF signal, decoupling networks were implemented using suitable inductors and capacitors. Attention was put on filter inductor L_F which is actually a series connection of different inductors in order to guarantee a minimum impedance of 300 Ω in all the measurement frequency range. The RF signal was injected through capacitor C_d into the V_{CC} pin to emulate the effect of RF noise pick up through the dc supply voltage network, usually fed by a suitable winding of the dc/dc converter power stage. It is worth noting that the presence of the electrolytic filter capacitor C_1 at V_{cc} pin, which is necessary to maintain a low impedance supply voltage at DC, does not attenuate the injected noise, because its impedance at the noise frequencies is high enough, being dominated by its equivalent series inductance. This was verified by measuring the injected noise level at the V_{cc} pin of the IC.

The amplitude of the sinusoidal injected RF signal, as set on the RF generator, is 105 dBµV and its frequency has been varied from 100 MHz to 1 GHz, but no significant effect was registered above 700 MHz. Fig. 10 describes the effect of the RF noise on the internal voltage reference, showing its relative deviation with respect to the nominal 5 V value (note that it is a negative value). It is interesting to note that the different implementations of the same device determine a different sensitivity to the RF noise. In particular, while the maximum effect is concentrated on the 200 MHz frequency range for all the IC's, the amount of voltage error is quite variable, ranging from 0.025% up to 0.325%. Unfortunately, since no layout information is available, it is not possible to justify the different response provided by the different IC's. It is worth noting the absolute amplitude of the voltage reference deviation is in any case very small and can be revealed only by means of a high precision voltmeter. Beside this DC shift, the reference voltage shows also a residual noise at the same frequency of the injected signal.

Fig. 11, instead, describes the effect of the same RF noise injection on the oscillation frequency. As can be seen, a significant relative deviation from the nominal value was measured. Here the different IC's present a different sensitivity in frequency. The maximum relative frequency deviation amounts to 1.2%. It is worth noting that tests were performed also with a separate voltage supply for the oscillator circuit, so as to make sure that the observed effects are generated by some process taking place inside the IC and not by direct coupling of the RF signal with the oscillator through the polarization network. The frequency deviation was revealed by means of a spectrum analyzer.

Finally, measurements were performed on a different PCB which allowed to inject the RF signal on the error amplifier non inverting input pin. In this case, no significant effects were revealed on the operating point (practically no duty-cycle modulation).

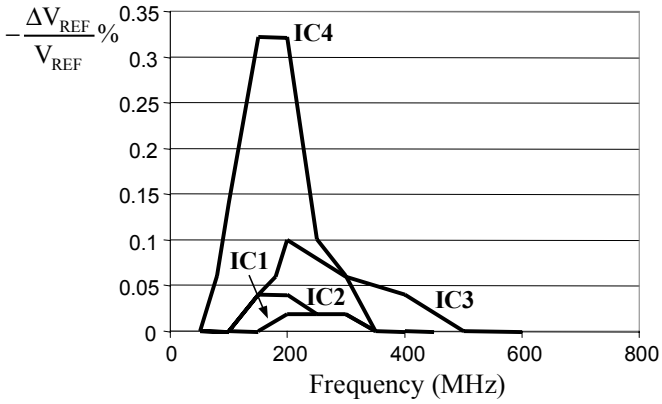

Fig. 10 - Reference voltage relative deviation as a function of noise frequency (V_{NOISE} = 105dBµV)

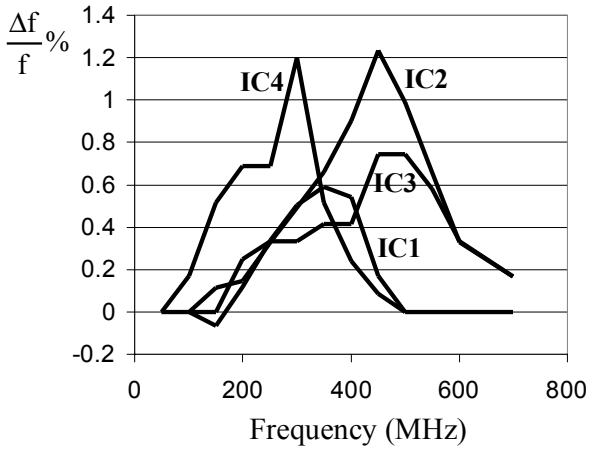

Fig. 11 - Oscillator frequency relative deviation as a function of noise frequency(V_{NOISE} = 105dBµV)

VI. CONCLUSIONS

This paper surveys the results of an extended research activity concerning the effects of RFI on IC's. Initially, the possible injection methods for conducted and radiated interference, that allow the characterization of IC's immunity to EMI to be performed, are presented. Three methods are taken into account, namely the workbench Faraday cage (WBFC) method, the direct injection method and the TEM cell method. Applicability and basic limitations of each method are briefly discussed. Some of the results of the analysis of EMI effects on operational amplifiers and smart power IC's are then presented. In particular, the EMI induced output voltage offset generation in operational amplifiers is addressed. As far as smart power IC's are concerned, the basic substrate effects, responsible of EMI transmission among the different parts of the chip are described. The paper is finally concluded by the presentation of experimental data, describing some effects of conducted EMI on a small group of widely used switch mode power supply integrated controllers.

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