

Susceptibility of Integrated Circuits to RFI: Analysis of PWM Current-Mode Controllers for SMPS

M. Citron, M. Corradin, S. Buso, G. Spiazzi

*Dept. of Information Engineering - University of Padova
Via Gradenigo 6/b, 35131 Padova – ITALY
Phone: +39-049-827.7573
Email: massimiliano.citron@unipd.it*

F. Fiori

*Electronic Department - Polytechnic of Torino
c.so Duca degli Abruzzi 24, I-10129 Torino – ITALY
Phone: +39-011-5644141
E-mail: fiori@eln.polito.it*

Abstract - This paper deals with the analysis of the effects of radio frequency conducted interfering signals (RFI) on integrated circuits (IC's). After reviewing the basic results of the susceptibility analysis of operational amplifiers and smart power integrated circuits, the behavior of several pin-to-pin compatible control IC's for PWM current-mode switching power supplies (SMPS) has been tested in the presence of both continuous wave interfering signals (CW) as well as of pulsed noise signals (underground condition). The tested ICs were selected between some common models available on the market. The variations of the primary functional parameters (inner voltage reference, switching frequency, etc.) are evaluated in different test conditions. The paper gives a comparative view of the results, focusing on the key macroscopic effects.

I. INTRODUCTION

Analog and digital integrated circuits are widely used in equipment operating in environments affected by a high degree of electromagnetic pollution, such as automotive, aeronautic and industrial systems. In these situations, the connection cables between different electronic systems represent an efficient coupling mechanism (antennas) with radio frequency interference (RFI), thus transforming the disturbing electromagnetic fields into noise signals superimposed on system signals. On the other hand, in case of modules composed of printed circuit boards (PCB's) with smaller dimensions than the interference wavelength, it can be assumed that the electromagnetic interference collected by PCB tracks and by integrated circuits package frames is negligible if compared to that collected by connecting cables.

No matter the coupling mechanism is, the RF signals enter the integrated circuits mainly through their external pins, and cause different malfunctions and performance degradation. RFI effects on active devices like diodes, bipolar and field effect transistors have been widely studied in the last 30 years, showing rectification phenomena [1,2], dc and ac current crowding in the emitter region of BJT's [3], etc. All these effects are enhanced into integrated circuits, due to the high number of unintentionally created parasitic components, which makes very difficult the analysis of RFI propagation inside these devices. Moreover, since many active devices share the same substrate, an effective coupling path between different subcircuits through the substrate parasitic capacitance is created. Such coupling mechanism can become dominant in smart power IC's, in which a power device, occupying a

large silicon area, exists [4]. In these cases, RFI can also be internally created by the power device operation, especially in switching applications, due to the high di/dt and dv/dt produced.

This paper reviews briefly the results of studies on susceptibility of operational amplifiers first (section II), and general aspects regarding smart power integrated circuits susceptibility (section III). In sections IV and V a comparative study on six pin-to-pin compatible PWM current-mode ICs (of 3845 family) is reported, in which the variations of the primary functional parameters in conditions of different frequency and amplitude interfering signals were measured. It is worth noting that the experimental set-up does not refer to any particular standard and thus only allows to compare the behavior of the considered ICs in the same conditions. The tests are performed with RFI in a frequency range of 100÷800 MHz at a fixed noise signal amplitude of 115 dB μ V.

Besides the use of continuous wave (CW) RFI, tests were done to compare the IC's behavior in the presence of an underground condition occurring at the output driver pin, normally connected to an external MOSFET power switch. This condition can occur during the switch turn off instant, and is caused by the presence of a parasitic inductance in the gate drive circuit, or can be due to a fast falling voltage transient occurring at the drain, e.g. in DCM operation. In fact, the falling drain to source voltage can couple capacitively a current into the gate circuit, possibly turning on the normally reverse biased isolation pn-junctions formed by the substrate of the IC and the different circuit wells (that's why it is recommended to connect Schottky clamping diodes very near the IC output).

II. SUSCEPTIBILITY OF ANALOG IC'S: OPERATIONAL AMPLIFIERS

Analog circuits are particularly susceptible to RFI, as they lack the regenerative effect which is typical of digital circuits. Among analog circuits, operational amplifiers (opamps) are extremely susceptible to RF disturbances. They demodulate RFI added on nominal input signals and so the nominal output signal is corrupted by in-band interference. In particular, the presence of CW interference generates an output offset voltage.

This opamp behavior was originally observed in aeronautic electronic systems and subsequently studied performing immunity tests on commercial ICs. In

particular, measurements of the output offset voltage induced by RFI conveyed on the input terminals of several feedback opamps were performed varying interference frequency and amplitude [5]. These experimental characterizations are useful in the design of electromagnetic interference (EMI) filters.

This behavior has been studied by time domain [6-8] and frequency domain (harmonic balance) [9] computer simulations: several efforts have been expended on research in order to derive both RFI-oriented numerical models of active devices and opamp macromodels intended to reduce computer simulation time. Although these models allow one to predict efficiently and accurately the RFI-induced offset in opamps, they do not grant a relationship with circuit parameters and parasitics and so they cannot be directly applied to derive design criteria.

More recently, it has been shown that the differential input stage of common MOS operational amplifiers is responsible for the generation of such a DC output offset voltage because it behaves like a mixer, whose input signals are the common mode and the differential mode RF input voltages [10,11]. These papers demonstrate that the RF applied to the opamp input terminals produces a corresponding RF modulation of the differential pair bias current, due to the finite admittance of the employed current source, which is particularly high at high frequencies because of its capacitive component. This component is essentially due to the well-to-ground parasitic junction capacitance which is present if the input transistors are designed in a well, as it is usually done in order to avoid the body effect.

III. IMMUNITY CONSIDERATIONS ON SMART POWER IC'S

Nowadays, smart power technologies allow the design and realization of complex IC's composed of analog, digital and power blocks (see Fig. 1). In many cases a complete electronic module is collapsed into an IC. In these devices, interference reach active and passive integrated components by metal interconnection routed on the silicon surface, or through parasitic paths. Since 50-70% of a smart power device area consists of power transistors, an effective capacitive coupling with silicon substrate is realized and RF interference, collected by cables, is injected directly into the substrate through the power transistors isolation diodes. Unfortunately, silicon substrate does not behave as a common ground plane and a part of the interference injected through power transistors reaches other components realized in the same die through reverse polarized p-n junctions.

For instance, the isolation of a lateral pnp transistor is obtained controlling n-type base region potential (see Fig. 2a). If a common emitter configuration is considered, the interference coming from the substrate is directly applied to the base and emitter junction (see Fig. 2b). In the presence of RF interference applied on the transistor b-e junction, emitter current crowding and rectification phenomena appear [1,3,12], hence the device quiescent operating point is modified. Furthermore, if a pnp transistor is used in a gain stage, then the base of the device has to be carefully shielded, or connected to a low impedance node. Otherwise

the interference in the substrate will be amplified by the gain of the circuit.

A vertical bipolar transistor is instead coupled to the substrate by a reverse polarized diode connected to its collector. In the case of a npn transistor polarized in the active region, interference superimposed on the collector-emitter voltage does not modify the transistor DC quiescent operating point. Despite the good behavior of npn vertical transistors, RF interference injected into the substrate through power-transistor isolation diodes, and collected through vertical-transistor isolation diodes is superimposed on signals of the circuits realized in the die surface. Therefore, interference could induce failures of the overall integrated system.

Finally, MOS transistors show high susceptibility to substrate interference since they exhibit a severe form of substrate interaction due to the body effect. In [4], the effectiveness of shielding substrate contacts in the case of a test smart power IC composed by a power transistor and a bandgap circuit has been evaluated in the case of a CW RF signal applied to the power MOS drain contact.

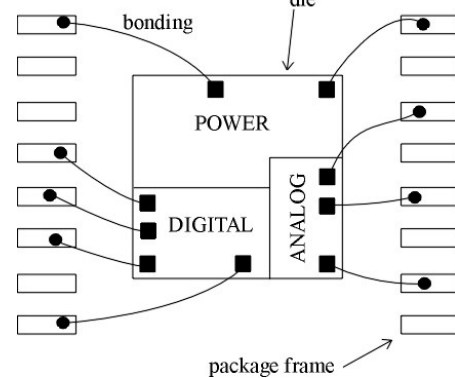


Fig. 1 - Top view of a smart power device

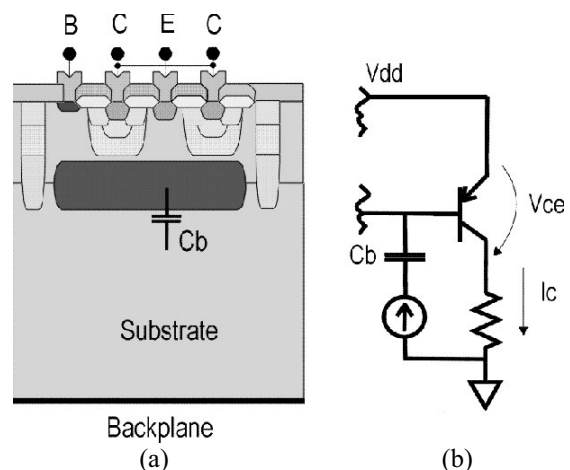


Fig. 2 - (a) Lateral PNP bipolar transistor cross-section. (b) PNP transistor in common emitter configuration with substrate interference (current source) applied to the base terminal by the parasitic capacitor C_b

IV. SUSCEPTIBILITY OF PWM CURRENT-MODE CONTROLLERS: EXPERIMENTAL SET-UP

In this section the susceptibility to RF disturbances of several popular PWM current-mode controllers (3845 family) for SMPS was evaluated.

Fig.3 shows the simplified block diagram of the IC. As we can see, it consists of a local oscillator, voltage reference, operational amplifier, comparator and output driver, plus some logic circuitry to ensure safe operation of the external power device. The test circuit board is designed to set the IC in a stable operating point, similar to the real operating conditions. Two points of injection for the RFI were considered, namely the supply voltage pin and the inverting input pin of the error amplifier. These are considered to be the preferred noise inputs in any practical application, since they are normally connected to the switching converter power stage. Fig. 4 shows the test circuit for the V_{CC} pin noise injection. In order to simulate a current-mode operation, the voltage at pin Isense must be a triangular waveform, synchronised with the IC internal clock. In the test set-up, this signal is derived from the oscillator ramp: changing the value of the resistor divider allows control of the duty-cycle. C_1 and L are responsible for the AC-DC separation. To ensure enough blocking capability in a broad frequency range (i.e. 100+800 MHz), L is formed by a series of six inductances with decreasing value (three with ferrite's core, three with ferrite's ring), so that a minimum impedance of 300Ω is ensured in the whole frequency range. The IC supply voltage is obtained with a series of batteries, to avoid undesired RFI couplings

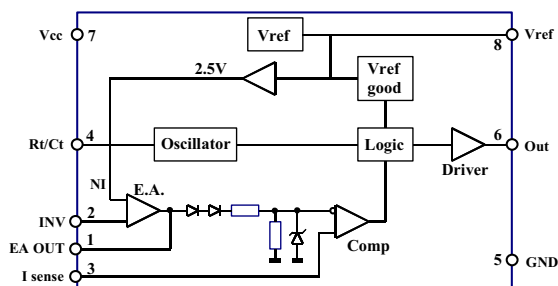


Fig. 3 - Simplified block diagram of the 3845 family ICs

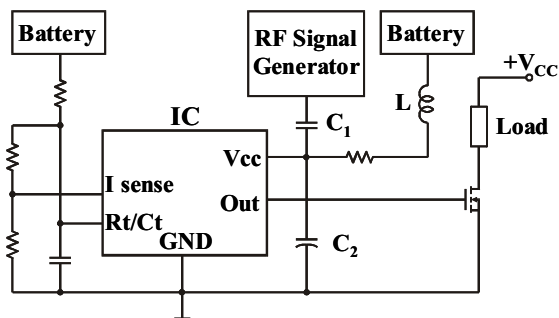


Fig. 4 - Schematic experimental set-up for RFI injection to V_{CC} pin

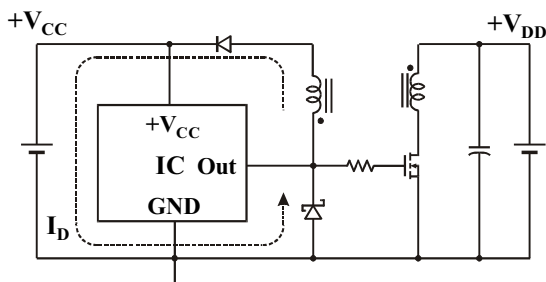


Fig. 5 - Schematic of the experimental set-up for generation of the underground condition

that could occur with an external power supply connected to the line grid. C_2 is a quite high value electrolytic capacitor necessary to filter the current pulses drawn by the IC in correspondence of the output driver commutations. We verified that, because of its equivalent series inductance, C_2 behaves as a high impedance circuit at RF, so that the noise voltage coupled to the supply pin was verified for all the devices to be only some $\text{dB}\mu\text{V}$ ($\leq 8 \text{ dB}\mu\text{V}$) below the nominal injected level. The output of the IC is connected to a power MOSFET loaded by a clamped inductance to simulate real life conditions. By shorting pin 1 and pin 2 (see Fig. 3), the error amplifier is set in a unity-gain buffer configuration.

Fig. 5 shows schematically the layout used for generation of the underground condition, in which the IC is still working on a stable operating point (the components for this purpose are the same as the previous case). Since it is common practice to connect a Schottky diode in parallel with the output to prevent the development of a high negative voltage spike, we also included it in the test circuit. In this circuit we use the switching action of the power MOSFET to store energy in a magnetic core. During the off state of the MOSFET this energy (like in a flyback converter) is sent to the secondary side of the transformer, forcing a current (i_D in Fig. 5) to circulate through the Schottky diode and the IC isolating pn-junctions. Adjusting the value of V_{DD} it is possible to control the value of i_D and, consequently, modulate the underground amplitude and duration.

V. EXPERIMENTAL RESULTS

We tested six different ICs. Thanks to their pin to pin compatibility, the test board was always the same. This permits to put into evidence the peculiar differences between their responses when submitted to the same operating and disturbed conditions. As explained before, two different injection points, the inverting input of the error amplifier and the voltage supply pin, were chosen. The main macroscopic effect in the former case, was a moderate frequency shift in the IC ramp. Possibly, the input capacitance of the IC shunted almost all the RF signal.

For injection into the supply pin, more interesting results were obtained. Fig. 6 presents the frequency deviation (nominal 32 kHz) for five models named from A to E. This fictitious names will correspond to the same components throughout the figures. Fig. 6 reveals that for this level of interference, an average deviation of +10% with respect to the nominal frequency can be obtained. For a specimen (B), almost +18% is reached. Measurements were performed at a lower noise signal level (not reported here) from which an almost perfect proportionality can be inferred between RF level and measured frequency deviation. Fig. 7 shows absolute measured duty-cycle deviation, again for 115dB μV . From a nominal 30%, almost all ICs reach 3% of shift, i.e. the induced duty-cycle becomes 33%. In Fig. 8 the DC-shift of the inner voltage reference can be appreciated. Here component C shows a maximum decrease of 300mV with respect to a nominal value of 5.1V.

The result for the sixth component (denoted component F) was deliberately reported in another figure. Fig. 9 isolates the DC shift for component F, which grows as high as -3.5V . The latter result does not appear in the previous graphics because at $115\text{dB}\mu\text{V}$ of injected signal the voltage reference collapses, falling to the point (close to the internal 2.5V reference) at which the switching action stops. This is due to the intervention of block "Vref good" shown in Fig. 3.

As far as the underground condition is concerned, the results obtained with the circuit in Fig. 5 indicate that the

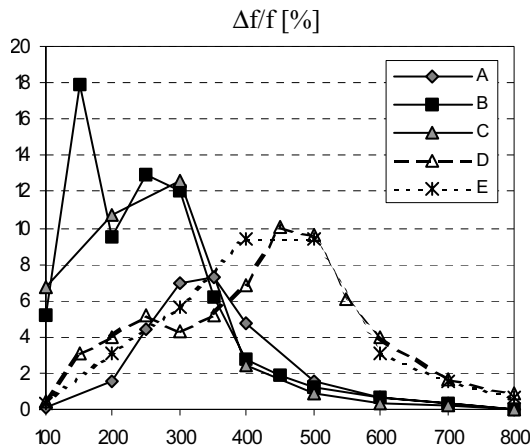


Fig. 6 – Frequency shift induced by RFI on Vcc pin. Signal level = $115\text{dB}\mu\text{V}$. Nominal duty-cycle = 30%

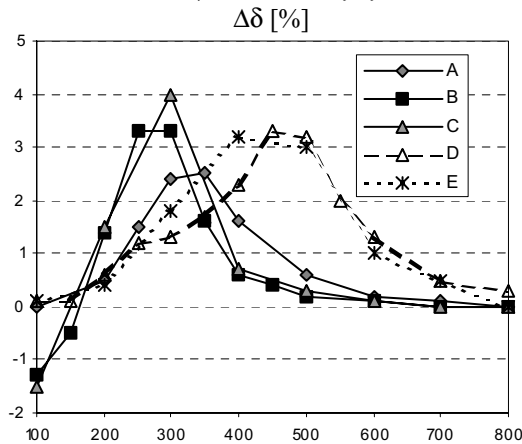


Fig. 7 – Duty-cycle shift induced by RFI on Vcc pin. Signal level = $115\text{dB}\mu\text{V}$. Nominal duty-cycle = 30%

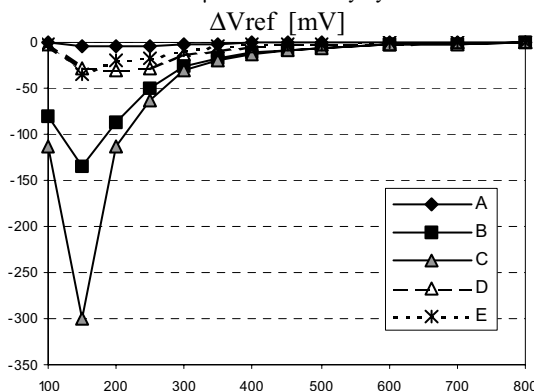


Fig. 8 – DC shift induced by RFI on Vcc pin. Signal level = $115\text{dB}\mu\text{V}$. Nominal duty-cycle = 30%. Nominal voltage = 5.1V

first effect appears in the ramp generation block. This holds for all the ICs, except F and A. The peak value of the induced current i_D into the Schottky diode was taken as a quality-reference, since it determines the amplitude and duration of the underground condition at the IC output. In Fig. 10 it can be seen that, for a certain level of the current i_D , the ramp signal begins to show negative spikes during its rising edge. If the i_D current is made higher (Fig. 11), in the correspondence of the underground condition, the ramp voltage collapses to zero and then starts to rise again, thus producing a step change in the switching period and duty-cycle. The other pins do not show any change in their nominal behavior. ICs B, C, D and E behave in the same manner, differing only for the threshold current-peak i_D at which the malfunction begins to appear: B and C have a threshold current level of 50mA , D and E of 500mA . The A-type IC presents deviations from its operating point only for a current level i_D of 2A , thus revealing a particularly high immunity to the underground condition. Anyway, at this high current level, a chaotic behavior appears at its output (Fig. 12): it seems that the IC is trying to switch on the MOSFET, supplying the i_D current and pushing the output voltage toward the high-state.

The F-type IC shows again a particular behavior (Fig. 13): for a peak-current i_D of 900mA , the output of the error amplifier collapses forcing the output pin into the low state where it remains for more than 2 ms. It then starts to rise very slowly. The output starts to drive the MOSFET again, until a critical duty-cycle is reached and another reset occurs. The output of the error amplifier is directly connected to the inverting input, so apparently there is not justification for such a long time-constant. For other considered ICs (3843 family, sixteen pins), not discussed here, a low value of the current-peak i_D , which triggers the malfunction, was found ($\sim 10\text{mA}$). Such a low current is normally able to occur in standard operating circuits.

VI. CONCLUSIONS

It is shown that RF interferences superimposed on nominal IC's signals can have a dramatic impact in their performance. Out-of-band interfering signals are demodulated by non linear characteristics of active devices thus producing in-band signals which affect their behavior in a very complex manner. The presence of a high number of parasitic components inside ICs increases the

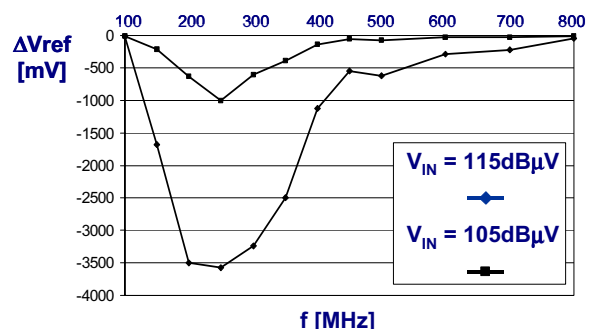


Fig. 9 – DC shift induced by RFI on Vcc pin for component F. Nominal duty-cycle = 30%. Nominal voltage = 5.1V

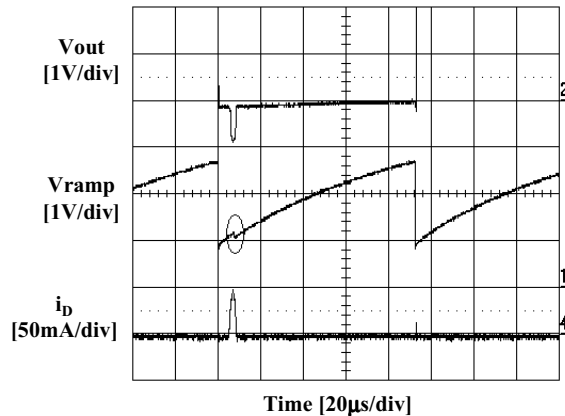


Fig. 10 – Effect of underground condition at output pin: Vramp begins to show a discontinuity. From top to bottom: output pin voltage, ramp voltage, secondary side current pulse

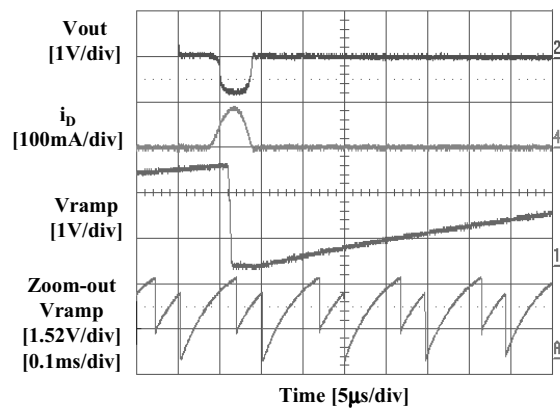


Fig. 11 – Effect of underground condition at output pin: Vramp resets to zero (B and C type). From top to bottom: output pin voltage; secondary side current pulse; ramp voltage; zoom-out track of the ramp voltage; (a toggle flip flop sets the switching frequency to half the ramp frequency)

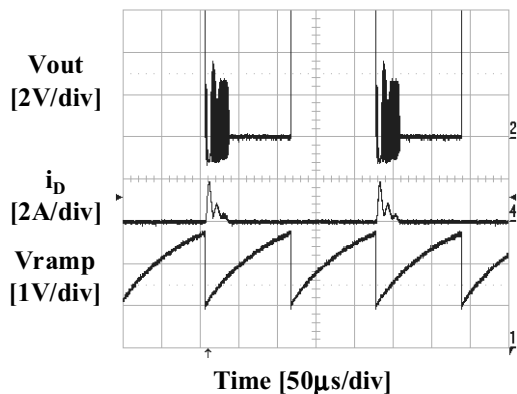


Fig. 12 – Effect of underground condition at output pin: the A-type output for an i_D current-peak of nearly 2A. From top to bottom: output pin voltage, secondary side current pulse, ramp voltage

complexity of the analysis.

Tests performed on commercial PWM Current-Mode Controllers for SMPS, in the presence of both CW RF signals on supply pin and of underground condition at output pin, showed degradation of their nominal performance, in terms of switching frequency, duty-cycle and voltage reference variations. Moreover, the degree of susceptibility changes significantly between different

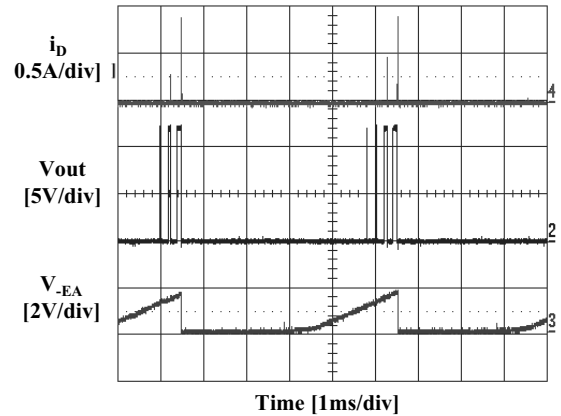


Fig. 13 – Effect of underground condition at output pin: the F-type presents a blackout in the error-amplifier block that disables the circuit for a long time. From top to bottom: secondary side current pulse, output pin voltage, error amplifier inverting input voltage

manufacturers, thus revealing that a correct design can be effective in increasing ICs robustness against RFI.

REFERENCES

- [1] Robert E. Richardson, Vincent G. Puglielli, Robert A. Amadori, "Microwave Interference Effect in Bipolar Transistor," IEEE Trans. on Electromagnetic Compatibility, Vol. 17, No. 4, November, 1975, pp. 261-219.
- [2] M. L. Forcier, R. E. Richardson, "Microwave-Rectification RFI Response in Field-Effect Transistors," IEEE Trans. on Electromagnetic Compatibility, Vol. 21, No. 4, November, 1979, pp. 312-315.
- [3] Robert E. Richardson, "Quiescent Operating Point Shift in Bipolar Transistors with AC Excitation," IEEE Journal of Solid-State Circuits, Vol. 14, No. 6, December, 1979, pp.1087-1094.
- [4] F. Fiori, "Prediction of RF interference effects in smart power integrated circuits," IEEE Int. Symp on Electromagnetic Compatibility, Washington D.C., USA, Aug. 21-25, 2000, pp. 345-347.
- [5] A. Engel, H. Astrain, J. Cagle, S. Ledford, M. Mahalingam, "Integrated Circuit electromagnetic susceptibility Handbook", Tech. Rep. MDC E1929, McDonnell Douglas Astronautic Company, St. Louis, MO, 1978.
- [6] J.G. Tront, J.J. Whalen and C.E. Larson, "Computer aided analysis of RFI effect in operational amplifiers", vol. EMC-21, pp. 297-306, Nov.1979.
- [7] G. K. C. Chen and J.J. Whalen, "Macromodel prediction for EMI in bipolar operational amplifiers", IEEE Trans. On Electromagnetic Compatibility, vol. EMC-22, pp. 262-265, Nov.1980.
- [8] S. Graffi, G. Masetti, and D. Golzio, "New macromodels and measurements for the analysis of EMI effects in 741 opamp circuit," IEEE Trans. on Electromagnetic Compatibility, vol. EMC-21, p.25-34, Feb. 1991.
- [9] Y. Hattori, T. Kato, H. Hagashi, H. Tadano and H. Nagase "Harmonic Balance Simulation of RF Injection Effects on Analog Circuits," IEEE Trans. on Electromagnetic Compatibility, vol. 40, pp. 120-126, May. 1998.
- [10] F. Fiori, P.S.Crovetti, "Nonlinear effects of RF interference in MOS operational amplifier," IEEE Int. Symp on Electronics, Circuits and System (ICECS), Malta, Sept. 2-5, 2001, pp. 201-204.
- [11] F. Fiori, P.S. Crovetti, "Nonlinear effects of RF interference in operational amplifiers," IEEE Trans. on Circuit and System, part I, vol. 49, no. 3, pp. 1-6 Mar. 2002.
- [12] F. Fiori, V.Pozzolo, "Modified Gummel Poon Model for Susceptibility Prediction," IEEE Trans. on Electromagnetic Compatibility, vol. 42, no.2, pp. 206-213, May 2000.