

DIGITAL CONTROL OF SINGLE-PHASE POWER FACTOR PREREGULATORS WITH INPUT VOLTAGE ESTIMATION

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Abstract – This paper proposes a fully digital control of boost Power Factor Preregulators (PFPs) with input voltage estimation. The proposed solution is based on a conventional multi-loop structure for PFP with an internal current control and an outer voltage control possibly with fast dynamic response. Instead, input voltage sensing is avoided by using a conventional PI (proportional-integral) current regulator for the estimation of the rectified input voltage. The use of the estimated rectified input voltage for the generation of current reference introduces an additional control loop which, however, increases the stability margin of the current regulator. The digital control has been implemented using the TMX320F2812 DSP, which has been proven to be an effective hardware for rapid prototyping. Experimental results on a single-phase 400W boost PFP show the effectiveness of the proposed approach.

I. INTRODUCTION

The investigation of digital control for Power Factor Preregulators (PFPs) is relatively new and the main contributions on this subject are given in [1]-[8]. The limiting factors in the application of digital control to PFP have been so far the cost and performance of discrete DSP and microcontroller systems, in spite of some interesting advantages that digital controllers offer compared to their analog counterparts: low quiescent power, immunity to analog component variations, ability to implement sophisticated control algorithms and system diagnostics. However, the recent use of digital controller IC specifically developed for high-frequency switching converters [9-11] has overcome some of the above-mentioned disadvantages allowing potential increase of applications of digital controllers for high-frequency switching converters.

The PFP digital control structure described in previous paper [1-7] is similar to conventional analog controllers, widely discussed in literature; thus, the control algorithm is essentially based on a multi-loop control where the outer voltage loop determines the amplitude of the current reference, the waveform of the current reference being proportional to the input voltage waveform. In this conventional configuration the sensed variables are output voltage, inductor current and input voltage.

In some papers [1-7] some potentialities of the digital control have been exploited and, more specifically, digital techniques, which remove the output voltage ripple at twice the line frequency, have been used in order to improve system dynamics. A recent implementation with FPGA has been proposed in [1], which exploits the potentiality of simultaneous executions of control procedures. Finally, in [14] the measurement of the input voltage has been avoided, by implementing a predictive digital current control together with a disturbance observer for input voltage estimation.

This paper proposes a fully digital control of boost Power Factor Preregulators using a more conventional PI (proportional-integral) control structure for the current regulator. Compared to [14], we avoid the use of a predictive control structure showing that, even with a conventional PI control the estimation of the input voltage can be easily achieved. Indeed, using the results of [15], we have seen that even in PFP applications the estimation of the input voltage does not require any additional calculations. In fact, the input voltage is proportional to the integral quantity computed by the current regulator, as long as the output of the current regulator is proportional to the complement of the duty-cycle. Thus, the proposed solution is based on a modification of the conventional multi-loop structure for PFP with an internal current control and an outer voltage control with fast dynamic response. However, we avoid the sampling of the input voltage and possibly a filter on the input voltage, which is sometimes needed in order to avoid the interaction with the EMI filter [17]. Experimental results on a Boost prototype using the TMX320F2812 show the effectiveness of the proposed approach.

II. CONTROL METHOD

Fig. 1 shows the basic scheme of a boost PFP. The PFP's current controller operates the switch so as to draw from the grid an average current $i_g(t)$ whose waveform is proportional to the line voltage $v_g(t)$ by a factor determined by the voltage loop control. Being the line voltage $v_g(t)$ estimated, the proposed control requires the sampling of two variables: output voltage and average input current with a sampling frequency equal to the modulation frequency.

A. Sampling instants

An advantage of the digital approach is that the average value of the sensed current is obtained, without low-pass filters in the loop, by synchronizing sampling and modulation so that the current is always sampled in the middle of the switch-on or switch-off period. One common procedure to avoid possible sampling noise around the switching transition is to choose the sampling in the middle of the switch-on period when the duty-cycle is greater than 0.5 and in the middle of the switch-off period when it is lower than 0.5 [18]. While the two sampling instants are equivalent in Continuous Conduction Mode (CCM), there are some differences in Discontinuous Conduction Mode (DCM) so that the cross-over distortion may be different depending on the sampling strategy.

B. PI Current control interpretation using PBC approach

There are different algorithms, which can provide the estimation of the input voltage. Among them, we found out that the simplest one is based on the integral part of the current controller, as long as a Proportional-Integral (PI) current control is chosen. In order to show this interesting property, let us derive the PI current control within the Passivity-Based Control (PBC) theory [16].

Assuming the time-scale decomposition between voltage loop and current loop, we can focus on the first-order dynamics of the boost inductor, which can be expressed (in CCM) as:

$$\frac{d}{dt} i_L(t) = \frac{1}{L} \left(v_r(t) - \delta'(t) \cdot v_o(t) \right) \cong \frac{1}{L} \left(v_r(t) - \delta'(t) \cdot V_o \right) \quad (1)$$

where $i_L(t)$ is the inductor current, $v_r(t)$ the rectified input voltage, $v_o(t)$ the output voltage, which can be approximated

with its constant DC value V_o , as far as the current dynamics is concerned, and $\delta'(t)$ the complement of the duty-cycle $\delta(t)$, which is also the output of the current regulator, as shown in Fig. 1.

Let us now consider the following ‘‘energy in the increment’’ [16]:

$$W = \frac{1}{2} L \left(i_L - i_L^{\text{ref}} \right)^2 + \frac{1}{2} \alpha \left(\hat{v}_r - v_r \right)^2 \quad (2)$$

where i_L^{ref} is the inductor current reference, \hat{v}_r the estimated input voltage, α a design coefficient and the time arguments have been dropped.

In order to stabilize the system, a sufficient condition is to impose that the energy term is always decreasing (i.e. $dW(t)/dt \leq 0$). Using (1) and (2), it is easy to verify that:

$$\frac{dW}{dt} = \varepsilon_{iL} \left(v_r - \delta' \cdot V_o \right) + \alpha \varepsilon_{v_r} \frac{d \hat{v}_r}{dt} \quad (3)$$

where $\varepsilon_{iL} = i_L - i_L^{\text{ref}}$, $\varepsilon_{v_r} = \hat{v}_r - v_r$ and we have assumed that the inductor current reference i_L^{ref} and the rectified input voltage v_r are constant, which can be considered a good approximation since they are slowly-varying compared to the current loop bandwidth.

Inspection of (3) shows that a good candidate for system control is

$$\delta' = \frac{k_d}{V_o} \varepsilon_{iL} + \frac{1}{V_o} \hat{v}_r \quad (4)$$

$$\frac{d \hat{v}_r}{dt} = \frac{1}{\alpha} \varepsilon_{iL}$$

since the condition $dW(t)/dt \leq 0$ becomes:

$$\frac{dW}{dt} = -k_d \varepsilon_{iL}^2 \leq 0 \quad (5)$$

which is, of course, always verified. Control algorithm (4) is a PI current control, where the proportional gain is $k_p = k_d/V_o$ and integral gain is $k_i = 1/(\alpha V_o)$. This reasoning shows not only the straightforward result that PI structure is a good candidate for system control, but also that the proportional gain is giving the dissipative term (5) [16], while the integral term provides an estimation of the rectifier input voltage. If the integral term can be seen as the estimation of the rectifier input voltage [16], then we propose to use it also for the generation of the waveform of the inductor reference current, as reported in Fig. 2. Indeed, the use of the estimation of the input voltage in order to determine the reference current $i_L^{\text{ref}}(t)$, introduces an additional loop in the proposed scheme, which must be analysed in order to validate the proposed approach.

The analysis is reported here in the continuous-time domain only for simplicity of explanation. It can be easily extended to

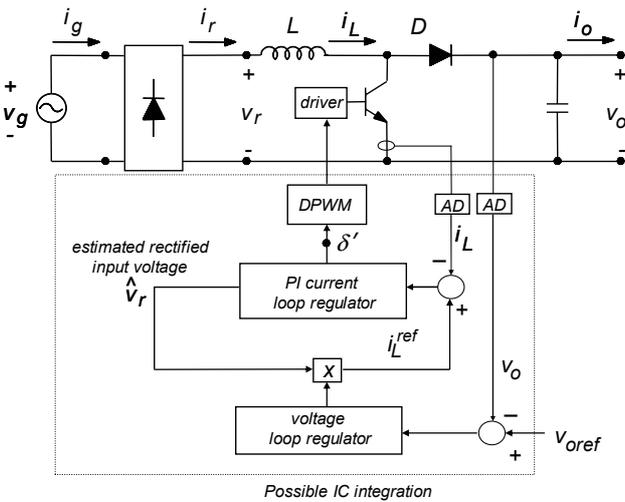


Fig. 1 – Digital control of Boost PFC with line voltage estimation.

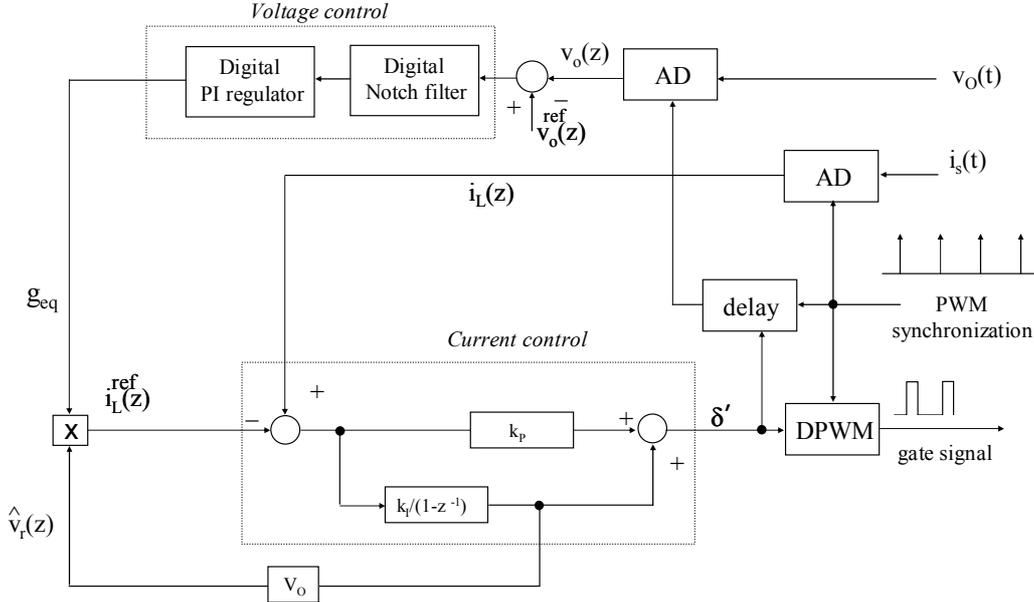


Fig. 2 – Block diagram of the proposed digital control with input voltage estimation.

the discrete-time domain with minor modifications. Indeed, the proposed approach is general and can be used not only for digital but also for analog implementation. However, the advantages obtainable with an analog implementation are not significant, since only a few passive components are avoided. Instead, more important advantages are obtained in the digital implementation, since all signal conditioning circuits related to the input voltage sensing (signal preconditioning, A/D converter, etc.) can be eliminated. Moreover, possible noise sampling in the input voltage due to switching actions is inherently avoided.

C. Stability analysis

The stability analysis can be easily performed using the equivalent block diagram of the current control reported in Fig. 3, where g_{eq} is representing the equivalent load conductance and $G_F(z)$ includes the inductance admittance and a delay which accounts for the computational delay of the digital implementation. With simple elaborations on Fig. 3a, the equivalent block diagram of Fig. 3b is obtained, where transfer function $H(z)$ is a first-order high-pass filter and its expression is given by:

$$H(z) = \frac{z-1}{(1+g_{eq}V_O k_I)z-1} \quad (6)$$

As far as the current loop gain, is concerned, it is clear that the additional control loop introduced by generating the current reference with a signal proportional to the integral part of the current regulator, only increases the stability

margin of the system. As an example, in Fig. 4 we report the bode diagram of the current loop gain $T_I(z)=H(z) G_F(z) V_O$ ($k_p+k_i/(1-z^{-1})$), with the parameter used in our experiments: $L = 2$ mH, $f_{sw} = 50$ kHz, $V_o = 400$ V, $P_{oNOMINAL} = 400$ W, $f_c = 7$ kHz (current loop bandwidth). Note how the current loop phase margin increases as g_{eq} moves from zero (no load condition) to the nominal value (full load condition).

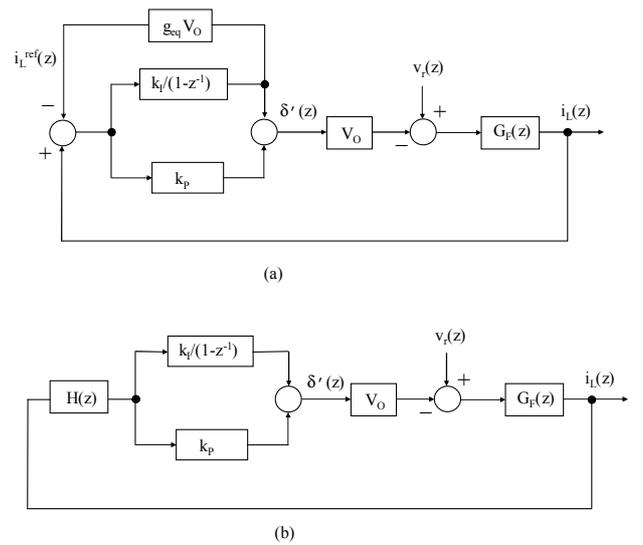


Fig. 3– (a) Equivalent block diagram of the current loop, (b) rearrangement of (a) showing the increased current loop phase margin.

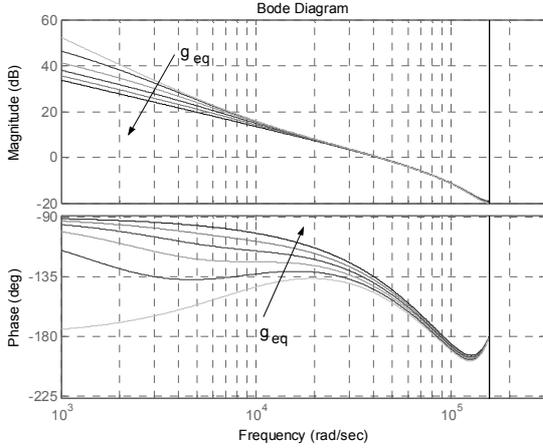


Fig. 4 – Bode diagram of the current loop gain varying equivalent conductance g_{eq} from zero (no load condition) to the nominal value

III. INTERACTIONS BETWEEN EMI FILTER AND PFP

In order to evaluate possible interactions between the EMI filter and the closed-loop PFP, the ratio of the EMI filter output impedance $Z_F(z)$ and the converter input impedance $Z_{in}(z)$ need to be analysed. In fact, such ratio can be interpreted as the loop gain $T_F(z)$:

$$T_F(z) = \frac{Z_F(z)}{Z_{in}(z)} = Z_F(z) \cdot Y_{in}(z), \quad (5)$$

which must satisfy stability criteria in order to avoid interaction between the EMI filter and the power converter [17]. In order to highlight possible reduction of these interactions due to the proposed estimation scheme, we have reported in Fig. 5 the closed loop input admittance using the measure of the input voltage (case a) and the proposed estimation scheme (case b). Note that the proposed solution shows a magnitude reduced by 5 dB, with a small phase increase close to the current loop corner frequency, where interactions with the EMI filter usually occur. Thus, the proposed solution gives an advantage even from this point of view.

IV. EXPERIMENTAL RESULTS

The proposed solution has been tested both using numerical simulations (Simulink) and an experimental prototype. Simulation results, which confirmed the analysis presented in the previous sections, are not reported here. From the experimental point of view, a boost PFP prototype has been realized with the following parameters: $L = 2$ mH, $C = 330$ μ F, $V_g = 230$ V_{RMS}, $f_{sw} = 50$ kHz, $V_o = 400$ V and $P_{oNOMINAL} = 400$ W. The digital controller has been implemented in a newly developed fixed-point DSP by Texas Instruments (TMX320F2812), which we found a powerful and flexible hardware support for rapid prototyping. The sampling frequency has been chosen to be equal to the

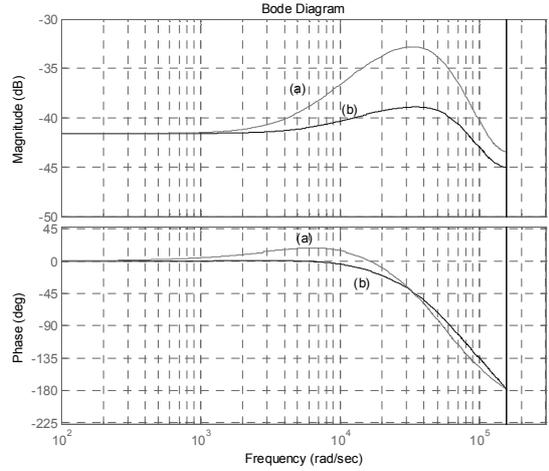


Fig. 5 – Closed loop PFP input admittance with the measurement (a) and the estimation (b) of the input voltage.

switching frequency both for the current and voltage loop, although downsampling could be advisable in a practical application, especially for the voltage loop, so as to reduce computational effort.

Fig. 6 shows input voltage $v_g(t)$ and unfiltered input current $i_g(t)$ at 75% of the rated load and for nominal input voltage of 230 V_{RMS}. Note that the distortion on the current waveform is quite small, even during zero crossing of the input current. This is also confirmed by the input current spectrum, reported in Fig. 7, where all harmonics are at least 40 dB below the fundamental one.

We have also tested our system at 25% of the nominal load where the converter operates in DCM for a significant part of the line period. As reported in Fig. 8, in this case the current waveform distortion is much higher due to the lower control gain in DCM. Note, however, that current harmonics are almost 30 dB below the fundamental component, as reported in the spectrum of Fig. 9.

In order to highlight the system performance for typical airport applications, we have increased the line frequency up to 300Hz, which was the maximum frequency available on our ac power supply, and the results at full load are reported in Fig. 10. The quality of the input current waveform is still very good, demonstrating the validity of the proposed approach.

Finally, we have tested the dynamics of the voltage control imposing step load changes from 25% to 100% of the nominal load (Fig. 11) and viceversa (Fig. 12). One important advantage of the digital implementation is the possibility to obtain quite easily a fast dynamic response. Among the solutions proposed in the past, we have implemented a voltage notch tuned at twice the line frequency. Figs 11 and 12 report the load transients and confirm the possibility to realize a high control loop bandwidth, which is not easy to achieve by analog means.

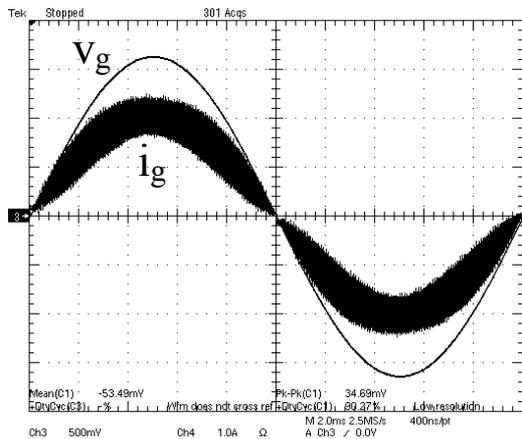


Fig. 6 – Line input voltage v_g (100V/div) and input current i_g (1A/div) at 75% of the nominal load.

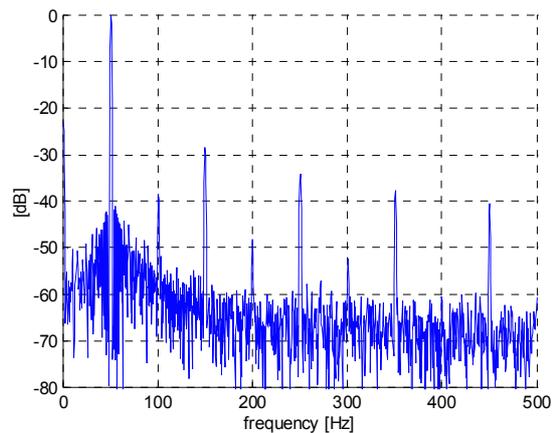


Fig. 9 – Normalized input current spectrum at 25% of the nominal load.

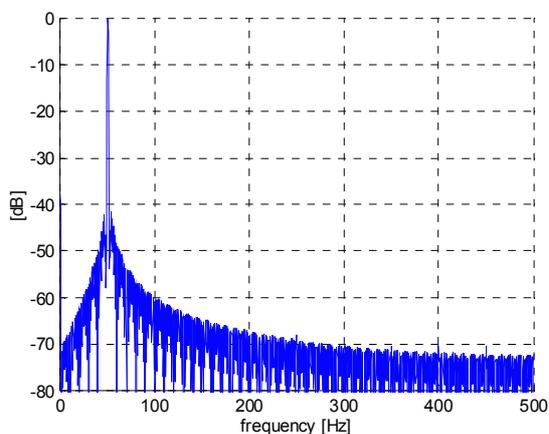


Fig. 7 – Normalized input current spectrum at 75% of the nominal load.

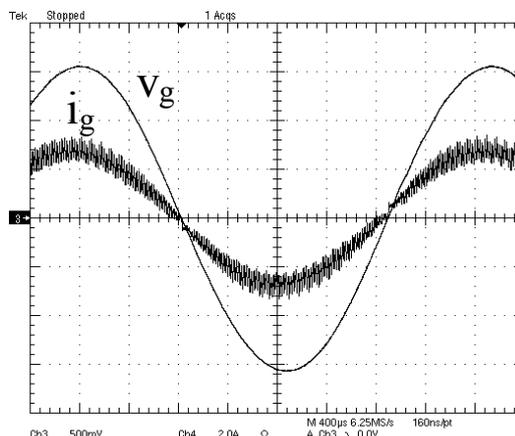


Fig. 10 – Line input voltage v_g (100V/div) and input current i_g (2A/div) at full load with line frequency equal to 300Hz.

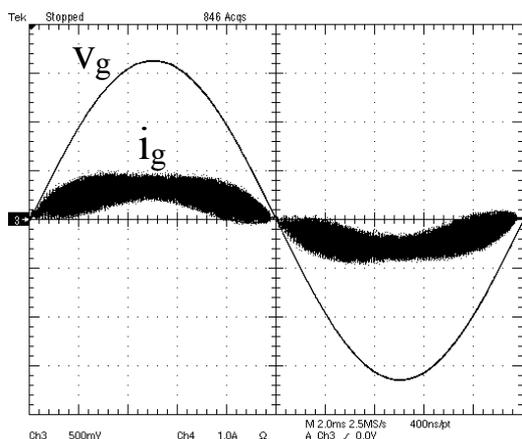


Fig. 8 – Line input voltage v_g (100V/div) and input current i_g (1A/div) at 25% of the nominal load

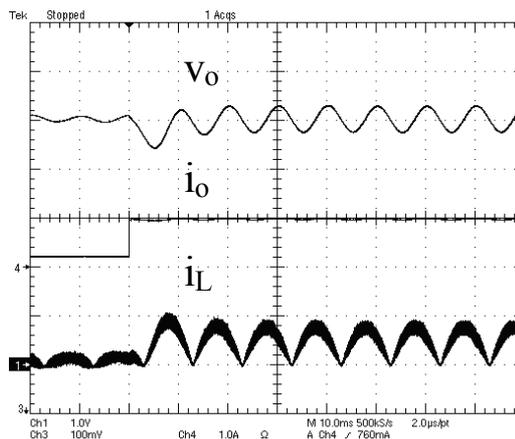


Fig. 11 – Load transient from 25% to 100% of nominal load: output voltage v_o (20V/div), output current i_o (1A/div) and inductor current i_L (4 A/div).

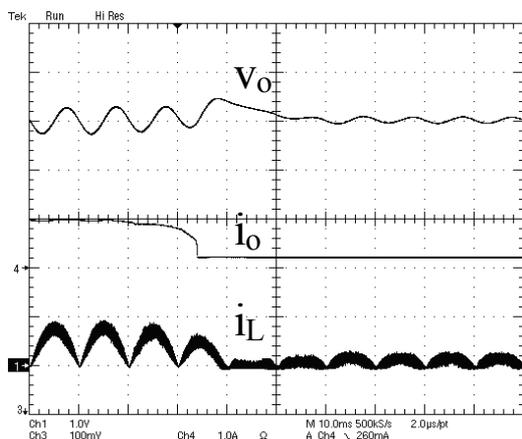


Fig. 11 – Load transient from 100% to 25% of nominal load: output voltage v_o (20V/div), output current i_o (1A/div) and inductor current i_L (4 A/div).

V. CONCLUSIONS

This paper has proposed a fully digital control of boost Power Factor Preregulators, where the line input voltage sensing is avoided and its estimation is simply taken from the integral part of a PI regulator. The additional control loop needed for input voltage estimation does not affect stability and increases current-loop phase margin. The proposed solution can be theoretically applied to analog controllers too, but it gives significant advantages only in the digital implementation. The proposed algorithm has been verified by experimental tests on a boost PFP, basically confirming the theoretical analysis.

VI. ACKNOWLEDGMENTS

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