Digital Control of Single-Phase Power Factor Preregulators suitable for Smart-Power Integration

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***Abstract*—This paper proposes a fully digital control of boost Power Factor Preregulators (PFPs) with input voltage estimation that is suitable for smart-power integration. The proposed solution features a minimum pin count by avoiding direct sensing of the input voltage for the construction of the internal current reference signal and by sensing the output voltage through a direct sampling of the voltage across the power switch during its off interval at the line voltage peak. The control algorithm requires the estimation of the rectified input voltage, that is simply done by exploiting the integral part of the current loop PI regulator, and a PLL (Phase-Looked-Loop) synchronization with the estimated line frequency for sampling the output voltage and rejecting the low-frequency output voltage ripple. The provisions needed to ensure correct output voltage sensing, even during transient and light-load conditions, are also discussed. Experimental results on a single-phase boost PFP show the properties of the proposed approach.**

I. INTRODUCTION

Digital controllers for Switch-Mode Power Supplies (SMPS) are gaining growing interest, since when it has been shown the feasibility and advantages of digital controller ICs specifically developed for high-frequency switching converters [1-2]. One interesting field of application is the control of Power Factor Preregulators (PFPs) because their dynamic performances are not very demanding. Indeed, one of the limiting factor for the use of digital control in SMPS is the achievement of performances comparable to those of analog controllers in presence of non idealities such as control delays and quantization effects. On the other hand, even in PFP applications, digital control offers some interesting advantages, such as immunity to analog component variations, ability to implement sophisticated control schemes, system diagnostic capability and faster design process from the controller integration point of view.

The investigation on digital control algorithms for Power Factor Preregulators (PFPs) is relatively new and few works are available so far [3-12]. The control structure described in previous papers [3-5] is defined according to what is normally done in analog controllers; thus, the control algorithm is essentially based on a multi-loop control where the outer voltage loop determines the current reference amplitude by multiplying a signal proportional to the rectified input voltage waveform. Moreover, in [3-9], some potentialities of the digital implementation have been exploited and, more specifically, digital techniques to remove the output voltage ripple at twice the line frequency have been used, so as to improve system dynamics. Moreover, techniques which do not require input voltage sensing have been proposed in [11-12] and, more specifically, in [11] the input voltage has been estimated using a disturbance observer and in [12] using the integral part of the Proportional-Integral (PI) current regulator.

This paper proposes a fully digital control of PFP boost that uses the results of [12] and employs an output voltage sensing by a PLL synchronized with the estimated rectified line voltage. With this provision, the low-frequency output voltage ripple is rejected and, more importantly, the output voltage measure is obtained by sampling the voltage across the switch during its off state and at the line voltage peak. Thus, digital control is based only on current and voltage measurements at the switch terminals, ensuring a minimization of external pin count and making this solution suitable for smart-power ICs, where the package cost affects considerably the overall IC cost. Experimental results on a boost prototype show the effectiveness of the proposed approach.

II. CONTROL STRATEGY BASED ON SWITCH VOLTAGE AND CURRENT MEASUREMENTS

Fig. 1 shows the basic scheme of a boost PFP. The PFP's current controller operates the switch so as to draw from the grid a current $\bar{i}_g(t)$ (averaged on each switching period) whose waveform is proportional to the line voltage $v_g(t)$ by a factor determined by the voltage control loop.

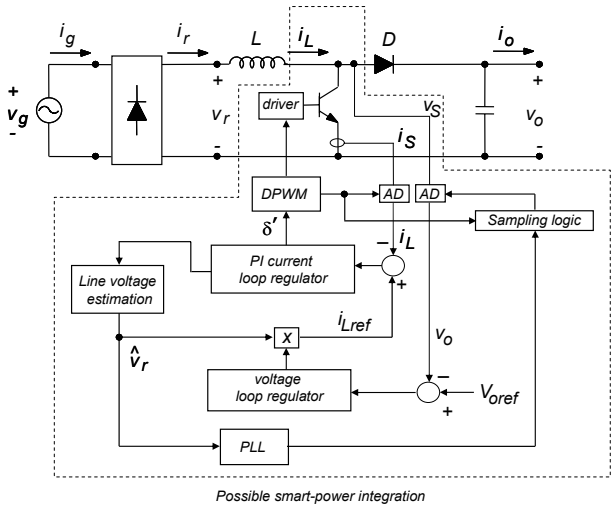

Fig. 1 – Proposed fully digital control of Boost PFP with current and voltage measurements at switch terminals

A. DPWM and sampling instants

As far as the Digital Pulse Width Modulation (DPWM) is concerned, the triangle modulation has been adopted, as depicted in Fig. 2. This choice easily provides the sampling instants for the switch current $i_S(t)$ in the middle of the switch-on time, since it occurs when the PWM carrier is zero. Moreover, under the assumption of Continuous Conduction Mode (CCM), it ensures that the sensed current is the average inductor current $\bar{i}_L(t)$ (averaged on each switching period). Compared to trailing edge or leading edge modulations, it also ensures constant sampling frequency.

The output voltage is obtained by sampling switch voltage $v_S(t)$ during switch-off time (t_{off}); more specifically, the output voltage sensing is obtained by sampling the switch voltage, with a delay T_d after the turn-off time and when signal S_{PLL}, synchronized at the line voltage peak, is active. The synchronization with the line voltage peak gives several advantages:

- the switch-off time (t_{off}) is maximum;
- the inductor current value is maximum within the line cycle; thus, diode D is more likely to conduct at the voltage sampling instants;
- the sampled output voltage coincides with its average value (averaged on each line period);
- the low-frequency output voltage ripple is rejected, similarly to the sample-and-hold solution proposed in [13].

The most critical point is the need to ensure diode conduction at the voltage sampling instant, even during PLL transients and light-load conditions. For such purpose, a set of protection algorithms is needed in the controller, as reported in subsection D.

B. Rectified line voltage estimation

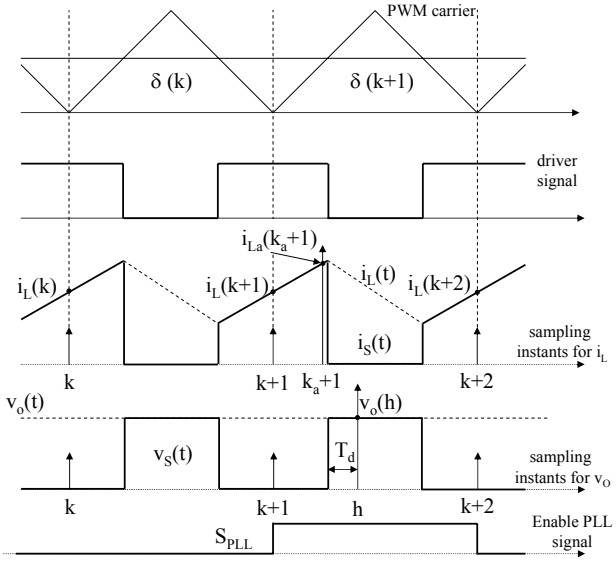

Fig. 2 – PWM timing and sampling instants

There are different algorithms which can provide the estimation of the input voltage. Among them, we found that the simplest one is based on the integral part of the current controller, as long as a Proportional-Integral (PI) current control is chosen, and the complement of the duty-cycle δ' is taken as the output of the current regulator [12].

The situation is depicted in Fig. 3 and we recall here the main results reported in [12]. The discrete-time model of inductor dynamics in CCM can be expressed as:

$$i_L(k+1) = i_L(k) + \frac{T_{sw}}{L}\left(v_r(k) - \delta'(k)\cdot v_o(k) \right) \qquad (1)$$

where $i_L(k)$ is the average inductor current, $v_r(k)$ the rectified input voltage, $v_o(k)$ the output voltage, which is approximated with its constant DC value V_o, T_{sw} the switching period and $\delta'(k)$ the complement of the duty-cycle $\delta(k)$, all of them evaluated at the sampling instant $k\cdot T_{sw}$. Using a PI control structure, the inner current regulator is expressed as:

$$\begin{aligned} \delta'(k+1) &= K_p\, \varepsilon_{iL}(k) + u_I(k) \\ u_I(k) &= u_I(k-1) + K_I\, \varepsilon_{iL}(k) \end{aligned}, \qquad (2)$$

where $\varepsilon_{iL}(k) = i_L(k) - i_L^{ref}(k)$. Since the only disturbance in the current loop is the input voltage, the integral part of the regulator is a good estimation of the rectified input voltage [12], i.e.:

$$\hat{v}_r(k) \cong V_o\, u_I(k). \qquad (3)$$

Thus, the integral term $u_I(k)$ can also be used for the generation of the inductor current reference waveform, as reported in Fig. 3, without the need for direct measurement of the rectified input voltage. Indeed, the use of the estimation of the rectified input voltage in order to determine the reference current $i_L^{ref}(k)$, introduces an additional loop, which however increases the stability margin of the current loop, as demonstrated in [12].

Since the estimated rectified voltage $\hat{v}_r(k)$ is also used for the synchronization of the output voltage sampling, estimation errors in Discontinuous Conduction Mode (DCM) need to be quantified. Fig. 4 shows the estimated rectified input voltage in a situation where the converter operates in DCM during a non negligible fraction of the line half period: as can be seen, the estimated waveform is substantially higher than the theoretic sine wave in DCM. This error can be quantified as follows: neglecting the average voltage drop across the input inductor, assuming DCM operation, from (1) we can write:

$$v_r(k) = \delta'_a(k) V_o, \qquad (4.a)$$

where $\delta'_a T_{sw}$ denotes the portion of the t_{off} time where diode D is conducting. From (2), the estimated rectified voltage is given by (at steady state $\varepsilon_{iL} = 0$):

$$\hat{v}_r(k) = \delta'(k) V_o. \qquad (4.b)$$

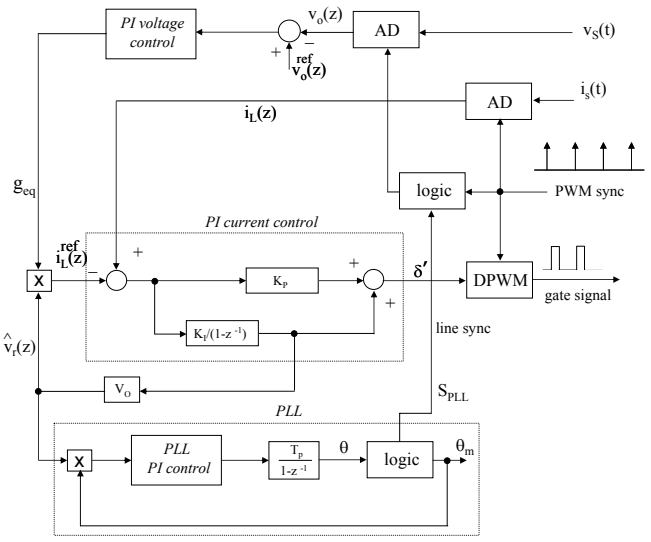

Fig. 3–Proposed digital control structure

Since $\delta'_a < \delta'$ in DCM, (4) shows that estimated rectified line voltage $\hat{v}_r(k)$ is always greater than actual value $v_r(k)$. Fortunately, the estimation errors do not give a significant input current distortion [12], since the overestimation of $v_r(k)$, which implies that the reference current $i_L^{ref}(k)$ is greater respect to the theoretical case, partially compensates for the current errors caused by the decrease of the current loop gain in DCM. Instead, estimation errors need to be considered in the choice of the synchronization scheme used for output voltage sampling.

C. Synchronized output voltage sensing

Synchronization with the line voltage is achieved by using a PLL (Phase-Locked-Loop) on the estimated line voltage $\hat{v}_r(k)$, as shown in Fig. 5. Due to the aforementioned estimation errors in DCM, that cause substantial distortion on the estimated rectified line voltage waveform, PLL algorithms based on waveform crossings are not suited in this case. For this reason, we adopted a PLL scheme whose operation is not strongly dependent on the actual waveform of the synchronization signal. Its block diagram is reported in Fig. 5a: it includes a Phase Detector (PD), which is obtained by multiplication between signal y and synchronized signal y_{sync}, a low-pass filter $F_{PLL}(z)$, a Voltage Controlled Oscillator (VCO), based on a integrator with reset, and a trigonometric function (like the sin(•) function). If ω_s is the angular frequency of y and ω_o the initial angular frequency of y_{sync} (i.e. when ω_c is zero), then $\omega_c = \omega_s - \omega_o$ under locked conditions. Moreover, if $F_{PLL}(z)$ includes an integral term, then the average value of the Phase-Detector output signal is zero and signals y and y_{sync} are in quadrature. This, indeed, is the situation depicted in Fig. 5a.

The actual PLL scheme adopted is reported in Fig. 5b, where the VCO is simply obtained using a modified integrator with an up-down counter that produces a triangular waveform θ_m, which, in steady-state, is in quadrature with the fundamental component of the estimated rectified line voltage. This solution provides a simpler control algorithm, which does not require a trigonometric function, as compared to the basic scheme of Fig. 5a, and a straightforward generation of the sampling signal S_{PLL} for the output voltage sensing, since it is simply obtained by detecting the zero-crossing when the triangular waveform θ_m is decreasing.

As already stated above, different PLL schemes can be used, like those based on zero-crossing of y and y_{sync}, or different VCO schemes can be adopted. It is worth to point out, however, that any other solution need to be robust against possible distortions on the estimated line voltage.

One of the weak point of the scheme in Fig. 5 is that the capture range is rather small. While this is not a problem in our prototype, where the capture range is large enough to guarantee synchronization with 50-60 Hz, avionic applications may call for additional provisions in order to extend the capture range to several hundred of Hz. Common solutions are, for example, the use of an estimation of the frequency of y using an intersection with a threshold voltage or a proper management of initial phase estimation [14]. These provisions, however, are beyond the scope of this paper and will not be further discussed here.

D. Issues at light load

The major drawback of the proposed solution is that it is not working at no-load conditions, where the duty-cycle is zero for very long times and the output voltage sensing is not possible through the switch voltage sensing. In order to ensure a precise output voltage sensing, a non zero switch on-time must be forced, even at no-load, at given time instants. These pulses, which we will refer as "sense pulses", are applied only if the enable signal is not present after a time interval which corresponds to the lowest frequency foreseen on the supply voltage. It is important to note that, in these conditions, the PLL is not working anymore, since the rectified line voltage is not estimated. Consequently, the output voltage sensing is no more synchronized with the peak of the line voltage. This, however, gives only negligible errors, since the output

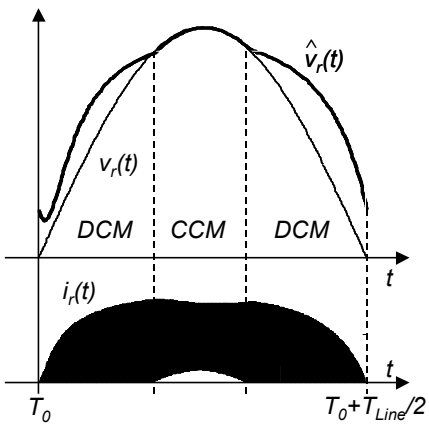

Fig. 4 – Typical estimated rectified line voltage and inductor current waveforms at light-load, showing a substantial DCM operation interval

voltage ripple is very small at light-load, and any instant is valid for the output voltage sensing.

The "sense pulses" imply a minimum load, that is, however, very small if they are applied at most once in each half line period. The minimum output power required can be roughly estimated assuming that the "sense pulses" always occur at the peak of the line voltage, which is, indeed, the worst case condition. Thus, the minimum output power is (assuming unity efficiency):

$$P_{o\min} = \frac{V_{gpk}^2}{L} t_{sense}^2 \left[\frac{1}{M-1}\right] f_{Line}, \quad (5)$$

where f_{Line} is the line frequency and M is the boost conversion ratio at the line peak ($M = V_o/V_{gp}$). Inspection of (5) shows that the minimum output power is very small, less than 1% of the nominal power in our case.

A final protection is needed in order to ensure that diode D is conducting during the switch voltage sampling instants, even during PLL transients or light-load conditions. Since the inductor current is available during the switch-on time, one possible solution, that we have adopted, it to sample the inductor current before the switch turn-off (this sampling is done only before the output voltage sampling, i.e. at twice of the line frequency). Let's denote $i_L(k)$ the sampling at the middle of the switch-on time and $i_{La}(k_a)$ the current sampling before the switch turn-off (see Fig. 2). A simple protection algorithm is based on the prediction of the inductor current level at the voltage sampling instant; when the predicted current is greater than zero, correct sampling is ensured. The condition to be satisfied is:

$$i_{La}(k_a) > \left(\frac{\delta(k)}{\delta(k) + 2T_d/T_{sw}}\right) \cdot \left(\frac{V_o}{L} T_d + i_L(k) \frac{2T_d}{\delta(k) T_{sw}}\right), \quad (6)$$

where V_o can be approximated with its reference $V_o^{ref.}$. A sufficient condition for (6) is that:

$$i_{La}(k_a) > \frac{V_o}{L} T_d, \quad (7)$$

where the inductor current down-slope was assumed equal to $-V_o/L$ (worst-case condition).

III. Design Criteria

Design criteria for PI current and voltage loop parameters and the analysis of the voltage loop bandwidth achievable when the output voltage is sampled at twice of the line frequency, are reported in previous papers and here not discussed [3-13]. In this section, we focus on the PLL analysis. For the scheme of Fig. 5a, the small-signal model of the phase detector is :

$$PD = \frac{Y_{in}\, Y_{sync}}{2}, \quad (8)$$

where Y_{in} and Y_{sync} are the peak amplitude of signal y and y_{sync}. The small-gain of the phase detector in Fig. 5b is slightly different due to the fact that signal $\hat{v}_r$ and θ_m are not sinusoidal. Neglecting the contribution of harmonic components and taking into account that the fundamental component of the rectified line voltage (V_{1r}) is $4V_{rp}/(3\pi)$, being V_{rp} the peak value of the line voltage, and that the fundamental component of signal θ_m is $4/\pi$, (8) is modified as:

$$PD = \frac{8 V_{rp}}{3\pi^2}. \quad (9)$$

The filter following the phase detector typically has a PI structure:

$$F_{PLL}(z) = K_{pPLL} + K_{iPLL} \frac{1}{1 - z^{-1}}, \quad (10)$$

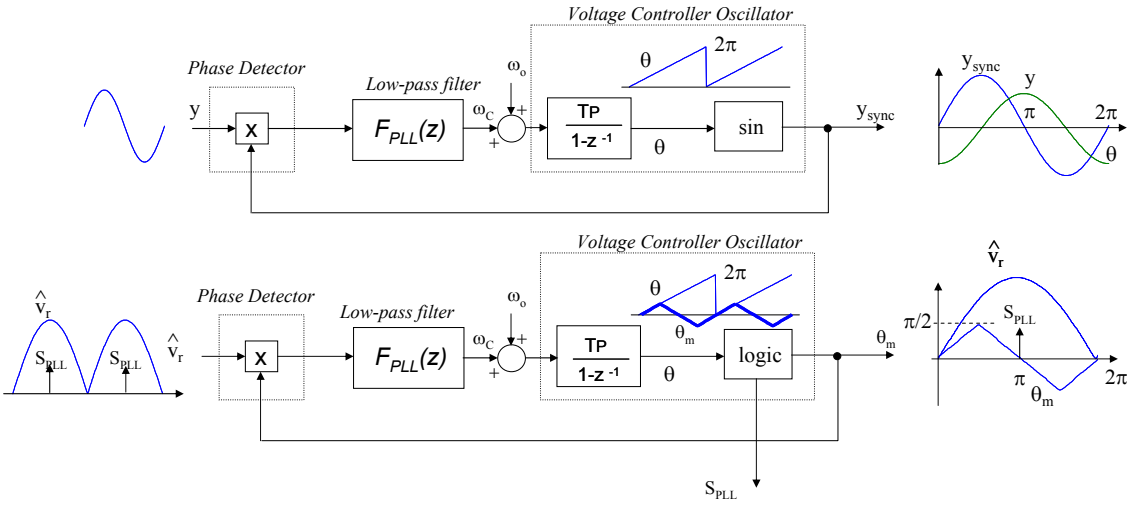

Fig. 5 – Phase-Locked Loop: (a) general block diagram; (b) solution used for synchronization with the estimated line voltage

possibly including high-frequency low-pass with time constant τ_{LP} for the attenuation of high-frequency components caused by the phase-detector. Finally, the VCO is a pure integrator, i.e.:

$$VCO(z) = \frac{T_P}{1 - z^{-1}}. \qquad (11)$$

where T_P is the sampling period of the PLL algorithm. Stability analysis and design of K_{pLL} and K_{iPLL} are performed looking at the PLL loop gain $GH_{PLL}(z)=PD \cdot F_{PLL}(z) \cdot VCO(z)$. The evaluation of the capture range is rather complex, especially when $F_{PLL}(z)$ includes an integral part. A rough estimation of the capture range is usually obtained when the amplitude of the transfer function $PD \cdot F_{PLL}(z)$ intersects the line with unity slope, as shown in Fig. 6. Using a PLL bandwidth of 30 Hz and including a low pass filter in (10) with time constant equal to 10 ms (τ_{LP}=10 ms), the estimated capture range is roughly 32 Hz, which covers very well 50-60 Hz applications. The results is also verified by simulations, where the supply frequency has been varied around a nominal value ω_o and the average value of ω_c (averaged over a given simulation time) has been reported with symbol 'o' in Fig. 6. When the PLL is locked, the average value of ω_c lies on the line with unity slope, as shown in Fig. 6. Thus, the estimated capture range is an underestimation of the actual one.

IV. Experimental Results

The proposed solution has been tested both using numerical simulations (Matlab/Simulink) and an experimental prototype. Simulation results, which confirm the analysis presented in the previous sections, are not reported due to space constrains. In the experimental prototype, the boost PFP prototype has the following parameters: L = 2 mH, C = 330 μF, V_g = 150 V_{RMS}, f_{sw} = 50 kHz, V_o = 260 V and P_{oNOM} = 240W. The digital controller has been implemented in fixed-point DSP by Texas Instruments (TMX320F2812). Indeed, the DSP used is much more powerful than needed for the specific application since we needed only a few percent of the processor time to implement the proposed algorithm. Thus, the use of this specific hardware should be seen only for rapid-prototyping purposes.

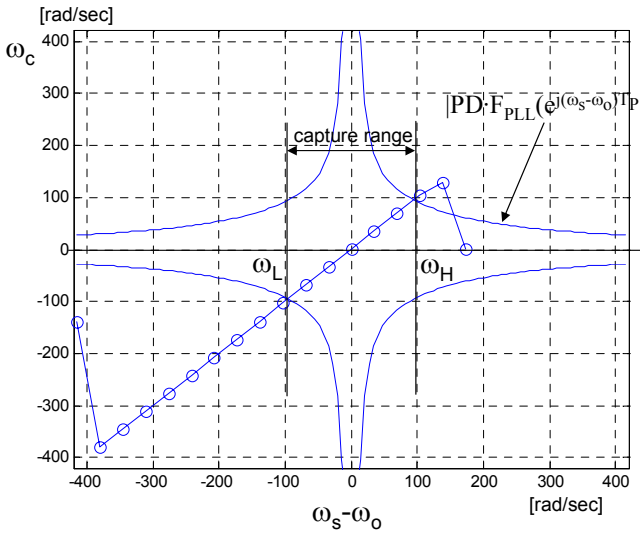

Fig. 6 – Estimation of the PLL capture range (ω_o=2*π*55 rad/sec)

Fig. 7 shows the input voltage $v_g(t)$ and input current $i_g(t)$ at full load. Note that the distortion on the current waveform is quite small, even during zero crossing of the input current. This is also verified by the input current spectrum, reported in Fig. 8. Fig. 7 reports also the synchronizing signal S_{PLL}, which occurs at the line voltage peak, and signal θ_m, obtained using an auxiliary PWM output and a low-pass filter, which implement a Digital-to-Analog (DAC) converter. The small phase-shift between zero-crossing of θ_m and the output voltage sampling instant is due to the delay of the low-pass filter.

Fig. 9 reports the dynamic behavior of the voltage loop in presence of load step changes from the nominal load to 33% of the nominal load and vice versa. The transient response time is very good while keeping low input current distortion in steady-state. This is, indeed, obtained thanks to the sampling of the output voltage at twice the line frequency [13].

In order to test the PFP operation at light-load, a resistor of 47 kΩ has been connected at the output terminal. As shown in Fig. 10, a sense pulse is applied every 11 ms. Consequently, there are small step variations on the output voltage following the sense pulses, which are, however, almost negligible. Details of the sense pulse are reported in Fig. 11, which shows correct output voltage sensing even during this condition. The sense pulse is, indeed, longer than needed since a switch turn-on is applied also after output voltage sampling. This particular solution adopted in the experimental prototype is due to the fact that the duty-cycle is updated only once in a switching period. Either using a double-update mode or a specific digital hardware, such as a Field Programmable Gate Array (FPGA), the sense pulse can be easily improved.

In order to verify the PLL dynamics, the converter behavior during the control start-up is reported in Fig. 12. Looking at the output ω_c of the PLL regulator, it can be seen that the PLL is able to lock the input voltage in around 250 ms. As far as the output voltage is concerned, the dynamic behavior is acceptable even without adopting any particular soft-star procedure, which is, however, needed in practical applications. It is interesting to note the small oscillation in the output voltage after the start-up, that corresponds to the oscillation in the PLL signal ω_c. This is due to the output voltage sampling, which, during PLL transient conditions, is no more synchronized with the line voltage peak: as a consequence, the measured output voltage deviates from its average value by a quantity related to the output voltage ripple.

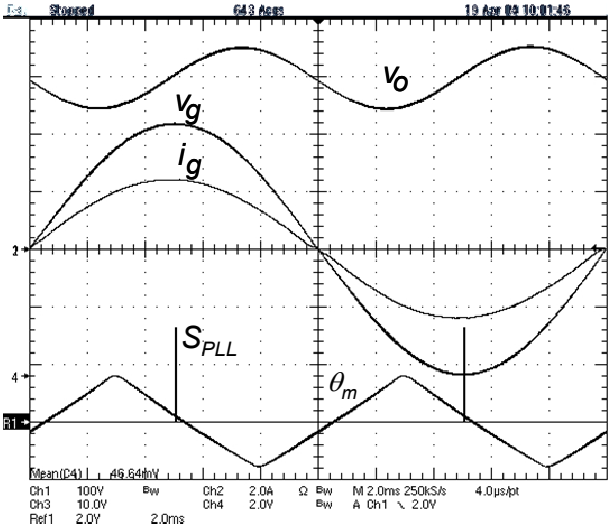

Fig. 7 – Line voltage v_g (100V/div), filtered line current i_g (2A/div), output voltage v_o (10V/div, ground reference out of scale), sampling signal S_{PLL} and PLL signal θ_m with P_o = 240 W (Horizontal scale = 2ms/div).

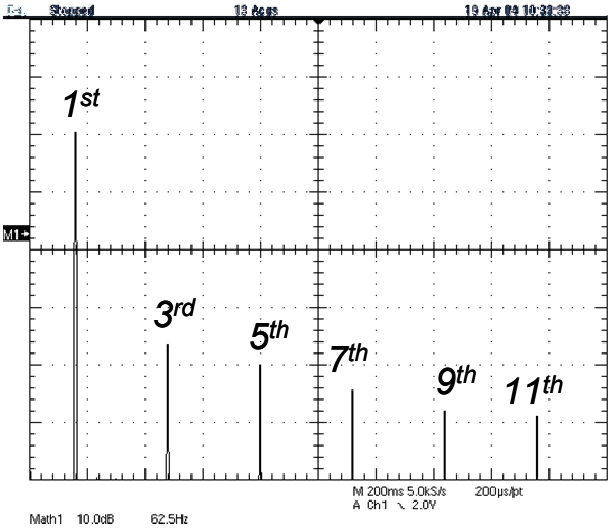

Fig. 8 - Normalized line current spectrum at the nominal load (Vertical scale: 10 dB/div, horizontal scale: 62.5 Hz/div)

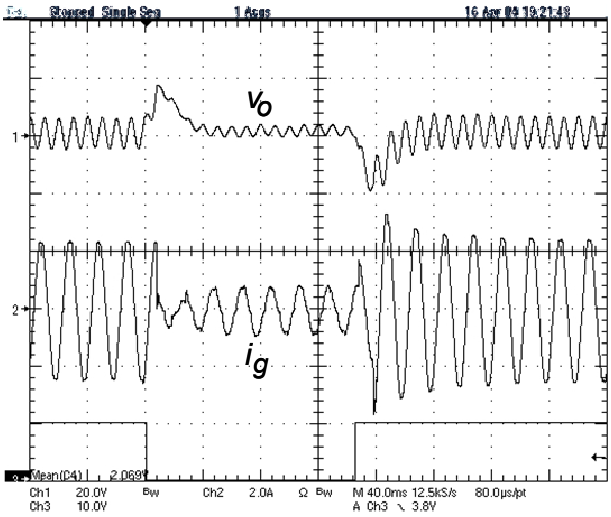

Fig. 9 – Ouput voltage v_o (20V/div, ground reference out of scale), input current i_g (2A/div) with step load changes (P_o = 240 W→ 80 W→ 240 W) (Horizontal scale = 40ms/div).

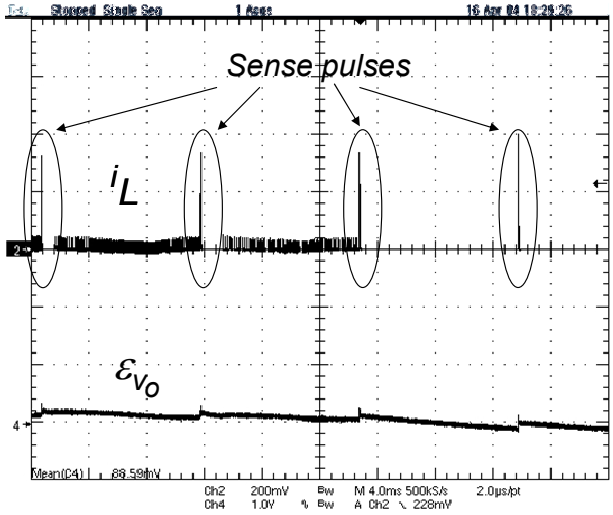

Fig. 10 – Inductor current i_L (800mA/div) and output voltage error ε_{vO} (1V/div) at light-load (P_o = 1.4 W). Horizontal scale = 4ms/div.

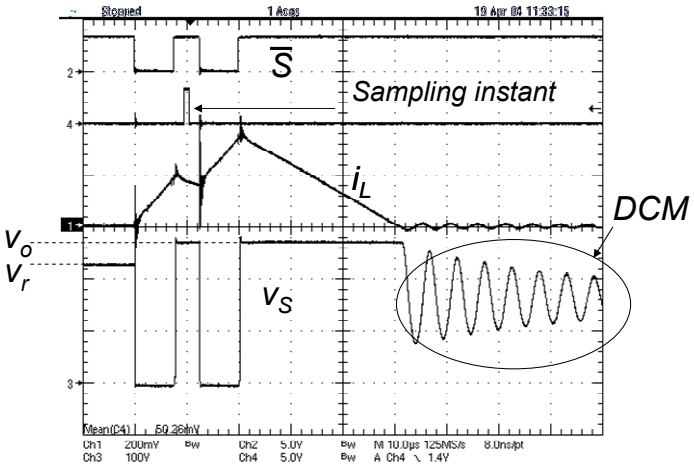

Fig. 11 – Output voltage sampling during a "sense pulse". From top to bottom: driver signal (inverted), sampling signal, inductor current i_L (800mA/div), switch voltage v_S (100V/div). Horizontal scale = 10µs/div)

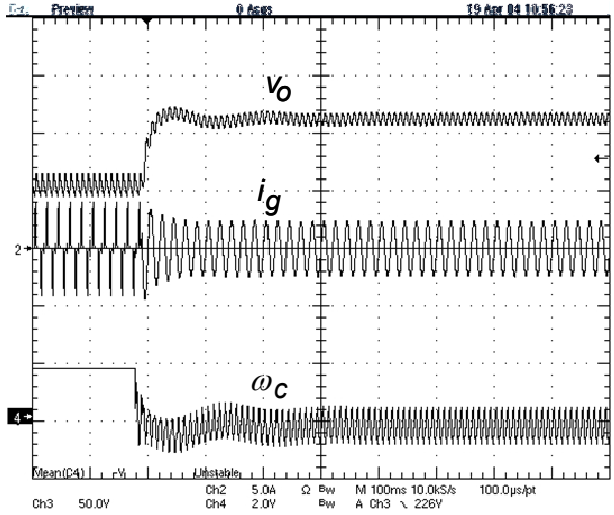

Fig. 12 – Output voltage v_o (50V/div), input current i_g (5A/div), output of PLL regulator F_{PLL} at start-up of PFP control.
(Horizontal scale = 100ms/div)

V. CONCLUSIONS

This paper has proposed a digital control of boost PFPs based on voltage and current measurements at switch terminals only. This solution is suitable for smart-power integration where an intelligent power switch with minimum pin count can substitute the main power switch and all control circuitry. The control algorithm requires the estimation of the rectified input voltage, that is simply done by exploiting the integral part of the current loop PI regulator, and a PLL for the synchronization with the estimated line frequency. The most critical part is the protection procedure for ensuring diode conduction during output voltage sampling even during transient conditions. Moreover, a minimum load is needed, even if very small. Experimental results have verified the performance of the proposed solution.

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REFERENCES

[1] B.J. Patella, A. Prodic, A. Zirger, D. Maksimovic, "High-frequency digital controller IC for dc/dc converters", *IEEE Trans. on Power Electronics*, Vol. 18, No. 1, January 2003, pp. 438-446.

[2] J. Xiao, A.V. Peterchev, S.R. Sanders, "Architecture and IC implementation of a digital VRM controller", IEEE Trans. on Power Electronics, Vol. 18, No. 1, January 2003, pp. 356-364.

[3] A. De Castro, P. Zumel, O. Garcia, T. Riesgo, J. Uceda, "Concurrent and Simple Digital Controller of an AC/DC Converter with Power Factor Correction", *IEEE Trans. on Power Electronics*, Vol. 18, No. 1, January 2003, pp. 334-343.

[4] A. Prodic, J. Chen , R. W. Erickson, D. Maksimović, "Digitally Controlled Low-Harmonic Rectifier Having Fast Dynamic Responses", *IEEE Applied Power Electronics (APEC) 2002*, Dallas, February 2002, pp. 476 - 482.

[5] S. Buso, P. Mattavelli, L. Rossetto, G. Spiazzi "Simple Digital Control Improving Dynamic Performances of Power Factor Preregulators", *IEEE Trans. on Power Electronics*, Vol. 13, No. 5, September 1998, pp. 814-823.

[6] M. Fu, Q. Chen, "A DSP based Controller for Power Factor Correction (PFC) in a Rectifier Circuit", *IEEE Applied Power Electronics (APEC) 2001*, Anaheim, March 2001, pp. 144 – 149.

[7] Y.T. Feng, G. L. Tsai, Y.Y. Tzou " Digital Control of Single Switch Flyback PFC ac/dc Converter with Fast Dynamic Response", *IEEE Power Electronics Specialists Conference (PESC)*, 2001, pp. 1251-1256.

[8] A. H. Mitwalli, S.B. Leeb, G. C. Verghese, V. J. Thottuveilil, "An Adaptive Digital Controller for a Unity Power Factor Converter", *IEEE Trans. on Power Electronics*, Vol. 11, No. 2, March 1996, pp. 374-382.

[9] A. Prodic, D. Maksimovic and R. Erickson, "Dead- Zone Digital Controller for Improved Dynamic Response of Power Factor Preregulators", *IEEE Applied Power Electronics (APEC)*, Miami, Feb 2003, pp. 382 - 388.

[10] K. De Gussemé, D. Van de Sype, A. Van den Bossche and J. Melkebeek, "Sample Correction for Digitally Controlled Boost PFC Converters Operating in both CCM and DCM", *IEEE Applied Power Electronics (APEC)*, Miami, Feb 2003, pp. 389 - 395.

[11] P. Mattavelli, G. Spiazzi, P. Tenti, "Predictive Digital Control of Power Factor Preregulators using Disturbance Observer for Input Voltage Estimation," *Proc. of IEEE Power Electronics Specialists Conf. (PESC)*, Acapulco, June 2003, pp.1703-1708.

[12] P. Mattavelli, G. Spiazzi, P. Tenti, "Digital Control of Power Factor Preregulators with Input Voltage Estimation," *IEEE 7th Brasilian Power Electronics Conference (COBEP)*, September 2003, Fortaleza, Brasil.

[13] J. Rajagopalan, J. G. Cho, B. H. Cho, F.C. Lee, **"**High performance control of single-phase power factor correction circuits using a discrete time domain control method", IEEE APEC'95, pp. 647-653.

[14] I. Agirman, V. Blasko, "A Novel Control Method of a VSC without AC Line Voltage Sensors", *IEEE Trans. on Industry Applications*, Vol. 39, no. 2, pp. 519-524, March/April 2003.