On the Applications of Active Filters to Generic Loads

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Abstract - **The paper discusses the application of parallel active filters to the compensation of generic loads. In particular, attention is focused on the potential instability which can occur in the compensating system in the presence of a capacitive load impedance. This problem is illustrated in the case of a typical active filter implementation but the analysis is extended also to other control strategies discussed in the literature. Some of these are shown to improve the system's stability, although at the expense of an increased interaction with the utility grid. The modulation technique of the power converter implementing the active filter also plays a key role in determining the system's robustness and the quality of the compensation. The last part of the paper discusses the effectiveness of the more common current control strategies both from the stability and from the compensation quality standpoint.**

I. INTRODUCTION

Applications of active power filters have undergone a remarkable development since the power electronics technology based on fast switching power devices has become available. As known, active filters can be used to supply leading and lagging reactive power, to compensate current harmonics, unbalance, and possibly flicker of non-linear and fluctuating loads [1], [2]. However, the great potentialities of active power filters have so far been used mainly to compensate individual non-linear loads, typically thyristor rectifiers with smoothing inductors. Many issues regarding topologies, compensation strategies, current control techniques have been investigated in the past for this kind of applications.

In the last few years, the application of active filters on a larger scale has gained increasing attention. This is due to the need of either the utility or the customer to provide an active power device able to compensate harmonics, unbalance and flicker for a given group of loads, which may possibly be located far away from the point of installation of the active filter. The loads to be compensated are, of course, unknown and may even include some internal reactive and/or resonant compensation system.

This kind of application, which refers to the so-called "custom power" concept, poses new and interesting problems for the design and control of active power filters, which mainly derive from the different and unknown configurations under which the load can present itself, and from the wide load power rating, ranging from a few kVA's to some MVA's. The most relevant issues concern the choice of the *compensation strategy*, the selection of the *modulation technique* and *EMI filters* and the choice of the *active filter topology*.

The paper presents a comparative analysis of the solutions proposed for the former two issues, while the selection of the filter topology is not considered, assuming that a parallel active filter is the chosen option. Indeed, for the application to the compensation of generic loads, both series active filters and hybrid solutions [5]-[8] can be considered, but will not be discussed here.

Regarding the compensation strategy, we recall [3], [4], [9] that, using the classical load current detection method or, equivalently, the supply current detection method, even a small capacitor in the load, rated at a few percent of the nominal power, may cause the instability of the system. We also show that providing a line current proportional to the line voltage instead of a purely sinusoidal waveform can contribute to the attenuation of the aforementioned instabilities. Compensation strategies based only on voltage detection methods [3], [4], [11] are not affected by the aforementioned instabilities, but their application implies an increased interaction with the supply voltage harmonics and thus is limited mainly to the damping of harmonic propagation in power distribution systems and is less suited for the compensation of a specific group of loads.

A key role in determining the system's robustness is played by the current control technique; in fact, as it will be

shown, the dynamic response of the current loop may directly affect the aforementioned instabilities. It is therefore extremely important to select an high performance current control strategy in order not to aggravate the problem. Moreover, the quality of the compensation in terms of residual harmonic content in the line current is also largely dependent on the current loop performance. Therefore, in the last part of the paper a critical analysis of some widely used current control strategies is presented. Among the digital-deadbeat current control, sine-triangular current control, possibly used in the d-q reference frame, and the fixed frequency hysteresis current control, the last one provides, of course, the best performance. However, the differences among these solutions are not so small as expected especially if the load is composed, for a non-negligible part, by thyristor rectifiers. In this case we show, through numerical simulations, how the THD of the line current can strongly change depending on the adopted current-control.

II. Review and Stability Analysis of Conventional Control Strategies

Fig. 1 shows an equivalent circuit of a parallel active filter compensating a generic load. The analysis assumes that the supply network is represented by an internal voltage e_S with a series impedance Z_S and the active filter by a current generator i_{FA} driven, with a delay mainly determined by the current control loop, by a current reference i_{FA}*. Instead, the load is represented by a Norton equivalent circuit, where the current generator indicates the purely distorting load and impedance Z_L the passive components of the load, which may also include the possible capacitive compensation. Note that also diode rectifiers with purely capacitive filters exhibit a low impedance component during diode conduction. Indeed, these assumptions are a very rough approximation of the actual system's behaviour, but they are complete enough to present and understand the typical instabilities which occur in the practical system, when generic loads include low-impedance components. In fact, when it is not possible to measure the purely distorting current i_L, the conventional compensation strategy, based on the total load current i_{LT} measurement, may imply the instability of the system, if Z_L includes a capacitive component, as shown in [3], [4], [9]. In fact, denoting the harmonic content of the line current by i_{LTh} and imposing the constraint:

$$i_{FA}^{*} = -i_{LTh} \qquad (1)$$

which implies the compensation by the active filter of any harmonic current drawn by the load, the block diagram depicted in Fig. 2 can be derived. Referring to Fig. 2 the open loop gain for the system can be calculated and Bode or Nyquist plots can be drawn to analyse the system's stability. The transfer function F(s) is intended to represent an ideal notch filter which eliminates only the fundamental component from the feedback signal. Transfer function G(s), as can be easily seen by Fig. 1, is instead given by:

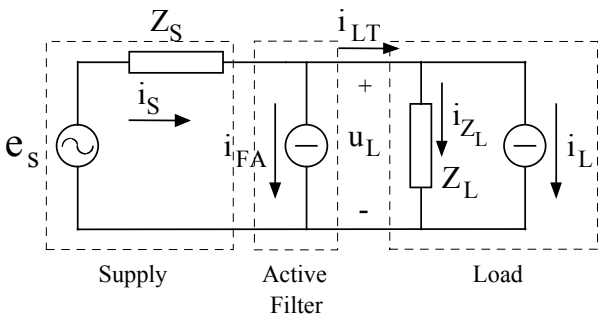

Fig. 1 - Simplified configuration of a parallel active filter compensating a generic load

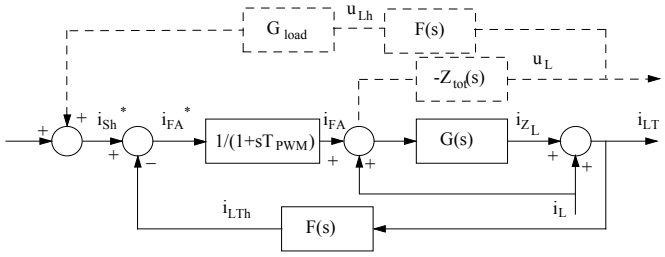

Fig. 2 - Load current detection method: dotted lines represent the active damping. $Z_{tot}(s) = Z_L(s) \,//\, Z_S(s)$

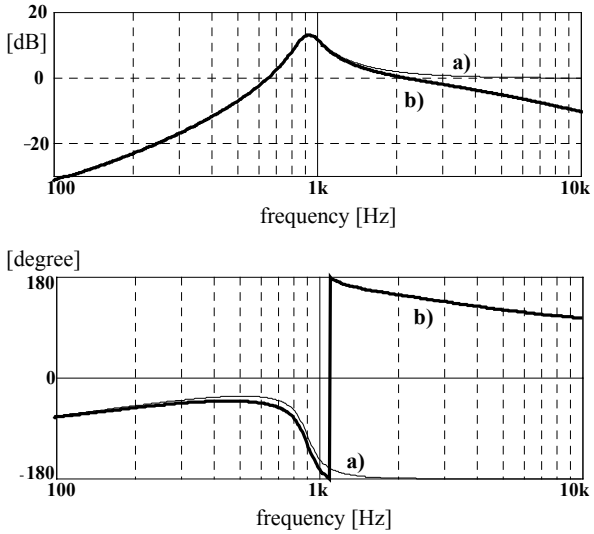

Fig. 3 - Load current detection method: ($Z_S=R_S+sL_S$, $Y_L=G_L+sC_L$; L_S=0.03pu, L_S/R_S=10, C_L=0.10pu, G_L=0.4pu)
a) load current harmonic compensation without control delay
b) load current harmonic compensation with control delay (T_{PWM}=0.6ms)

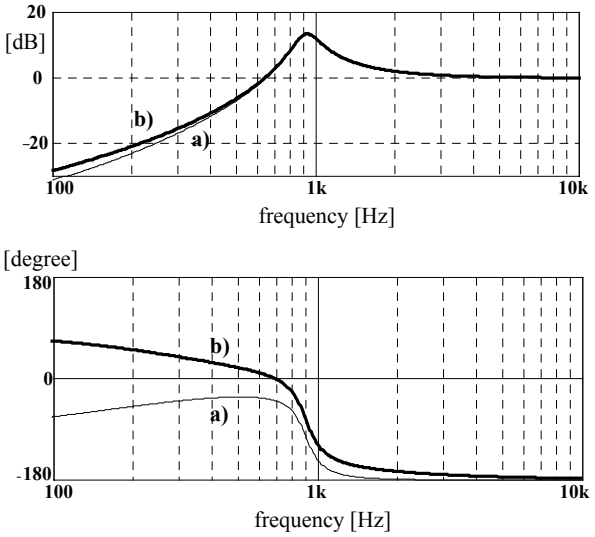

Fig. 4 - Effect of the active damping: ($Z_S=R_S+sL_S$, $Y_L=G_L+sC_L$; G_{load}=1pu, L_S=0.03pu, L_S/R_S=10, C_L=0.10pu, G_L=0.4pu)
a) load current harmonic compensation without control delay
b) resistive absorption without control delay

$$G(s) = -\frac{Z_S(s)}{Z_S(s)+Z_L(s)} \qquad (2)$$

As can be seen in Fig. 3, the loop gain exhibits a very small phase margin at those frequencies where the possible current loop delay is effective. A very small delay can therefore bring the system to instability. Fig. 3 also shows the resulting Bode plot when a pole is inserted in the loop to model the delay introduced by the current control. The outcoming system is clearly unstable (bold line).

It is worth noting that the resulting instability is *inherent* in the active filter's control strategy, which tries to cancel any of the load harmonic currents, even if, as in the considered case, the capacitive component of the load impedance is quite small (0.10pu). A certain improvement in the system stability can be provided if a damping function is added to the active filter control strategy, as shown by the dotted line in the diagram of Fig. 2, where G_{load} is the damping coefficient. This function is inherently implemented when a line current proportional to the load voltage is chosen as the active filter

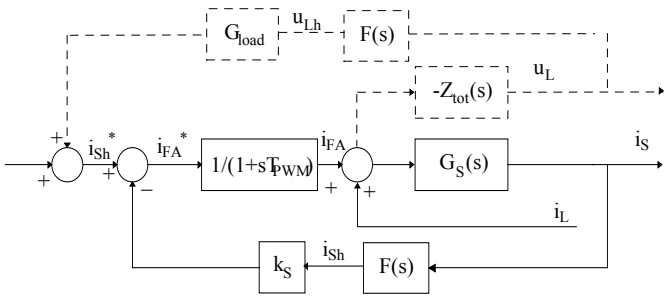

Fig. 5 - Supply current detection method: dotted lines represent the active damping. $Z_{tot}(s) = Z_I(s) \,//\, Z_S(s)$, $G_s(s)=Z_I(s)/(Z_I(s)+Z_s(s))$

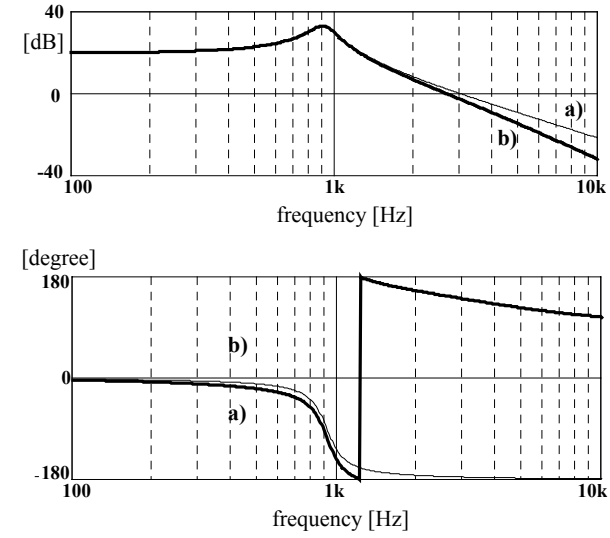

Fig. 6 - Supply current detection method: ($Z_S=R_S+sL_S$, $Y_L=G_L+sC_L$; k_S=10, L_S=0.03pu, L_S/R_S=10, C_L=0.10pu, G_L=0.4pu)
a) without control delay;
b) with control delay (T_{PWM}=0.5ms)

control strategy. In this case, as can be seen in the Bode diagram shown in Fig. 4, the phase margin is slightly increased, but, anyway, this provision is not a solution to the problem. Even if bigger than before, the phase margin is in fact still not sufficient to guarantee the system's stability. To further clarify the generality of this point a similar analysis is done for a different control strategy, sometimes encountered in practical implementations, which is based on the supply current measurement. In this case, by imposing:

$$i_{FA}^{*} = -k_S\, i_{Sh} \qquad (3)$$

where k_S is a sufficiently high gain, the block diagram depicted in Fig. 5 can be obtained. Again, the calculation of the open loop gain allows to derive the Bode plot depicted in Fig. 6, which demonstrates the potential instability of the system, particularly evident when the control delay is explicitly taken into account in the calculation of the open loop gain (bold line). Also in this case a damping action in the active filter control can slightly improve the stability margin.

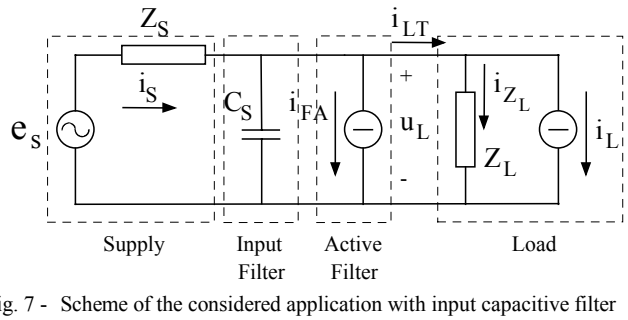

Fig. 7 - Scheme of the considered application with input capacitive filter

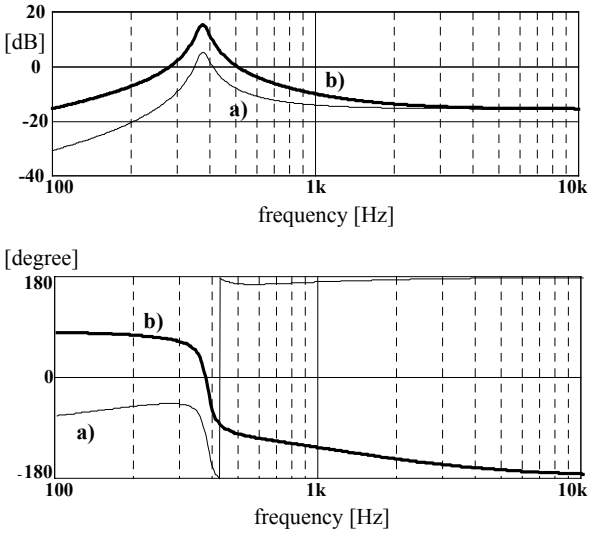

Fig. 8 - Load current detection method with a capacitor on the line side: ($Z_S=R_S+sL_S$, $Y_L=G_L+sC_L$; $L_S=0.03$pu, $L_S/R_S=10$, $C_L=0.10$pu, $C_S=0.5$pu,$G_L=0.4$pu)
a) without active damping;
b) with an active damping kv=3pu

III. Summary of Possible Alternative Approaches

This section of the paper presents some alternative approaches for the control of the active filter, which can somewhat improve the system's stability.

A. Input capacitive filter

As shown in [10], the insertion of a properly sized capacitor on the line side, as shown in Fig. 7, is a potential solution for the aforementioned instabilities. Indeed, this solution modifies the transfer function G(s) so that a better stability margin can be achieved, as shown in Fig. 8. Note, however, that even a 0.50pu value for C_S does not give the desired improvement even with a small load capacitor (C_L=0.10pu). A better phase margin is obtained when the filter C_S is combined with an active damping action implemented by the active filter, as shown by the thick line of Fig. 8. However, even in these conditions, a big filter capacitor is needed to achieve the desired stability margin.

A considerable improvement can be achieved without physically connecting a filter capacitor at the input of the compensating system by "virtually" generating a capacitive current absorption from the grid by means of the active filter itself, whose reference current will include a term proportional to the time derivative of the input voltage. This

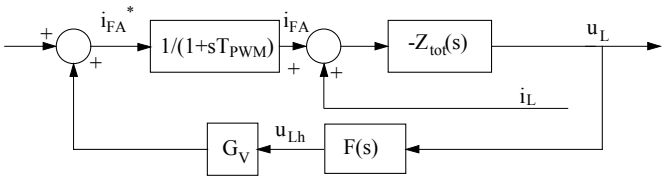

Fig. 9- Supply voltage detection method. $Z_{tot}(s) = Z_L(s) // Z_S(s)$

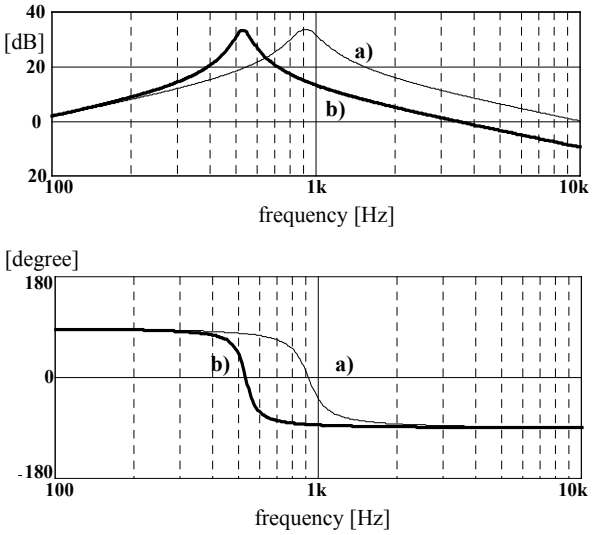

Fig. 10 - Supply voltage detection method: ($Z_S=R_S+sL_S$, $Y_L=G_L+sC_L$; $G_V=20$, Ls=0.03pu, L_S/R_S = 10, C_L=0.10pu, G_L=0.4pu)
a) C_L=0.10pu;
b) C_L=0.30pu

solution tends to cancel the feedback loop shown in Fig. 2. This can be an effective solution if the capacitive component of the load is limited to a given amount and the "virtual" capacitor offered by the active filter is set equal to the maximum capacitive component of the load. Note that even this solution increases the interaction with the voltage harmonics, as the solutions hereafter reported.

B. Voltage Sensing Based Methods

A different control strategy for the active filter is the one proposed in [3], [4], where the line voltage is used to derive the current reference for the active filter, as shown in Fig. 9. The same loop gain evaluation done in the previous cases reveals for this solution a very good phase margin (close to 90°), as shown in Fig. 10 for two different values of the capacitive load impedance. This solution is, however, well suited for the compensation of very high power loads, but it is not possible to use it to compensate a load, or a group of loads, having a power rating much smaller than the power rating of the line they are connected to. This, indeed, would require a considerable oversizing of the compensation system

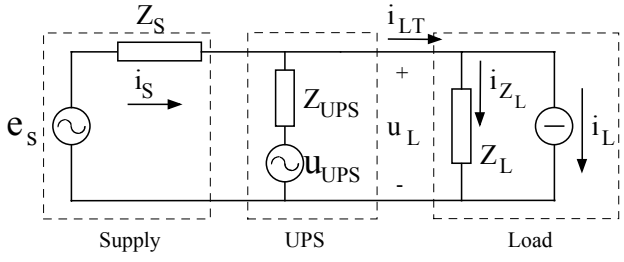

Fig. 11 - Scheme of the *voltage source* solution

to cope with the interaction with the power line or, in alternative, the use of considerable series reactive impedances to reduce such interaction.

An alternative approach is the one proposed in [11] and shown in Fig. 11. The solution to the stability problem is found in the implementation of a stabilised voltage source capable of having a smaller impedance than the power line in the frequency range of interest. With this scheme, the harmonic currents drawn by the load are supplied by the stabilised voltage source rather than by the line, thus achieving the harmonic compensation. Of course the limitation to the application of this solution is, as in the previous case, the need to oversize the converter. Besides, the output capacitor of the voltage source must be considerably rated, in order to offer to the harmonic currents a lower impedance than the one offered by the line, when the output voltage control bandwidth is exceeded. This solution has, however, some potential advantages when the active filter must behave as an UPS during possible line voltage sags.

C. Off-line Reference Calculation

When the load behaviour can be considered slowly varying, it is possible to adopt the off-line generation of the active filter current reference, based on the FFT evaluation of the load current. By compensating only the slowly varying harmonic content of the distorting current and by limiting the maximum harmonic order of the compensation, it is possible to reduce the effects of the stability problem. In fact, even if the harmonic compensation is performed with a delay equal to a supply period, the aforementioned potential instability is still present.

IV. An Example of Active Filter Instability

This section presents some simulation results showing how the aforementioned instabilities may occur also in the compensation of a common three-phase diode rectifier with capacitive output filter. The considered situation is quite different from the cases discussed above, since the load is highly non-linear, and is presented only as an illustrative example. A parallel active filter, implemented with an hysteresis current control, compensates the harmonics generated by the diode rectifier, which adopts a capacitive output filter C_{dc} (C_{dc}=680μF) and supplies a load rated 1kW. A small inductor filter L_f (L_f=500μH) is connected at the input of the distorting load, fed at $380V_{rms}$ phase-to-phase voltage. The line impedance is supposed to be inductive (L_s=4mH) and a small filter capacitor (C_s=5μF) is used to eliminate the high frequency harmonic components from the line current. Fig. 12 clearly shows an unstable behaviour during diodes' conduction. Indeed, when the load current is zero because the rectifier diodes are off, the active

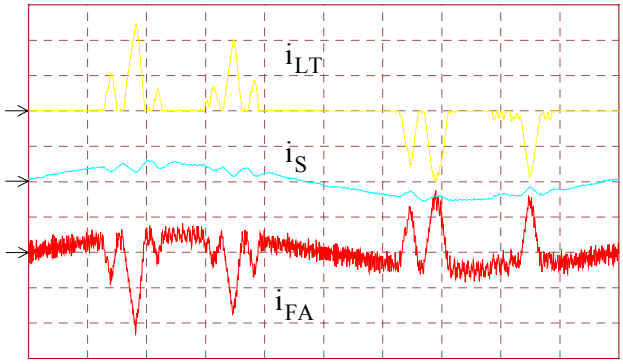

Fig. 12 - Simulated active filter behaviour; i_{LT} (6 A/div.), i_S (6 A/div), i_{FA} (6 A/div); time scale (2 ms/div.)

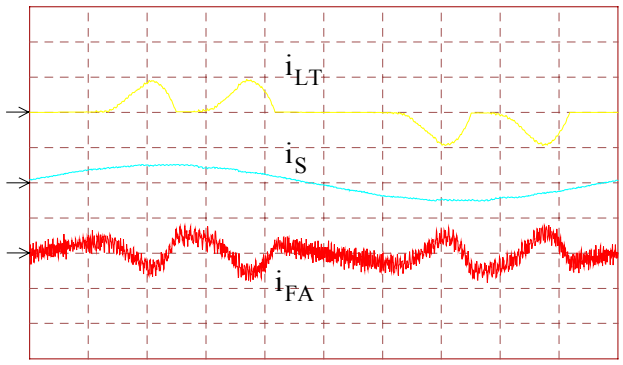

Fig. 13 - Simulated active filter behaviour ; i_{LT} (6 A/div.), i_S (6 A/div),. i_{FA} (6 A/div), time scale (2 ms/div.)

filter is able to control the supply current i_s, which appears almost sinusoidal. Instead, when the diodes are conducting, the active filter load presents a capacitive impedance, which destabilizes the system. Consequently, oscillations appear on the current waveforms. A straightforward strategy to remove these oscillations is to increase the filter inductor at the input of the diode rectifier (L_f=2mH) thus reducing the capacitive impedance of the load. In this particular case, this provision eliminates the instability, as clearly shown by Fig. 13.

V. Review of Current Control Techniques

The stability analysis presented in section II revealed the very important part played by the current control strategy, adopted for the active filter implementation, in determining the stability margin of the system. It is possible to see that the current control delay gives a decisive contribution in the determination of the residual phase margin of the system. If, for instance, a conventional dead-beat current control technique is used, an additional phase margin reduction corresponding to the typical two-cycle delay of the algorithm must be taken into account. Depending on the adopted switching and sampling frequency, this can represent an unacceptable deterioration of the stability margin of the system. It is therefore critical to select the current control

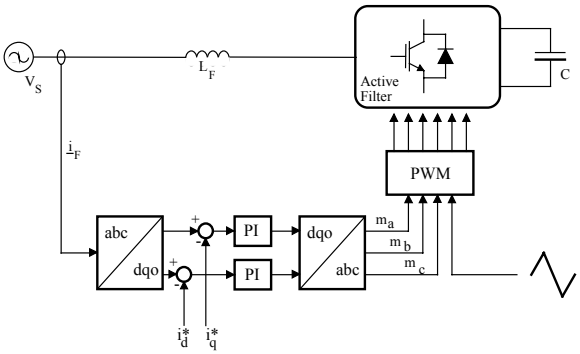

Fig. 14 - Basic scheme of a linear rotating frame current regulator; $\underline{i}_F$ is the active filter current vector (abc frame)

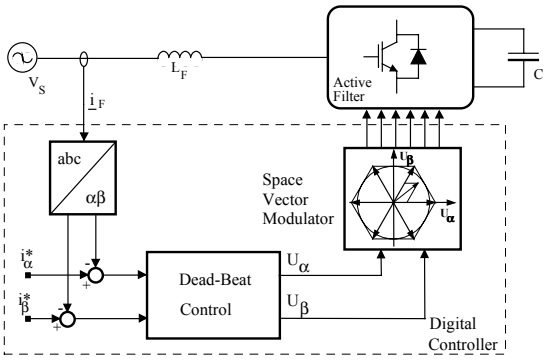

Fig. 15 - Basic scheme of a digital dead-beat current regulator $\underline{i}_F$ is the active filter current vector

strategy that potentially offers the fastest dynamic response. Moreover, even if no stability problems are encountered, the quality of the achieved compensation is greatly affected by the dynamic performance of the current control. To evaluate these aspects, a comparison of the more commonly adopted current control strategies is now proposed [12]-[17].

A. Linear Current Control

The conventional version of the linear current controller, performs a sine-triangle PWM voltage modulation of the power converter using the current error filtered by a proportional-integral (PI) regulator as the modulating signal. Differently, recent versions of the linear current control exploit the d-q rotating frame [18]-[21]. Control variables are mapped into the rotating frame, according to the scheme represented in Fig. 14. The main advantage of such a solution is that the fundamental harmonic components of voltage and current signals appear constant to the current regulator. Therefore, the line voltage, which is almost sinusoidal, is seen by the current regulator as a constant quantity. As a consequence, the rejection of this disturbance is much more effective. On the other hand, the well known bandwidth limitation of the PI regulators, which remains unchanged, still implies significant errors and delays in the tracking of the high order harmonic components of the current reference. In active filter applications these errors usually reflects in a not completely satisfactory harmonic compensation's quality.

B. Digital Dead-Beat Control

As it is described in [22] an effective exploitation of the advantages of the digital current control can be achieved by adopting an improved version of the well known dead-beat control technique [23]-[27]. In the conventional implementation the digital control calculates the phase voltage so as to make the phase current reach its reference by the end of the following modulation period [28], [29]. The calculations are often performed in the α, β frame, and the space vector modulation (SVM) strategy, which suits the digital implementation very well, is applied to the switching converter. This is essentially the situation depicted in Fig. 15. An important advantage of this technique is that it may not require the line voltage measurement in order to generate the current reference. Indeed, the dead-beat control's algorithm implies an estimation of the line voltage instantaneous value, which can therefore be used also for the current reference generation. On the other hand, the inherent delay due to the calculations is indeed a serious drawback for this technique [22]. Due to the high required speed of response it becomes the main limitation in active filter applications and may imply an unsatisfactory performance level.

C. Hysteresis Control

The basic implementation of the hysteresis current controller derives the switching signals from the comparison of the current error with a fixed hysteresis band. Though simple and extremely robust, this control technique exhibits several unsatisfactory features. The main one is that it produces a varying modulation frequency for the power converter. This is in general responsible for various problems from the difficulty in designing the input filters to the generation of unwanted resonances on the utility grid. Another negative aspect of the basic hysteresis control is that its performance is negatively affected by the phase currents'

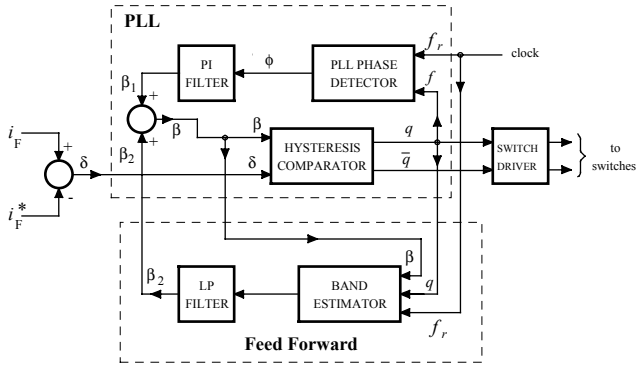

Fig. 16 - Basic scheme of an hysteresis current regulator

interaction typical of three phase systems with insulated neutral. Anyway, a lot of improvements to the original control structure have been suggested by industrial applications. First of all, phase current decoupling techniques have been devised. Secondly, fixed modulation frequency has been achieved by a variable width of the hysteresis band as function of the instantaneous output voltage. Fig. 16 shows the simplified scheme of the implementation of such a controller. As can be seen, the controller modifies the hysteresis band by summing two different signals. The first is the filtered output of a PLL phase comparator (β_1), the second is the filtered output of a band estimation circuit (β_2). The band estimator implements a feedforward action that helps the PLL-based circuit to keep the switching frequency constant; in this way, the output of the PLL circuit only provides the small amount of the modulation of the hysteresis band which is needed to guarantee the phase lock of the switching pulses with respect to an external clock signal. This ensures also the control of the mutual phase of the modulation pulses. All of these provisions have allowed a substantial improvement in the performance of the hysteresis current controller, as it is widely discussed in [30].

VI. Comparative Simulation of the Current Controllers

This section of the paper presents some simulations illustrating the main issues so far discussed. The ratings of simulated system used for the evaluation of the current controllers' performance are reported in Table I. The considered situation is a typical, high demanding, application

Table I - Simulated System Ratings

Input Voltage	$V_S = 380V_{RMS}$
Rectifier Load Rated Power	$P_n = 100kW$
Rectifier Input Inductor	$L_R = 100\mu H$
Rectifier Load Inductor	$L = 750\mu H$
Rectifier Load Current	$I_L = 150A$
Switching Frequency	$f_{SW} = 10kHz$
Active Filter Inductor	$L_F = 250\mu H$
Active Filter DC Link Capacitor	$C = 2500\mu F$
Active Filter DC Link Voltage	$E = 750V$

of a parallel active filter for the compensation of a thyristor rectifier with inductive load. This situation is the more suited to highlight the differences in the dynamic performance of the various current controllers. The presence of step changes in the load current allows to immediately evaluate the dynamic speed of response of the active filter, that, as was previously said, directly affects the stability of the system when applied to the compensation of generic loads, and, in general, determines the quality of the compensation of harmonic currents injected in the line by any distorting load.

Fig. 17, 18 and 19 describe the system's operation with the linear, digital dead-beat and hysteresis control respectively, all for the same firing angle of the thyristor rectifier (α=40°). In particular, the upper part of each figure shows the relevant system's waveforms; these are the line voltage V_S, the line current i_S, the rectifier current i_{LR}, the active filter current i_F superimposed to its reference i_F^*, and the current error ε_S. On the figure bottom, the corresponding line current spectrum, referred to the amplitude of the fundamental current, is shown. As far as the linear control is concerned (Fig. 17), it is possible to notice the relevant effect, in terms of current error, of the sudden change in the slope of the load current. For this controller, as it was said before, the main limitation is represented by the quite low achievable bandwidth of the linear regulator. In this case the bandwidth is about 2.5kHz. It is worth noting that, since the modulation frequency of the power converter is 10kHz, this value is pretty close to the limit beyond which stability problems may

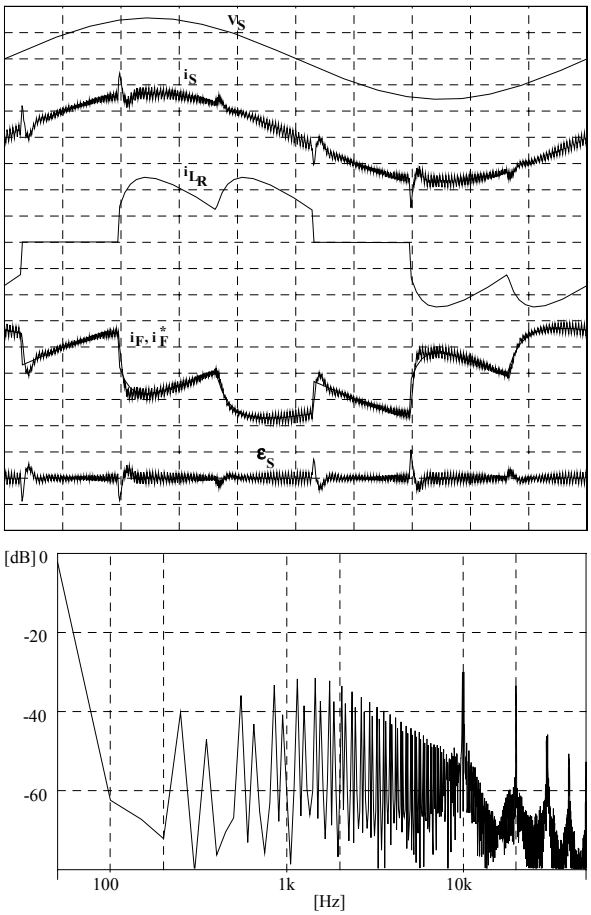

Fig. 17 - Top: simulated active filter behaviour with α=40° and linear control
i_S (150 A/div.), ε_s (75 A/div.), t (2 ms/div.)
Bottom: line current i_S spectrum

arise. Accordingly, the position of the PI zero is about 1460Hz, where the open loop gain is about 1.7, so as to guarantee a proper phase margin (60°). Anyway, due to the control's delay the compensated current exhibits significant residual errors in the presence of load current's step variations. The quality of the compensation is especially degraded in the high frequency range of the spectrum, where the effect of such variations in the current waveform is particularly evident. It is therefore possible to see that the linear controller may not be recommended for the application to active filters, because of its inherently slow dynamic response.

Fig. 18 reports the results of the system's simulation with the dead-beat controller. Note that the considered implementation uses a double-prediction algorithm for the calculation of the current reference that minimises the control's delay. As the load power is unchanged, the current reference practically coincides with that of the linear control. As can be seen, also the dead-beat regulator exhibits a not very satisfactory compensation quality. Because of the residual compensation errors the harmonic content of the line current is particularly relevant in the high frequency range, demonstrating a substantial delay in the response to the step changes in the load current. Therefore, also the dead-beat controller may have stability problems if applied to the compensation of generic loads.

TABLE II
RMS CURRENT ERROR AND LINE CURRENT THD

	Linear Control	Dead Beat Control	Hysteresis Control
RMS [%]	7.68	7.04	1.63
THD [%]	7.64	6.98	1.45

Finally, Fig. 19 describes the behaviour of the hysteresis controller. All the details concerning the controller's design can be found in [30]. As it can be seen, for this control technique, the quality of the harmonic and reactive power compensation is better than the previous cases. The speed of response of this controller is maximum, which, in case of application to the compensation of generic loads, allows to get the largest stability margin.

The comparison of the simulation results can be performed by evaluating also the current error RMS value and the line current total harmonic distortion (THD). Both the RMS value and the total harmonic distortion have been calculated in the range of the harmonic components up to a frequency of 2kHz, as required by IEC standards. This choice is justified also by the fact that the high frequency harmonic components due to the modulation process are always practically eliminated by means of suitable passive filters.

The normalised RMS value of current error and the total harmonic distortion of the line current, both related to the amplitude of the fundamental component of the input current, are given in Table II. As can be seen, the significant superiority of the hysteresis current control technique is confirmed by the reported data.

In conclusion, as far as the compensation quality and the previously discussed stability issues are concerned, the performance of the linear and dead-beat controllers may not be in any case adequate. The hysteresis control, by keeping the harmonics about 60dB below the fundamental level, seems to be able to guarantee the fastest dynamic response and therefore the highest stability margin. This superiority is also confirmed by the data reported in Table II, where both the current total harmonic distortion and the error RMS value are much lower than those of the linear and dead-beat controls. The difference between the hysteresis controller performance and that of the other controllers is, of course, related to the firing angle of the rectifier and, in general, increases when the phase angle is increased.

It is also possible to notice that the performance of the

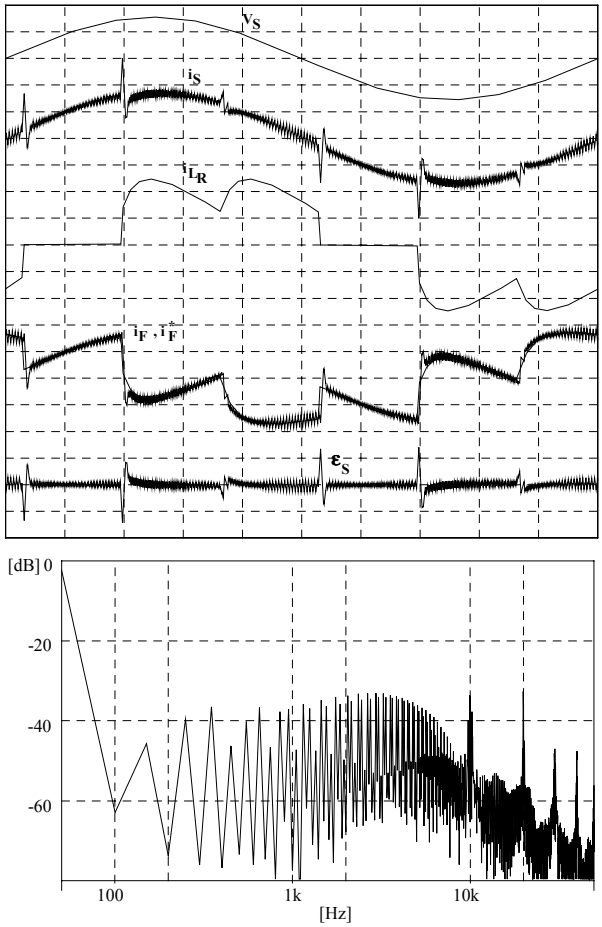

Fig. 18 - Top: simulated active filter behaviour with α=40° and dead-beat control; i_S (150 A/div.), ε_s (75 A/div.), t (2 ms/div.)
Bottom: line current i_S spectrum

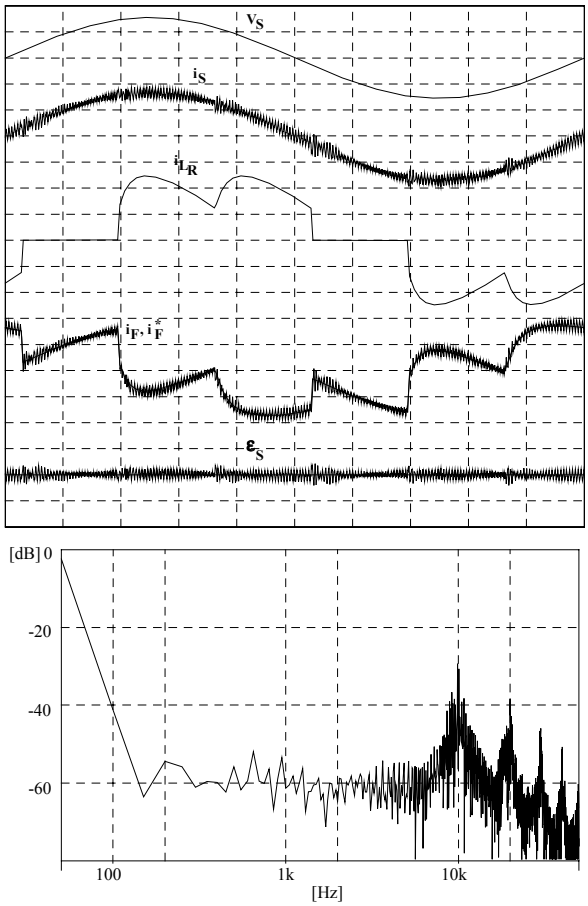

Fig. 19 - Top: simulated active filter behaviour with α=40° and hysteresis control
i_S (150 A/div.), ε_s (75 A/div.), t (2 ms/div.)
Bottom: line current i_S spectrum

linear and of the dead-beat controllers turn out to be quite similar, with a slight superiority for the dead-beat controller. Both are not able to offer a sufficiently fast dynamic response, which makes their application not recommendable, in any case when the stability margin of the compensation system is critical.

VII. CONCLUSIONS

The application of parallel active filters to the compensation of generic loads poses interesting control and design problems. The paper shows that, when the load configuration is unknown and capacitive load impedances can be expected, the conventional active filter control strategies, based on line or load current sensing, are potentially unstable. The stability margin of the compensation system is calculated for a small capacitive load impedance and results to be rather poor. Because of that, the delay in the implemented active filter current control loop is a truly critical factor in determining the stability of the system. Different control strategies are analysed, which allow to significantly increase the stability margin, but pay this positive effect at the expense of an increased interaction with the utility grid. This, consequently, makes the application of these compensating systems suited mainly for large power distribution systems, or in those cases where the line power rating is comparable with the load power rating. A significant oversizing of the power converter or the insertion of decoupling inductive reactances are otherwise necessary to cope with the interaction with the line. To conclude the analysis, a review of the most common current control strategies is proposed, whose aim is to highlight the differences in the dynamic performance of the various techniques in an active filter application. The comparison is performed by simulating a typical situation where the distorting load to be compensated is a thyristor rectifier.

The results of the comparison show a clear superiority of the hysteresis control. Indeed, the performance of this control strategy is, on the basis of the indexes considered in the paper (line current spectrum, THD and RMS value of current error), better than those of the other techniques. The dead-beat controller, which has the advantage of being suitable for a fully digital implementation, is limited in its performance by the inherent calculation delay. Similarly, the linear control's bandwidth limitation turns into a not completely satisfactory compensation's quality especially in the presence of high *di/dt* in the current reference.

Therefore, the hysteresis control strategy seems to be the most indicated for the application to the compensation of generic loads, since it minimises the control's delay which affects the system's stability.

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