Dead-Beat Current Control for Active Filters

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Abstract - **The paper discusses the main issues concerning the implementation of digitally controlled parallel active filters. The considered control strategy is based on the combination of dead-beat control of inverter currents and space vector modulation. For an active filter application, key features of the power converter's control are the achievable harmonic compensation quality (IEC standards compliance) and the robustness of the system's stability (load structure and parameter uncertainty). Both aspects are examined in the paper. As far as the former is concerned, simulations and experimental tests show that even if a high switching frequency is achieved (using a state-of-the-art DSP platform), the intrinsic calculation delay of the dead-beat algorithm represents a serious hurdle for the achievement of a satisfactory compensation quality. From the stability standpoint instead, the effects of parameter mismatches on the system's performance are investigated by means of a complete eigenvalue analysis, which allows to reveal the limits of the system's stability for different possible implementations of the considered control strategy.**

I. INTRODUCTION

The use of parallel active filters [1] for the compensation of harmonic currents and reactive power generated by distorting loads [2], such as the conventional diode or thyristor rectifiers, is becoming more and more attractive, especially for the so-called retrofit of existing converters and for particular electronic systems (i.e. telecom converters) where the reliability of the main power supply is a critical issue. Moreover, the use of fully digital control techniques is, more and more often, the chosen option thanks, on the one hand, to the well known advantages of the digital controls in terms of flexibility, insensitivity to ageing effects and/or thermal drifts, ease of implementation and upgrade, and, on the other hand, to the availability of powerful, low-cost microcontrollers (μC's) and digital signal processors (DSP's).

This paper discusses the main issues involved in the application of what is now probably the most effective digital current control technique for power converters, i.e. the dead-beat current control technique, to power active filters. A first key point in the evaluation of the control's performance in such applications, is the quality of the achievable harmonic compensation. In the work reported in this paper, this investigation is performed by means of an experimental set-up where the digital control unit is based on the combination of the ADSP21020 digital signal processor and the ADMC200 motion control board. Thanks to the speed of the adopted DSP board it is possible to implement the dead-beat control of inverter currents and the space vector modulation routine, necessary for inverter operation, in a small fraction of the modulation period. Therefore, the power converter, implementing the active filter function, can be driven at the maximum switching frequency allowed by its IGBT switches. Nevertheless, due to the inherent delay of the dead-beat control algorithm, this is not enough to achieve a satisfactory performance level. More precisely, simulations and experimental tests reveal a significant residual compensation error in the line currents, much higher than what, according to our experience, can be achieved with different current control techniques [3], [4] for the active filter.

A possible solution to reduce the compensation error is the insertion of suitably designed passive filters, as discussed in [5]. However different problems can be encountered if this solution is applied, especially as far as the system's stability is concerned. Indeed, the presence of tuned filters for the reduction of the high frequency harmonic content of the line currents and the potential occurrence of resonances between such filters and the line impedance represent a serious limitation to the achievable control's performance. More generally, the presence of model mismatches or, in case of a correctly identified model's structure, of parameter uncertainties and/or variations can cause stability problems to the current control loop, especially when a line voltage estimation strategy is adopted. This paper proposes a detailed analysis of the problem, based on a generalized discrete-time state-space representation of the controlled converter and its load. The analysis procedure reveals the stability margins of the algorithm in the case of a conventional load model and line voltage estimation technique, giving the possibility of predicting the occurrence of oscillations in the current loop by mapping the closed loop plant's eigenvalues. Besides, a modified estimation technique for the line voltage is proposed, which is shown to increase the control's robustness.

II. BASIC SCHEME OF THE SYSTEM

The basic scheme of the active filter application, which is discussed in this paper, is shown in Fig. 1. A three phase thyristor rectifier supplying an inductive load is considered. Indeed, this can be considered a significant example of the typical distorting loads whose retrofit

compensation is a potential application of parallel active filters. The harmonic content and reactive power absorption of the rectifier are reduced by a parallel active filter, implemented by using a three phase voltage source IGBT inverter. The passive elements L_1, C_1 required for filtering the harmonic components at the modulation frequency and the residual compensation errors are also shown, together with inductor L_2 which limits the current slope during thyristor commutations. In L_1 also the line impedance is included.

Branch R_2, C_2 shown in Fig. 1, indicates one of the possible configurations to smooth the resonance of the input filter. Actually, as in this case, it can be substituted by active damping obtained by a proper control of the active filter [6], [7], since oscillation frequency falls within the active filter bandwidth.

III. Control Technique

In the compensation system of Fig. 1, the control of the active filter's current is performed by means of the dead-beat control technique [8]-[10]. As it is well known, in a dead-beat controller the control algorithm calculates the phase voltage so as to make the phase current reach its reference by the end of the following modulation period. Here, the calculations are performed in the α, β frame, and the space vector modulation (SVM) strategy, which very well suits the digital implementation, is applied to the switching converter. This is essentially the situation depicted in Fig. 2. An important advantage of the dead-beat technique is that it does not require the line voltage measurement in order to generate the current reference. The dead-beat control's algorithm, in fact, allows an estimation of the line voltage instantaneous value, which can therefore be used also for the current reference generation. On the other hand, the inherent delay due to the calculation time is indeed a serious drawback in active filter applications. In particular, when compensating thyristor rectifier loads, it produces appreciable errors in correspondence of thyristor commutations. Thus, additional provisions to get to a satisfactory performance level are required. In the more recent versions [10] of the

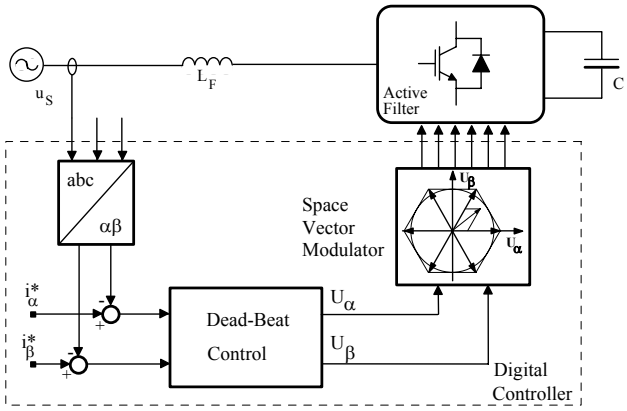

Fig. 2 - Basic scheme of the digital dead-beat current regulator

dead-beat controller, the delay may be reduced by sampling the control variables and executing the control routines twice in a modulation period. The turn-on and turn-off times of the power converter switches may be independently decided in two successive control periods. As a consequence, the aforementioned delay in current reference tracking can be reduced to a single modulation period. Due to limitations in the adopted modulator this technique could not be used in the implementation discussed in this paper.

In any case, the residual compensation errors can be reduced by a suitable value of limiting inductor L_2 and a proper design of the input passive filter L_1, C_1.

IV. Stability Analysis of the Dead-Beat Algorithm

Deadbeat control of three-phase inverter has been widely investigated by many researcher in recent years [8]-[10], especially for drive applications. The application of this control technique to active filters is almost straightforward; however, the effect of the input filters, commonly used to eliminate the high frequency harmonic currents generated by the inverter's modulation, must be carefully considered. These filters, in fact, are not normally accounted for in the control algorithm, which refers to an "ideal" load model, where only inverter inductances L_F are taken into account, as shown in Fig. 3. This is what can be called a *model mismatch*. Due to the presence of the input

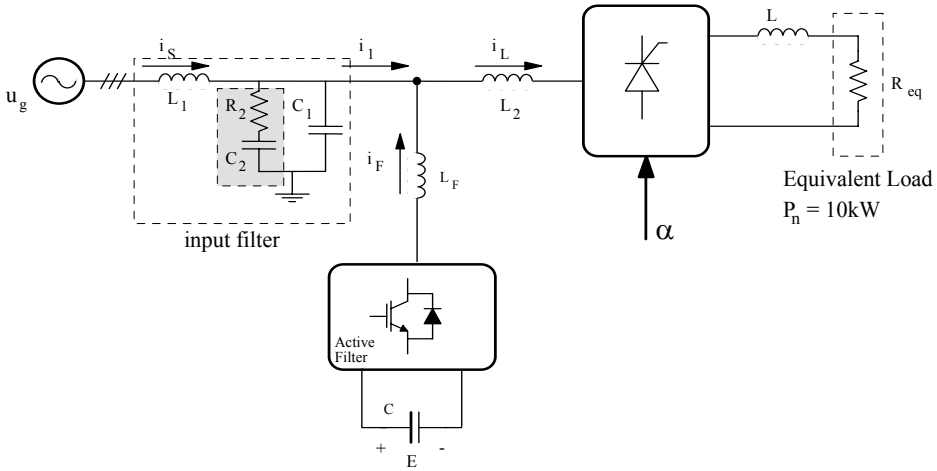

Fig. 1 - Basic scheme of the system with the parallel active filter

filters, the dynamic behaviour of the current loop changes and may even reach instability. Some issues concerning this problem are discussed in [5]. Anyway, similar problems arise also when there is a *parameter mismatch* between the modeled inverter inductance and the actual one [10]. In the following, we restrict our analysis only to this last issue. Therefore, in the analysis, the presence of the line impedance, of the input filters and of the load are neglected, as shown in Fig. 3.

Stability analysis is performed using the discrete-time state space equations of the remaining first order system, given by the actual inductances L_F. As a consequence, the discrete time system equations, developed in the α, β fixed reference frame, have the following expression:

$$i(k+1) = \frac{T_{sw}}{L_F}\left[u_{av}(k) - u_s(k)\right] + i(k), \qquad (1)$$

where $i(k)$ is the inverter current, $u_{av}(k)$ the average phase voltage, generated by the active filter, and $u_s(k)$ the supply voltage, all of them evaluated at the sampling instant kT_{sw}.

The control algorithm, which ensures a deadbeat response for the first order system based on the modeled inductance L_{Fm} is given by [6]-[10]:

$$u_{av}(k+1) = \frac{L_{Fm}}{T_{sw}}\left[i_{ref}(k) - i(k)\right] + 2\,u_s(k) - u_{av}(k), \qquad (2)$$

where the line voltage u_s is either measured or estimated [6]-[10]. The line voltage estimation can be obtained using the algorithm:

$$e_s(k-1) = u_{av}(k-1) + \frac{L_{Fm}}{T_{sw}}\left[i(k-1) - i(k)\right] \qquad (3)$$

and then substituting in (2) $u_s(k)$ with $e_s(k\text{-}1)$ [6]-[9].

The stability analysis of the closed loop system can be performed by applying the Z-transform to (1), (2) and possibly (3), by deriving the characteristic polynomial of the closed loop system, and by mapping the closed loop poles. If the magnitude of the closed loop poles is equal or greater that one, the resulting system is, of course, unstable.

Following this procedure, we found that, if the line voltage is measured, the poles of the closed loop system given by (1) and (2) are:

$$p_{1,2} = \pm\sqrt{-\Delta L_{\%}}\,, \qquad (4)$$

where $\Delta L_{\%} = L_{Fm}/L_F - 1$ is the relative error between the actual and the modeled inductance. Eq. (4) shows that system stability is ensured up to 100% error in the modeled inductor L_{Fm}, revealing a considerable robustness to parameter mismatches for this condition.

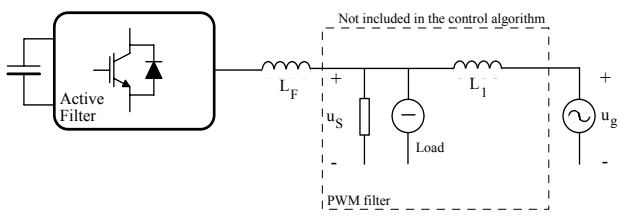

Fig. 3 - Simplified representation of Fig. 1.

Instead, if the line voltage is estimated using (3), we found that the characteristic polynomial of the closed loop system, determined by (1), (2) and (3), is

$$\lambda(z) = z^3 + 3\Delta L_{\%}\, z - 2\Delta L_{\%}\,. \qquad (5)$$

The closed loop poles, obtained solving $\lambda(z)=0$, show that only a 20% error is allowed before the system instability occurs. It is worth noting this result is independent of switching frequency since (5) is only function of the relative error $\Delta L_{\%}$.

A significant change in the system behaviour is obtained when the active filter current reference $i_{ref}(k)$ is a function of the line voltage estimation $e_s(k\text{-}1)$:

$$i_{ref}(k) = -G_{eq}\, e_s(k-1) + i_{load}(k)\,. \qquad (6)$$

Indeed, this provision, which avoids the use of the line voltage sensors, is peculiar of active filters and high-quality rectifiers, where the line current reference is related to the line voltage, and does not occur in drive applications. Using (6) into (2) and applying the Z-transform to (1), (2), (3), we derived that the closed loop poles are given by the following characteristic polynomial:

$$\lambda(z) = z^3 + \Delta L_{\%}\left(3 - K\right)z - \Delta L_{\%}(2 - K) = 0 \qquad (7)$$

where $K = G_{eqpu}/2\,m\,\Delta i_{max\%}$, and G_{eqpu} is the per-unit equivalent conductance of the compensated load, directly related to the active power absorbed by the load, m is the maximum inverter modulation index ($m = 2\hat{U}_s/E$), and $\Delta i_{max\%}$ is the maximum relative ripple of the inverter currents. Eq. (7) shows that the closed loop poles are strongly dependent on the conductance G_{eqpu} and thus on the operating condition of the load. When G_{eqpu} is null, (7) reduces to (5) and the 20% margin on the inductance error still applies. Instead when G_{eqpu} is greater than zero, the stability limits change and depend also on the system parameters. Assuming that the maximum modulation index is 0.9 and $\Delta i_{max\%}$ is 10%, we found that the use of (6) improves the stability limit up to a 40% margin on the inductance error when G_{eqpu} is at its maximum value, which is, of course, unity. Fig. 4 shows the maximum absolute value of the closed loop poles for the aforementioned conditions as a function of the relative error $\Delta L_{\%}$. Trace (a) refers to G_{eqpu} equal to zero and trace (b) refers to G_{eqpu} equal to one. Note that the system robustness is increased in the last condition since the maximum error $\Delta L_{\%}$, which is allowed before instability occurs, moves from 20% to 40%. Indeed, this result is not general and strongly depends on the system parameters (dc link voltage, supply voltage, inductance L_F, switching frequency). Moreover, it is worth noting that for applications where the power converters are injecting active power into the line, which correspond to negative values for G_{eqpu}, the maximum allowed error $\Delta L_{\%}$ is drastically reduced.

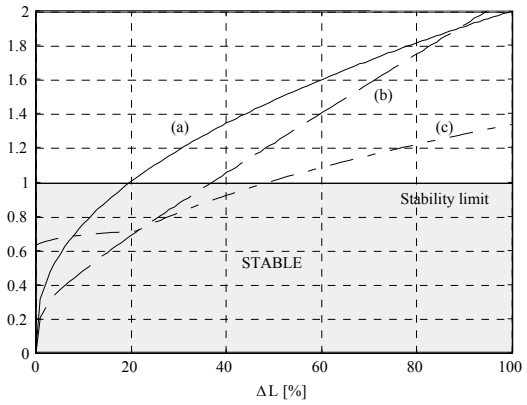

Fig. 4 - Absolute value of the maximum closed loop plant eigenvalue as a function of the relative estimation error on L. Solid line (a): line voltage conventional estimation; dotted line (b): reference calculation based on voltage estimation; dash-dotted line (c): proposed estimation technique.

In order to improve system stability a modified algorithm for the estimation of the line voltage $u_S(k)$ is here proposed. This modification is based on the fact that the aforementioned instabilities occur at half the switching frequency, which is, of course, much higher than the supply frequency, mainly because of the interaction between the estimation algorithm (3) and the control law (2). Therefore, it is possible to decouple the aforementioned interaction using a filter on the estimation voltage $e_s(k)$ which provides attenuation at high frequency and, at the same time, maintains the same low frequency content.

Since the line voltage $u_s(t)$ can be considered almost sinusoidal at a fixed frequency, a proper choice for the aforementioned filter is a pass-band filter centred at the supply frequency. This solution minimises the phase-shift at the supply frequency compared to low pass-filter solutions.

The improvement given by this provision is shown by the trace (c) of Fig. 4, obtained using $G_{eqpu}=0$ (worst-case condition) and a second-order band-pass filter with two null zeroes and a resonant pole couple with a magnitude of 0.7, located at the line frequency. We can see that with this provision the maximum relative error $\Delta L_{\%}$ moves from 20% (trace a) to 50% (trace c). A much greater improvement can be achieved by increasing the magnitude of the band-pass filter poles, at the expense of a slower transient response and of an increased sensitivity to supply frequency variations.

V. Analysis of the Active Filter Performance

This section of the paper discusses the quality of the compensation achievable by a dead-beat controlled active filter. Fig. 5a and 5b show the results of some simulations of the system depicted in Fig. 1, giving an indication of the achievable performance, when no significant passive filters (L_1=0, L_2=0.06pu) are used and the thyristor firing angle α is set to 75. Although the active filter is able to replicate its reference with a two modulation period delay (100μs), the current error exhibits a significant harmonic content. To further illustrate this, in Fig. 5c the line current spectrum is compared with the IEC 1000-3-2 standard requirements, which apply to the type of load here considered. As can be seen, the standard limitations are not met by the compensated load, especially for the high order harmonics. Thus, unless passive filter L_2 is extremely large, the use of an active filter alone, even if properly designed, is not enough to meet the standard requirements. Adding the input filter constituted of capacitor C_1 and inductance L_1, it is possible to achieve the required filtering action in the high frequency range and the standard limitations can be complied. Different problems can anyway arise concerning the stability of the current control; these compel to slightly oversize the passive filters, as it is discussed in [5], in order to maintain a suitable stability margin.

The simulation results have been verified by means of experimental tests on a laboratory prototype of an active filter operating in the conditions represented in Fig. 1. The ratings of the laboratory prototype are given in Table I. An

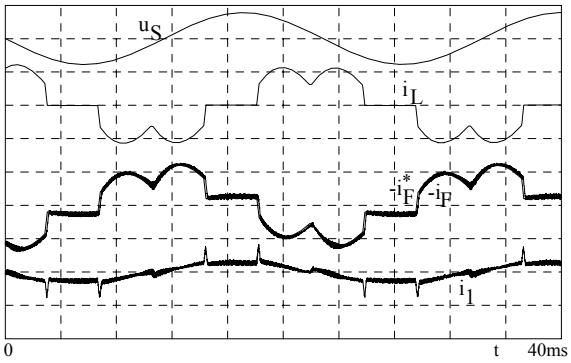

Fig. 5a - Simulated active filter behavior with L_1=0 and L_2=0.06pu: u_S(400V/div), i_L, i_1, i_F, i^*_F (20A/div)

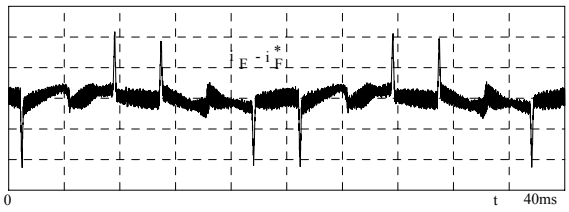

Fig. 5b -Residual line current with L_1=0 and L_2=0.06pu: (5A/div)

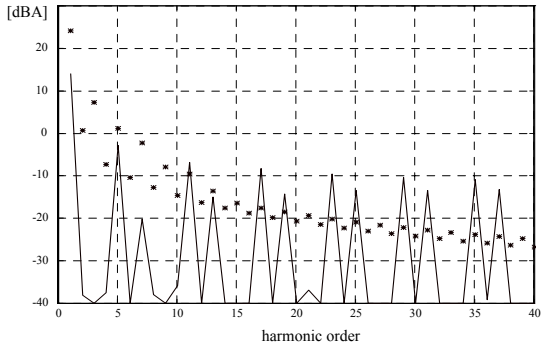

Fig. 5c - Spectrum of line current i_1 with L_1=0 and L_2=0.06pu - Symbols '*' represent IEC 1000-3-2 harmonic limits for class A equipment

accurate tuning of the control parameters has been performed to avoid the occurrence of the described instabilities. A brief description of the implemented system is given in the following.

A. Control Implementation

The dead-beat control strategy which was previously described, has been practically implemented by means of a floating point digital signal processor (ADSP21020). This DSP unit represents a powerful tool for digital controls implementations due to the fast arithmetic unit (40ns cycle) and its floating point architecture (32/40 bits). The interface between the processor and the power converter has been implemented exploiting the ADMC200 motion control board which includes all the necessary facilities for implementing a current control loop in a three phase voltage source inverter, from the PWM modulator to the A\D converter. All the details concerning the practical implementation of the digital control can be found in [5].

TABLE I
PROTOTYPE RATINGS

Line Voltage (RMS)	220 V
Bridge Output Power	10 kW
DC Link Voltage	750 V
Active Filter Inductance	1.2 mH
Bridge inductance	2.6 mH
Switching Frequency	20 kHz

B. Experimental Results

The first considered operating condition is characterised by a 65° ÷ 75° thyristor bridge firing angle, with L_1=0 and L_2=2.6mH. Fig. 6a shows the thyristor bridge (i_L) and active filter currents ($-i_F$). Fig. 6b instead shows the thyristor bridge (i_L) and the line compensated currents (i_S). It is possible to see that the main effect of the calculation delay of the dead-beat controller is the presence of compensation errors corresponding to any bridge commutation. Due to the steep current slope, the quality of the compensation is low. This is further confirmed by the line current harmonic content measurement, which is clearly outside the limitations imposed by the standards, as shown by Fig. 7. Fig. 8 instead, shows a good agreement between the effective and the estimated line voltage indicating a good tuning of the controller's parameters. The simulation results regarding the performance of the active filter are therefore confirmed by these tests. It is possible to conclude that, no matter the controller speed, which in this case is pretty high, the dead-beat current control may encounter some difficulties in achieving an acceptable compensation quality in an active filter application. To improve this quality the combination of the active filter with suitable passive filters is mandatory. As a consequence, to make the meeting of the IEC standards possible, a passive filter has been inserted between the line and the active filter (L_1=2.4mH, C_1=23μF, L_2=2.6mH). Then the experimental tests have been repeated in similar operating conditions of the thyristor rectifier load as compared to the previous situation. Figs. 9 to 11, describe the behaviour of the modified compensation system with a 65° ÷ 75° firing angle. As in can be seen in Fig. 10, the line current spectrum is now within the standard limits.

VI. CONCLUSIONS

The harmonic and reactive power compensation for a thyristor bridge rectifier is shown to be a quite difficult task for a digitally controlled parallel active filter. The dead-beat control strategy, in fact, being affected by calculation delays, turns out to be not very adequate to the task, even if control refinements and a considerably high switching and sampling frequency are adopted. The main problem is shown to be the residual high frequency harmonic content of the line current, which is difficult to keep within the very demanding standard limitations. The addition of passive filters to reduce this harmonic content is therefore necessary. This result is proved both by simulations and by experimental tests. Another important aspect of the digital dead-beat current control application to active filters is the sensitiveness to parameter mismatches between the load model and the actual converter load. The paper proposed an accurate modeling of the power converter and its load, allowing to perform the system's eigenvalue analysis and to evaluate the stability margins for different possible implementations of the control algorithm. The estimation of the line voltage is shown to represent the major responsible in the control's sensitiveness to parameter mismatches calling for alternative solutions, one of which is also discussed.

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