# A 400 Hz, 100 kVA, Digitally Controlled UPS for Airport Installations

G. L. Basile*, S. Buso**, S. Fasolo**, P. Tenti**, P. Tomasin***

*OCEM S.p.A.
Via 2 Agosto 1980 n.11 40016 S.Giorgio di Piano (BO) - ITALY
Phone: +39.051.665.0169 Fax: +39.051.665.0099 e-mail: ocem@ocem.com

**Department of Electronics and Informatics - University of Padova
Via Gradenigo 6/a - 35131 Padova - ITALY
Phone:+39.049.827.7503/7517 - Fax:+39.049.827.7699 - e-mail: simone@dei.unipd.it

***CREIVen Consorzio di Ricerca in Elettronica Industriale Veneto
Corso Spagna 12 - 35020 Padova - ITALY
Phone: +39.049.806.1212 - Fax: +39.049.806.1230 - e-mail: ricerca.creiven@iperv.it

*Abstract* - **The paper describes analysis, design and prototyping in reduced scale of a digitally controlled inverter for uninterruptible power supply (UPS) applications. The converter is rated for 100 kVA nominal power and 400 Hz, three-phase, 220 V sinusoidal output voltage. The final equipment is meant to be installed in airport docks and used as the aircraft's electrical power supply during refuelling and loading operations. It will be manufactured with different power ratings ranging from 30 to 300 kVA.**

**The power converter and digital control circuits are devised to provide rated voltage and frequency with a fairly low output impedance, so as to keep the voltage total harmonic distortion (THD) small even in the presence of highly distorting loads. Simulation results for the rated converter and experimental results from a scaled (5 kVA) prototype are given, which illustrate the expected converter performance.**

## I. INTRODUCTION

Uninterruptible power supplies (UPS's) are nowadays widely adopted for the protection of sensitive loads, like PC's or medical equipment, against line failures or other AC mains' perturbations such as voltage sags or swells. A large number of products, with different topologies and very different power handling capabilities, are available on the market, making the UPS a quite mature product. Accordingly, the past and recent research activity related to this particular type of voltage source inverter application has been very wide and detailed, extensively exploring both topological ([1], [2], [3]) and control related issues ([4], [5]).

This paper describes the analysis and design of the inverter unit of a new family of commercial UPS's that is specifically aimed at airport installations. This market niche is characterised by a very challenging demand for high static and dynamic performance, calling for careful selection and design of both the power converter stage and the control system. The desired features of the final UPS unit are: 100 kVA rated power, three-phase, 400 Hz - 220 V regulated output voltage, output voltage THD lower than 3% (with linear load). In addition, direct parallel connection [6] of up to three units is required.

In the first part of the paper, complete design specifications are presented and the problem of developing a cost-effective and reliable power stage, compliant with all requirements, is approached. In the second part, control issues are considered and the digital control platform used for the implementation is described. Finally, results of full scale system simulation and measurements on a reduced scale prototype (5 kVA) are presented.

## II. SYSTEM DESCRIPTION

The basic scheme of the UPS system is shown in Fig. 1, while the main design specifications are reported in Table I. As can be seen, the considered topology is that of a classical no-break UPS, where the load is continuously fed by the PWM-controlled DC/AC converter. This is due to the

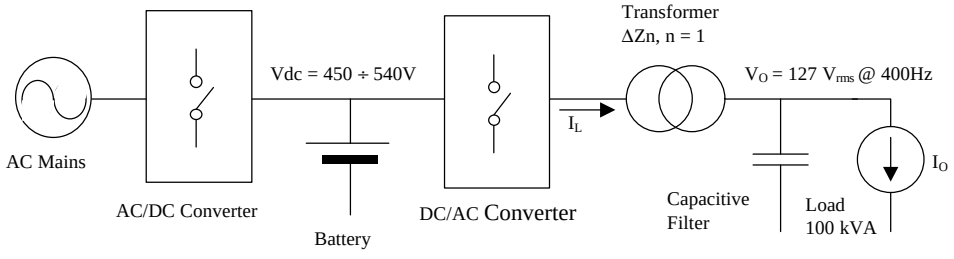



Fig. 1 – Simplified schematic of the UPS system

0-7803-6404-X/00/$10.00 (C) 2000

necessity of generating a 400 Hz voltage supply for the aircraft. The batteries are kept charged by a conventional thyristor controlled rectifier. The specifications show a reduced DC link voltage variation range, thanks to the high quality of the batteries employed in these special

TABLE I
THREE-PHASE CONVERTER SPECIFICATIONS

| | | | |
|---|---|---|---|
| DC link voltage | $V_{DC}$ | 450 ÷ 550 | [V] |
| Nominal output power | $P_o$ | 100 | [kVA] |
| Output frequency | $f_o$ | 400 | [Hz] |
| Output voltage (line to line) | $V_{oRMS}$ | 220 | [V] |
| Voltage harmonic distortion* | $THD_{Vo}$ | 3 | [%] |

* with linear load.

applications. It is standard practice, and therefore an implicit design specification, to provide the electrical isolation of the load by means of a transformer. The transformer, which is a critical and expensive component of this design, has several peculiarities. In the first place, it is designed for a 400 Hz operating frequency and is consequently much smaller and lighter than a standard line-frequency transformer of the same power rating. As far as the winding arrangement is concerned, a four-wire secondary side is the most commonly used in this kind of products. A ΔZn structure is normally preferred to the more usual ΔYn because the zigzag arrangement at the secondary side offers a relatively small impedance to the possible zero sequence or *homopolar* component of the load current. Being a special component, the transformer leakage and magnetising inductance can be used as degrees of freedom in the system design and selected, within feasible ranges, as it is more convenient. As usual, the converter output voltage is cleaned from the high frequency harmonic content generated by the PWM process by means of suitable filter capacitors. The output impedance of the converter is largely determined by the size of these filters, whose selection is a key point in the converter design. A reduced ESR is required to avoid voltage steps in the presence of steep load variations.

Finally, it is worth noting that a large variety of loads is typically connected to this type of power supplies. A large percentage of the total applied load, which can get as high as 50% in the worst case, is commonly made up of highly distorting loads (typically diode rectifiers with capacitive filters). It is also common for the load to be strongly unbalanced, lots of single phase loads being connected between two output phases (no homopolar currents are generated in this case), or between phase and neutral, with consequent generation of homopolar current components.

## III. POWER CONVERTER DESIGN

The power converter design begins with the selection of the desired DC link voltage. This must be consistent with the state-of-the-art batteries available for this power level and this particular application. Based on the manufacturer experience, a nominal DC link voltage of 500 V is chosen, which may exhibit a ±10% variation, depending on the battery charge state. Given the required output power level, the inverter switching frequency is selected to be 8 kHz, to be compatible with commercial 1.2 kV - 1.2 kA, press-pack IGBT power modules, which will be used as converter switches. In order to limit the thermal stress on the active devices, the use of flat-top PWM has been considered particularly useful and has been implemented in the modulation routine of the control software.

As far as the transformer is concerned, initially it is assumed that each of its phases can be represented by a single equivalent series inductor L, which will be in practice closely related to the leakage inductance. The effect of the magnetising inductance $L_\mu$ will be considered successively. The value of L is selected as a trade-off between phase current ripple and inductance voltage drop at the fundamental output frequency. Eq. (1) gives the peak to peak inverter current ripple $\Delta i_{Lpprel}$, normalised to the rated peak phase current $i_{Lp}$:

$$\Delta i_{Lpprel} = \frac{\Delta i_{Lpp}}{i_{Lp}} = \frac{R_{base}}{4 \cdot f_{sw} \cdot L}, \qquad (1)$$

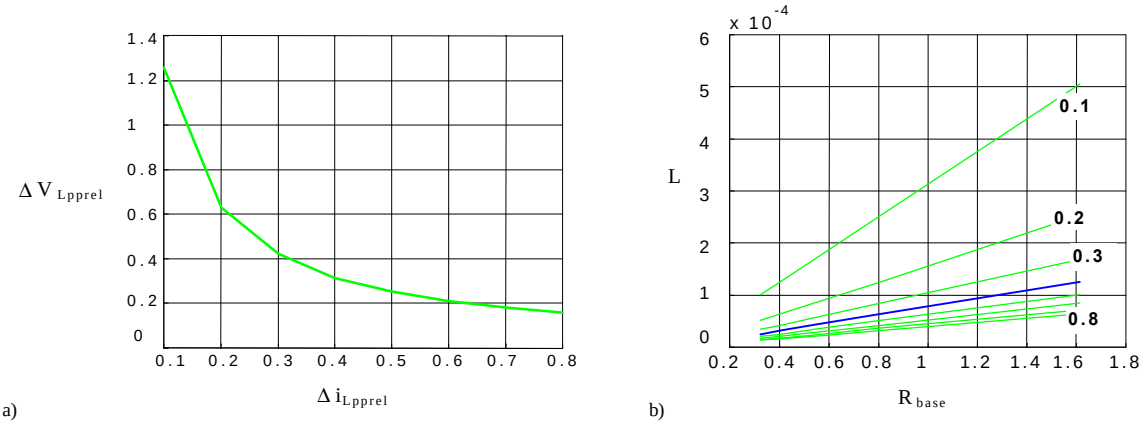



Fig. 2 – a) Relative inductance voltage drop at fundamental frequency as a function of the relative peak to peak current ripple.
b) Inductance value as a function of $R_{base}$ for different relative peak to peak current ripple values.

where $R_{base} = V_{DC}/i_{Lp}$ and $f_{sw}$ is the switching frequency.

Eq. (2) instead gives the peak to peak voltage drop $\Delta V_{Lpprel}$ on the phase inductance at the fundamental output frequency $f_o$, normalised to the DC link voltage:

$$\Delta V_{Lpprel} = \frac{\Delta V_{Lpp}}{V_{DC}} = \frac{4 \cdot \pi \cdot f_o \cdot L}{R_{base}} \qquad (2)$$

The combination of (1) and (2) gives the diagram of Fig. 2a, while the diagram of Fig. 2b is directly derived from (1). For the given DC link voltage and load power, a reasonable choice is to keep the inductance normalised voltage drop below 30%, which implies a relative current ripple greater than 40%. It is worth noting that this approximated procedure does not take into account the phase interference typical of three-phase converters with insulated neutral, which will significantly reduce the actual current ripple. In practice, the relative current ripple will be smaller than 20%. Anyway, from Fig. 2b it is possible to see what value of L keeps the relative current ripple below 40%, as the parameter $R_{base}$ varies. This parameter depends on the size of the capacitive output filter and of the magnetising inductance and can be defined only after these other elements have been designed. As a consequence, an iterative procedure must be followed. In our design, a value of 120 µH was finally selected.

As far as the output filter capacitor is concerned, Table I shows that the output voltage harmonic distortion must be less than 3% in the presence of a linear load. This specification, together with the chosen switching frequency and inductance L, directly determines the minimum output capacitor necessary to filter the current ripple, which, in this case, turns out to be about 400µF.

The dependence of the output voltage THD on the capacitor value, in the presence of non-linear loads, was deeply analysed. This type of analysis cannot be performed without taking into account the presence of the control system, which, in general, reduces the converter's output

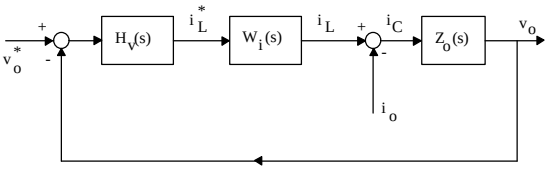
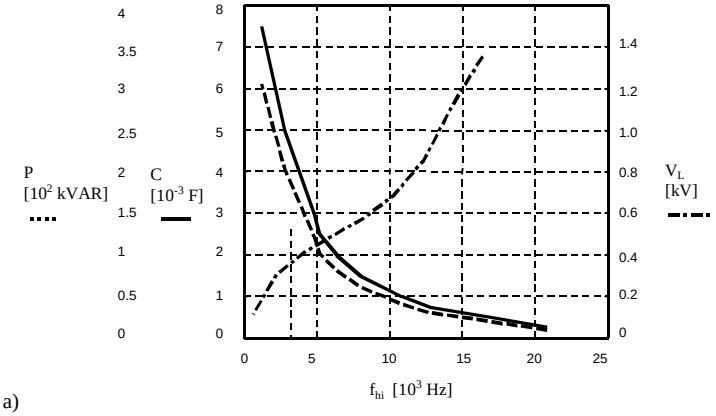


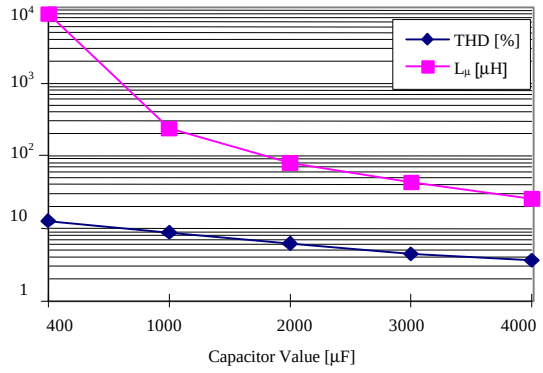

Fig. 3 – Simplified control scheme. $H_V(s)$ is the voltage controller, which generates the current loop reference $i_L^*$. $W_i(s)$ is the transfer function of the closed loop current control, while $Z_o(s)$ is the intrinsic output impedance, due to the output filter capacitor.

impedance and consequently improves the voltage THD induced by distorting loads. In particular, as it will be explained with greater detail in the following section, a current control loop and a voltage control loop have been implemented, basically as shown in Fig. 3. Even if, in principle, both the control loops contribute to the output impedance reduction, in the following considerations the presence of the voltage control loop will always be neglected. Given the bandwidth limitation that characterise it, its effect on the reduction of the converter output impedance is, in fact, negligible. To practically perform the THD analysis, a typical distorting load current pattern, i.e. that of a diode bridge rectifier with capacitive filter, absorbing 50% of the nominal output power with a crest factor not lower than 2, is assumed. Then, the induced harmonic distortion as a function of the capacitor value and current loop bandwidth is analytically computed and verified by simulations.

As it can be expected, for a given current loop bandwidth, increasing the output capacitor reduces the residual harmonic distortion. On the other hand, for a given capacitor value, increasing the current loop bandwidth helps to reduce the voltage distortion. However, both these actions affect the power converter design. In fact, increasing the filter capacitor causes an increase of the VA rating of the converter (i.e. of the peak phase current $i_{Lp}$), unless special provisions are taken, such as using the transformer magnetising inductance to partially compensate for the capacitive reactive power. On the other hand, increasing the




a)




b)

Fig. 4 a) Relationship between current loop bandwidth ($f_{hi}$) and filter capacitor value (C) needed to keep voltage distortion below 3% with the assumed distorting load. On the same diagram: reactive power (per phase) absorbed by the capacitive filter and instantaneous voltage drop across the output inductance for a 1 kA load peak current (in absence of converter saturation).

b) Magnetizing inductance value (needed to compensate reactive power absorbed by the capacitive filter) and expected voltage THD as a function of filter capacitor value, with the same distorting load considered in a) and current loop bandwidth of about 3 kHz.

current loop bandwidth calls for an increase of the DC link voltage, in order to avoid converter saturation during transients and so to take full advantage of the faster dynamic response.

Fig. 4 shows the design diagrams resulting from the above described analysis. In particular, Fig. 4a shows the required capacitor value (per phase), which is necessary to keep the THD below 3% with the specified distorting load, as a function of the current loop bandwidth $f_{hi}$. Unless unrealistic loop bandwidths are assumed, the capacitive filter must be pretty high, and so the associated reactive power. The diagram also shows an estimation of the instantaneous voltage drop across the phase inductance, needed to sustain a given current loop bandwidth during transients, assuming the distorting current can be roughly approximated by a 1 kA triangular pulse. This trace indicates that a current loop bandwidth in the range of 3 kHz is capable of causing power converter saturation in the presence of any load current steep transition. In fact, it implies an instantaneous voltage drop across the phase inductance in the range of the DC link voltage. Therefore, it is clear that a much bigger THD must be accepted, to limit the VA rating of the power converter. Fig. 4b shows the relationship between output capacitor and residual voltage THD, when a feasible bandwidth (≈ 3 kHz) is assumed for the current loop. On the same diagram, the magnetising inductance needed to compensate the capacitive reactive power is also shown. Based on these diagrams, a selection was made to use 1000μF capacitive output filters and partial reactive compensation by means of the transformer magnetising inductance $L_\mu$ (240 μH). Note that this small value is not typical for a transformer: this is not a problem anyway, since the fundamental frequency, by itself, already requires a special transformer design. With this design, the expected voltage THD will be about 10% when a typical distorting load is applied and below 3% with linear load.

## IV. Control Strategy and Implementation

The structure of the control system is shown in Fig. 5. As can be seen, the system is provided with an internal current loop controlled by two external voltage loops. The inner voltage loop controls the voltage fundamental harmonic component and operates on a d-q rotating reference frame; the outer loop controls the voltage RMS value. The presence of the current loop is required to guarantee the effective control and limitation of the converter output current and to simplify the control of parallel connected units. The current control bandwidth is inherently limited by the delays associated to the modulation and sampling processes. To partially overcome this limitation, the PWM modulator of the control system, which is a FPGA-based custom circuit, was designed to allow the asymmetrical PWM mode of operation, which reduces the delay to a half of the modulation period. With this technique, the sampling and control frequency are set to twice the modulation frequency and the PWM modulator is updated twice in each modulation period, the first time to set the switches' turn-on instant and the second to set the turn-off. This allows to increase the current loop bandwidth to values in the range of 3 kHz. The structure of the adopted current controller is truly simple consisting of a pure proportional gain. The output of the current controller is processed according to the space vector modulation (SVM) approach, as usual in the digital control of three-phase converters. Then the FPGA based modulator is programmed to generate the required voltage vector.

As far as the voltage loop is concerned, it is very difficult to achieve a satisfactory output voltage regulation with a conventional voltage control (e.g. PI regulator), mainly because of the relatively high output voltage fundamental frequency, which hardly falls within the bandwidth of a feasible voltage regulator. To overcome this problem and achieve a good regulation accuracy, at least in steady state and with linear load, a d-q rotating-frame controller is considered. This allows to get a very precise regulation of the fundamental component of the output voltage, at the expense of the regulation bandwidth, which is unavoidably limited. Therefore, in the presence of non-linear loads, the achievement of a small voltage distortion mainly depends on the converter intrinsic output impedance, which has to be

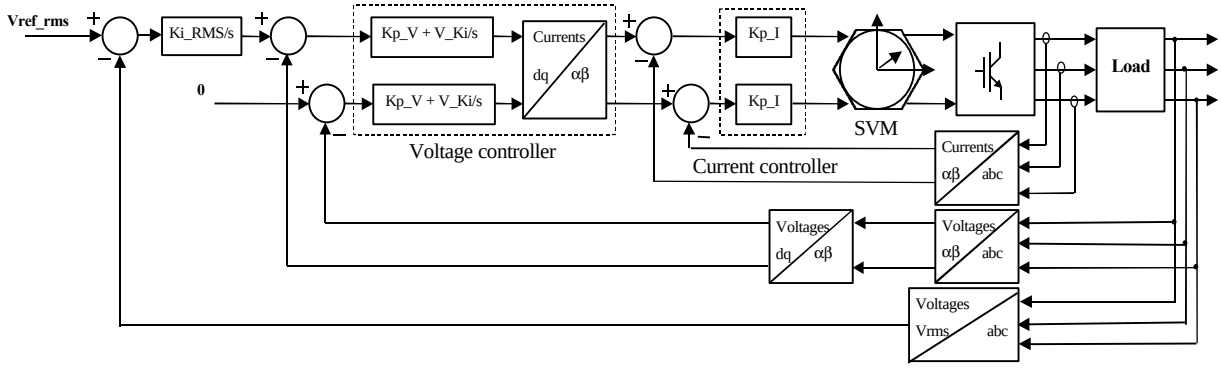



Fig. 5 – Detailed structure of the control system

designed accordingly. It is important to notice that, with a simple modification of the control loop, which introduces also an inverse sequence d, q transformation on the output voltage, it is also possible to effectively compensate for some of the effects of unbalanced loads. When an unbalanced load is connected to the power converter, the output voltage normally becomes unbalanced itself, due to unsymmetrical voltage drops on the transformer output impedance. In this case, the output voltage vector $\dot{V}_O$ can be seen as the superposition of direct sequence component $\dot{V}_{Od}$, an inverse sequence component $\dot{V}_{Oi}$ and a zero sequence component $\dot{V}_{Oo}$, and decomposed accordingly:

$$\dot{V}_{Od} = \frac{\dot{V}_{Or} + \alpha\dot{V}_{Os} + \alpha^2\dot{V}_{Ot}}{3}, \qquad \alpha = e^{j2\pi/3};$$
$$\dot{V}_{Oi} = \frac{\dot{V}_{Or} + \alpha^2\dot{V}_{Os} + \alpha\dot{V}_{Ot}}{3}; \qquad (3)$$
$$\dot{V}_{Oo} = \frac{\dot{V}_{Or} + \dot{V}_{Os} + \dot{V}_{Ot}}{3};$$

where $\dot{V}_{Os}, \dot{V}_{Or}, \dot{V}_{Ot}$ are the output voltage phase vectors.

The usual rotating-frame controller implementation shown by Fig. 5 regulates only the direct component $\dot{V}_{Od}$, the inverse component being seen as an oscillation at twice the fundamental frequency, well outside the bandwidth of the control loop. On the other hand, if an inverse d-q transformation is added, which simply considers the reverse phase sequence, (1, $\alpha$, $\alpha^2$) instead of (1, $\alpha^2$, $\alpha$), and therefore maps the inverse sequence components into constant voltages, also the inverse sequence component $V_{Oi}$ can be controlled and, in principle, fully compensated by a proper regulator, which operates in parallel to the direct sequence one. It is important to notice that the same PI regulator used for direct sequence controller can be used also in the inverse sequence controller, which makes the implementation relatively simple. This feature has been included in our final implementation and has implied only a slight increase in the total computation time.

There is clearly nothing to do for the compensation of possible homopolar current components and of related voltage unbalances because of the physical limitations of the converter structure which, having only three wires on the primary side, cannot generate currents whose sum is not zero. Anyway, the transformer structure ($\Delta$Zn) allows to achieve at least a partial compensation of also this type of unbalances, thanks to the low impedance shown to the homopolar currents.

Finally, it is worth noting that an external rms voltage control loop is implemented to keep the rms output voltage under control in the presence of significant harmonic distortion, which cannot be compensated by the internal voltage loop.

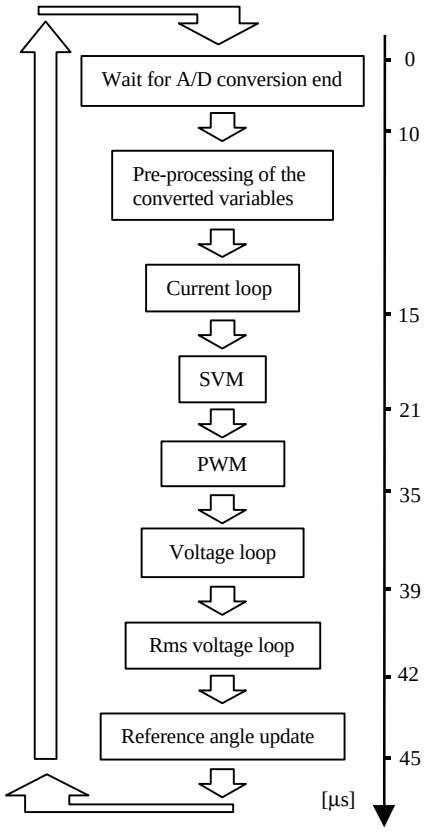
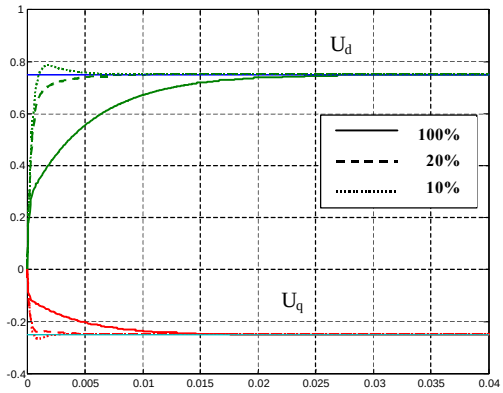



Fig. 6 – Flow chart of the control program

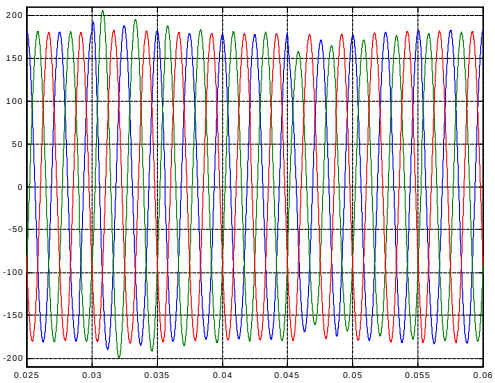
As far as the control implementation is concerned, all the control loops are implemented by means of a TMS320C31 floating point DSP with a 60 MHz clock. Fig. 6 shows a flow chart of the control program indicating also the measured duration of the different control routines. As can be seen, the PWM process is controlled by a relatively time consuming routine ($\approx 14\ \mu s$); this is because the FPGA implementing the modulator is programmed by the DSP through a synchronous serial interface, which determines a large part of the measured delay. In the future implementation this limitation will be removed by a new modulator, which will be seen by the DSP as a memory-mapped peripheral. However, it is worth noting that, thanks to the computational power of the adopted DSP unit, it was possible to completely write the control program in C language, without the need for particular code optimisation. Actually, given the measured computation time and being the control algorithm executed twice per modulation period, it would be possible to increase the switching frequency up to 10 kHz, without modifications to the control program.

## V. Simulation Results

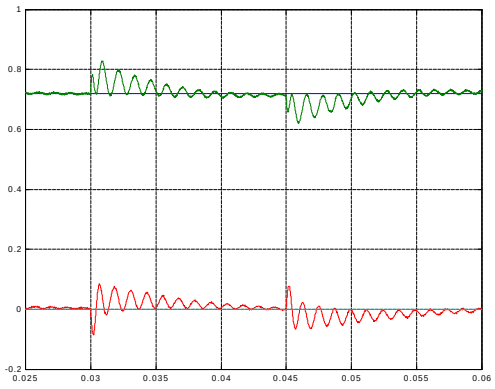
The designed system has been simulated to verify the quality of the design. The simulations do not include the effects of the particular transformer magnetic structure, which has not been modelled. Anyway, this is only effective in particular operating conditions, e. g. when the load is unbalanced and homopolar current components are expected.




a)

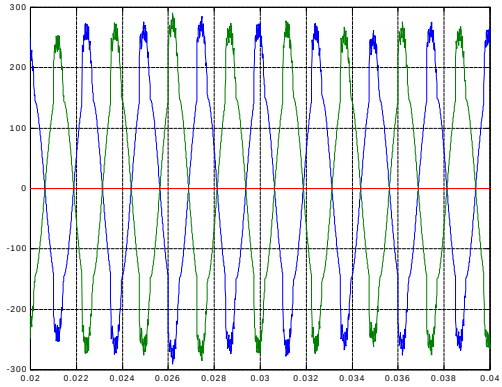


b)

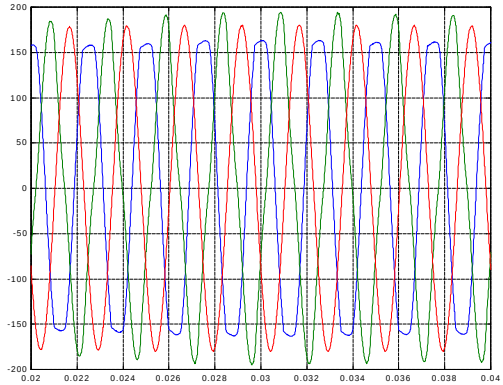


c)

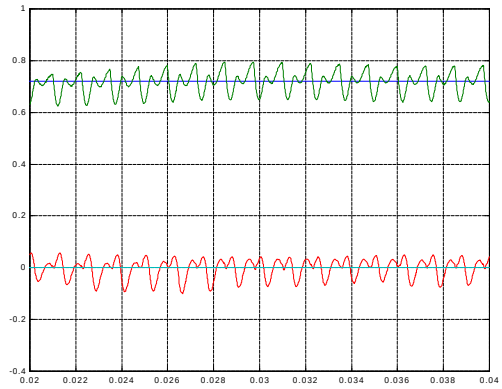
Fig. 7 – a) Voltage loop step response with different loads
b) Load variations (100%-40%-100%) with unbalanced load.
c) d, q voltage regulation in the same conditions of case b)



a)



b)



c)

Fig. 8 – a) Phase currents with non-linear unbalanced load;
b) Phase voltages (abc reference frame);
c) d, q voltage regulation in the same conditions of case b).

These aspects will be investigated in the future prototype developments. The control system performance, instead, has been extensively evaluated.

Fig. 7 shows some of the obtained results. In particular, Fig. 7a shows the voltage controller step response with different loads. As can be seen, due to a suitable decoupling action on the axes dynamic equations, the response is first

order and acceptably damped within a considerable load range. Fig. 7b shows the system behaviour in case of step load variations, when an unbalanced load is connected to the converter. More precisely, a single resistive load is connected between two converter phases, which drains a current equal to the nominal one. The load is then reduced to 40% and then increased again to the original level. It is possible to see that the correct voltage amplitude is practically recovered in three fundamental periods for all the phases, achieving a fairly good compensation of the unbalance. The dynamics of the voltage regulator can be better evaluated in Fig. 7c, where the direct d, q regulation is shown. As can be seen, the unbalance in the output voltages induced by the unbalanced load appears in the direct d, q reference frame as an oscillation at twice the fundamental frequency. The action of the inverse sequence regulator is then revealed by the progressive reduction of the oscillation amplitude.

The system behaviour in the presence of a non-linear and unbalanced load is shown by Fig. 8. As can be seen, the considered load is a single-phase rectifier with capacitive filter connected, in parallel with a linear load, between two phases, being the third not connected. Again, the power drawn from an active converter's phase is in the range of the nominal power. As can be seen, the control system is able to compensate the unbalance, but practically nothing can be done against the distortion, which is only limited by the output capacitors. As a consequence, the d, q regulation of the output voltage exhibits persistent oscillations, which are related to the residual high order harmonics of the output voltage.

TABLE II
CONVERTER PARAMETERS

| | |
|---|---|
| DC Link Voltage | 300 V |
| Phase Inductor | 1.8 mH |
| Magnetising Inductor | 5 mH |
| Output Capacitor | 60 μF |
| Switching Frequency | 10 kHz |
| Nominal Output Power | 5 kW |

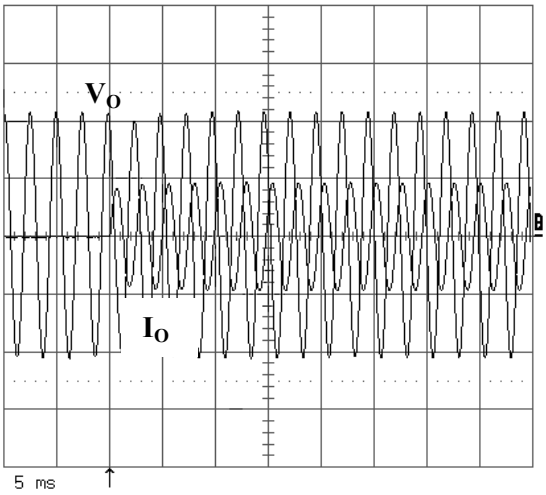
The results are anyway consistent with the design choices of Section II, since with the adopted capacitor size the voltage THD stays well below 10%.

## VI. EXPERIMENTAL MEASUREMENTS

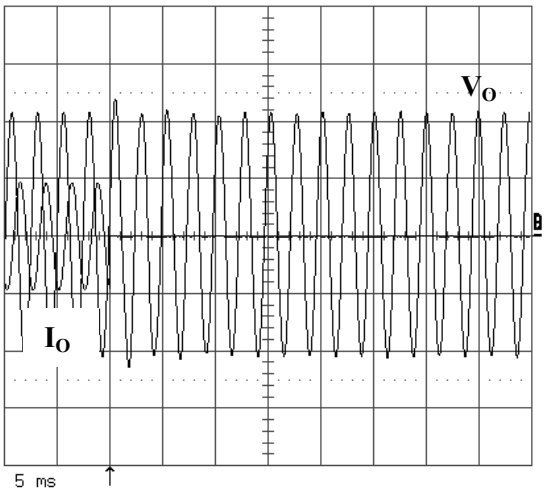
The control algorithm discussed so far has also been implemented and tested experimentally, on a low power three-phase voltage source inverter. The output filter has been synthesised by means of discrete inductors, since a reduced scale version of the transformer was not available at the moment. This gives to the output filter a dynamic behaviour similar to that of the final converter, so that the same previously discussed controller structure could be used. The laboratory converter's parameters are given in Table II.

Preliminary tests have been performed simply to demonstrate the feasibility of the control strategy: more experimental activity will be necessary when a prototype of the final converter will be available.

Fig. 9 shows the system's behaviour in the presence of step load variations. In particular Fig. 9a shows the step variation from no load to 50% of the nominal load, while Fig. 9b shows the opposite transition. The control system guarantees in both cases a practically complete recovery of the desired voltage waveform in four fundamental periods,




a)




b)

Fig. 9 – a) Step load variation from 0% to 50%;
b) Variation from 50% to 0%;
Output voltage $V_O$: 60 V/div.
Load current $I_O$:10 A/div).
Time base: 5 ms/div

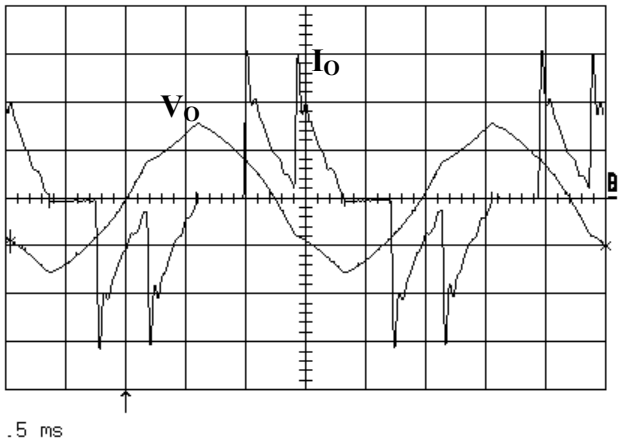



Fig. 10 – System's behavior with non-linear load. Output voltage $V_O$ (60V/div), distorting load current $I_O$ (5A/div).

which is in good agreement with the expected performance.

Fig. 10 refers to the application of a non-linear load to the converter. The applied load is a three-phase diode rectifier with capacitive filter. The control system is in this case capable of controlling the true rms voltage value to the desired set point. The residual harmonic distortion is within the limits imposed by the control bandwidth and output filter design.

## VII. CONCLUSIONS

The paper described the design of a new line of UPS systems, featuring power ratings ranging from 30 kVA to 300 kVA, 220 $V_{rms}$, 400 Hz regulated output voltage and low output impedance, so as to limit the voltage harmonic distortion even in the presence of highly distorting loads.

The design of a 100kVA-power converter with fully digital control was analysed detail. The power converter design was validated by means of computer simulations for the full-scale prototype, while the control system effectiveness was also evaluated by preliminary experimental tests on a laboratory scaled version.

## REFERENCES

[1] F.Kamran, T.Habetler, “A Novel on-line UPS with Universal Filtering Capabilities” IEEE PESC’95 Conf. Rec., 1995, pp. 500-506.

[2] K.Hirachi, M.Sakane, T.Matsui, A.Kojima, M.Nakaoka, “Cost-Effective Practical Developments of High-Performance and Multi-Functional UPS with New System Configurations and Their Specific Control Implementations”, IEEE PESC’95 Conf. Rec., 1995, pp. 480-485.

[3] D.M.Divan, “Inverter Topologies and Control Techniques for Sinusoidal output Power Supplies,” JE.EEAPEC ’91 Conf. Rec., 1991, pp. 81-S6.

[4] L.Malesani, L.Rossetto, G.Spiazzi, A.Zuccato: "An AC Power Supply with Sliding Mode control," IEEE IAS Conf. Proc., 1993, 1115-1121.

[5] N.M.Abdel-Rahimand J.E.Quaicoe, “Analysis and Design of a Multiple Feedback Loop Control Strategy for Single-Phase Voltage-Source UPS Inverter” IEEE Trans. on Power Electronics, vol. 11, no. 4, pp. 532-541, July 1996.

[6] J.F.Chen and C.L.Chu “Combination of Voltage-Controlled and Current-Controlled PWM Inverters for UPS Parallel Operation,” IEEE Trans. on Power Electronics, vol. 10, no. 5, Sept. 1995, pp. 547-558.