

A Line-Frequency-Commutated Rectifier Complying with IEC 1000-3-2 Standard

Simone Buso, *Member, IEEE*, and Giorgio Spiazzi, *Member, IEEE*

Abstract—Consumer and household appliances require low-cost ac/dc power supplies complying with EMC standards. The commonly employed passive solutions are bulky and do not provide output voltage stabilization. Active solutions, based on power-factor correctors with high-frequency switching, provide compactness and regulation capability, but are generally expensive due to the need for fast-recovery diodes and complex EMI filters. This paper presents a high-power-factor rectifier, based on a modified conventional rectifier with passive L - C filter, which improves both the harmonic content of the input current and the power factor, by means of a low-frequency-commutated switch and a small line-frequency transformer, and allows compliance with IEC 1000-3-2 standard with reduced overall inductive components' volume.

Index Terms—Electromagnetic interference, harmonic distortion, reactive power, rectifiers.

I. INTRODUCTION

LINE-CURRENT harmonic standards, like IEC-1000-3-2 [1], have led to a great effort in developing front-end ac-to-dc converters absorbing lightly distorted currents. High-frequency power-factor correctors (PFC's), which draw from the grid a current nearly proportional to the input voltage, have already been extensively analyzed in the literature. Their typical performance is very good, but, for some large-volume applications, like household appliances and personal computers, they imply an unacceptable increase in the cost and complexity of the conversion unit. These applications indeed require very inexpensive and reliable solutions; therefore, in many cases, passive filters are still used in conjunction with diode rectifiers. A classical diode-bridge rectifier and filter capacitor with a series filter inductor (L - C rectifier), can actually achieve compliance with the standards, but bulky and heavy reactive components are needed [2].

Different passive configurations are analyzed in [3], which are derived from the classical L - C filter by adding another capacitor inside the rectifier or even another diode [4]. The result is a substantial improvement in the harmonic content of the absorbed current and power factor. However, such solutions are effective for an input power up to 300 W, even taking into account the Class A limits of IEC 1000-3-2 [1]. Moreover, being completely passive, these solutions do not provide any kind of output voltage stabilization.

Manuscript received April 20, 1999; revised December 12, 1999. Abstract published on the Internet March 12, 2000. This paper was presented at the 1999 IEEE Applied Power Electronics Conference and Exposition, Dallas, TX, March 14–18.

The authors are with the Department of Electronics and Informatics, University of Padova, 35131 Padova, Italy.

Publisher Item Identifier S 0278-0046(00)04737-7.

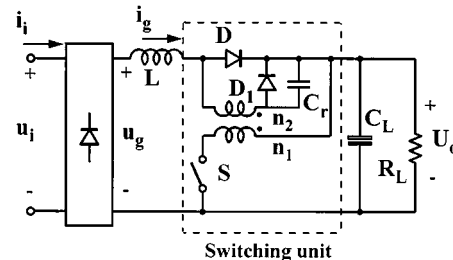


Fig. 1. Scheme of the low-frequency-commutated rectifier.

This paper discusses a high-power-factor rectifier, based on a modified conventional rectifier with passive L - C filter, which includes, as the main additional elements, a low-frequency-commutated switch (twice the line frequency), two diodes, and a small line-frequency transformer. This approach improves both the harmonic content of the line current and the power factor and, therefore, allows compliance with the standards with a much smaller inductive components' volume as compared to fully passive rectifiers. Moreover, the boost action achieved by the switch operation allows the proposed rectifier to compensate for the input inductor voltage drop and to regulate the rectified output voltage in a wide load range. Finally, the rectifier exhibits limited di/dt and dv/dt , which imply reduced high-frequency EMI generation, and very small switching losses, which allow for a quite high overall efficiency.

II. LINE-FREQUENCY-COMMUTATED RECTIFIER

The scheme of the proposed modified rectifier is shown in Fig. 1. The basic structure is that of the usual rectifier with an L - C filter, where an additional switching unit is inserted. Such unit consists of a low-frequency-commutated switch, two diodes, and a line-frequency transformer which is reset by the secondary-side capacitor C_r . All the elements of the switching unit, with the exception of diode D (which can be a slow-recovery diode), are rated for only a small fraction of the output power. The switch is turned on only twice per line period, thus allowing reduced di/dt , dv/dt , and losses.

The operation of the circuit depicted in Fig. 1, momentarily neglecting the transformer magnetizing current, can be explained as follows. The switch is turned on with a constant delay T_d after the zero crossing of the line voltage causing a fraction n_2/n_1 of the output voltage to appear in series with the inductor with the right polarity to cause the premature bridge diode turn-on (diode D is off in this interval). As a consequence, the inductor current starts to increase earlier with respect to the natural diode turn-on instant, as shown by Fig. 2. The duration of the switch on-time T_{ON} is controlled

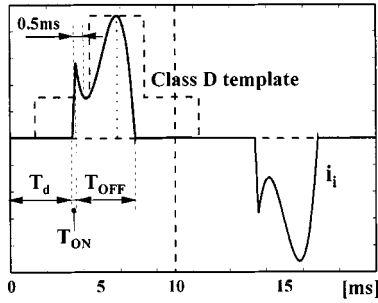


Fig. 2. Input current waveform (1 A/div) of low-frequency PFC and Class D template ($U_i = 230 \text{ V}_{\text{rms}}$, $P_o = 300 \text{ W}$, $T_d = 3.5 \text{ ms}$, and $T_{\text{on}} = 0.18 \text{ ms}$).

by an output voltage regulator and is limited to a maximum level to avoid the transformer saturation. Thus, a simple current-limiting protection of the switch is also inherently implemented. As the switch turns off, diode D starts to conduct and the filter inductor resonates with the output capacitor until the current zeros.

It is interesting to note that, for a unity transformer turns ratio, the converter behavior becomes identical to that of a boost rectifier [5], [6]. Thus, the improvement in the input current waveform as compared to the line-frequency-commutated boost comes from the possibility of choosing the inductor voltage during the switch on-time through a proper transformer turns ratio value. Reducing this voltage causes a reduction in the current slope with a consequent decrease of the high-frequency harmonic amplitudes.

In the practical implementation, reset circuitry must be provided to make sure the magnetizing current is forced to zero at the end of each period. This is achieved by capacitor C_r . To explain the reset process, let us refer to Fig. 3(a), which reports the transformer winding currents i_{pri} and i_{sec} and the voltage across the reset capacitor C_r . During the switch on-time, the output voltage is applied to the transformer primary winding and its magnetizing current i_μ increases linearly according to the relation

$$i_\mu(t) = \frac{U_o}{L_\mu} t \quad (1)$$

where L_μ is the primary magnetizing inductance. During the same interval, the secondary winding current i_{sec} coincides with the input current. Note that capacitor C_r can have a residual voltage at the beginning of the T_{ON} interval which depends on its value and on the transformer magnetizing inductance value. Consequently, the initial input current evolution is dominated by the resonance between the input inductor L and the reset capacitor C_r . The latter can or cannot be completely discharged before the end of the T_{ON} interval; in the former case, its voltage is clamped to zero by the presence of diode D_1 . When the switch turns off, i_μ transfers to the secondary winding and charges capacitor C_r flowing through diode D , which now conducts the sum of the input current and the magnetizing current reflected to the secondary side. Thus, a resonant oscillation between capacitor C_r and magnetizing inductance L_μ takes place. If the corresponding resonant frequency is sufficiently low, as it is assumed

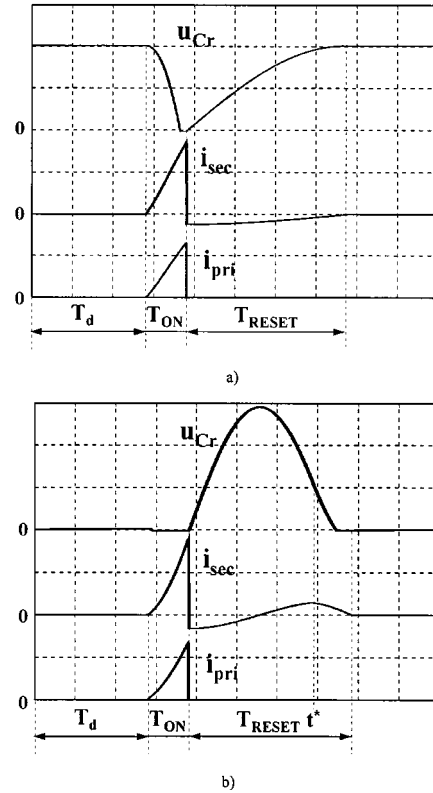


Fig. 3. Key waveforms during the transformer reset. (a) $T_r > 4T_{\text{off}}$. (b) $T_r < 4T_{\text{off}}$.

in Fig. 3(a), the input current goes to zero when i_μ is still greater than zero, thus minimizing the switch voltage stress. In fact, assuming C_r is completely discharged at the end of the T_{ON} interval, the magnetizing current and the capacitor voltage are given by (assuming the time origin at the switch turn off instant)

$$\begin{aligned} i_\mu(t) &= \hat{I}_\mu \cos(\omega_r t) \\ u_{C_r}(t) &= Z_r n \hat{I}_\mu \sin(\omega_r t) \end{aligned} \quad (2)$$

where $\hat{I}_\mu = (U_o/L_\mu)T_{\text{ON}}$, $\omega_r = (n/\sqrt{L_\mu C_r})$, and $Z_r = (1/n)\sqrt{(L_\mu/C_r)}$. Thus, the highest C_r value should be chosen compatible with the transformer reset, and this goal is achieved when the resonance period is chosen to be four times the minimum available reset time, i.e.,

$$T_r = 4 \left(\frac{T_g}{2} - T_{\text{ON max}} \right) \quad T_r = \frac{2\pi}{\omega_r} \quad (3)$$

where T_g is the line period. In this way, the switch voltage stress is minimized and is given by

$$\hat{U}_S = U_o \left(1 + \pi \frac{T_{\text{ON max}}}{T_g - 2T_{\text{ON max}}} \right) \quad (4)$$

as can be verified by summing $u_{C_r}(T_g/2 - T_{\text{ON max}})$ and U_o , using (3) to eliminate ω_r .

This result holds on the hypothesis that the switch on-time is long enough to completely discharge C_r during T_{ON} , as shown in Fig. 3(a). If this is not the case, the voltage across C_r stabilizes around an average value which guarantees the transformer reset.

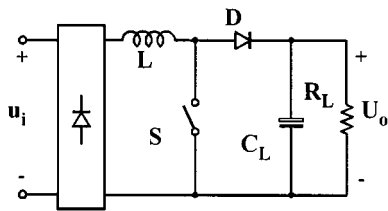


Fig. 4. Boost rectifier. The switch is operated at twice the line frequency.

At the limit of a constant voltage across it, the switch voltage stress becomes

$$\hat{U}_S = U_o \left(1 + 2 \frac{T_{ON \max}}{T_g - 2T_{ON \max}} \right) \quad (5)$$

which is obtained by imposing the magnetizing current reset in the minimum available switch off-time with $u_{Cr}(t) = U_{Cr}$, i.e., equating $U_{Cr} \cdot (T_g/2 - T_{ON \max})$ and $U_o \cdot T_{ON \max}$.

If the latter condition holds at nominal power, then, in theory, there is no need for diode D_1 . However, a small diode should be used in order to prevent the reversal of the voltage across the electrolytic capacitor C_r during transient conditions.

However, a different criterion in the choice of C_r value can be adopted, since it influences the input current waveform during the switch on-time and, consequently, the current harmonic amplitudes. Thus, a tradeoff between such aspect and the switch voltage stress becomes necessary.

In order to complete the analysis, Fig. 3(b) shows the circuit behavior with a reduced C_r value which causes interval $T_r/4$ to be lower than interval T_{OFF} ; in addition to the higher peak voltage across it as compared to the previous case, which reflects to the transformer primary winding increasing the switch voltage stress, we can observe that i_μ can now reverse and at instant t^* it becomes equal in magnitude to the input current, but of opposite polarity. At that point, diode D stops conducting, the input current and the secondary magnetizing current remain equal, and go to zero, thus completing the reset interval. For a complete converter description, including current and voltage equations, during a line half period, see the Appendix.

III. MODIFIED RECTIFIER APPLICABILITY

As clearly demonstrated in [3] and [4], there is a wide variety of simple modifications of the conventional L - C diode rectifier which allows compliance with the IEC 1000-3-2 standard for loads having a rated power lower than 300 W. The basic idea is to exploit the difference between the absolute harmonic limitations applied to class A loads and the relative limitations applied to class D loads [1]. As is known, the difference can be remarkable, in particular, for low-power applications. Thus, the goal of these modified rectifiers is to change the shape of the input current so as to stay outside the Class D template, also shown in Fig. 2, for at least 5% of the line half period, i.e., 0.5 ms if the line frequency is 50 Hz. For the low-power range of applications, these solutions are surely cost effective.

If the required output power is in the range between 300–600 W, the same basic idea can be applied, but the simple

solutions proposed in [3] may be effectively replaced by a converter, such as the low-frequency-commutated boost presented in [5] and [6], whose schematic diagram is shown in Fig. 4. The same effect can be achieved also by the modified rectifier proposed in this paper. As a comparison, let us consider the case of a standard diode–capacitor rectifier with inductive filter. The scheme is the same as that of Fig. 1 without the switching unit. For an input voltage U_i of 230 V_{rms} (which is the standard voltage considered by IEC 1000-3-2) and a rated power of 300 W, simulations of the rectifier show that the minimum value of inductor L , which allows compliance with the standard, is 15.5 mH. In this case, the output voltage at the rated current is 292 V, due to the inductor voltage drop. As is well known, the resulting line current waveform classifies the rectifier as a Class D piece of equipment. The maximum power deliverable by the equipment is limited by the third harmonic, as stated also in [2]. The switching unit added to the standard passive L - C filter shown in Fig. 1 can achieve class A current absorption. The corresponding current drawn by the line for the same operating conditions, i.e., $U_i = 230$ V_{rms} and $P_o = 300$ W, is shown in Fig. 2. The figure shows that the input current waveform stays outside the Class D template for at least 5% of the line half-period, thus, the rectifier is now in Class A (it is important to remember that the Class D template must be centered to the highest current peak and scaled accordingly). As a consequence, the filter inductor needed to comply with the standard, at this power level, reduces to 3.4 mH. As will be explained in the following, the transformer has both a stored energy and a global size which is considerably smaller than the inductor's. Therefore, the converter actually reduces the total magnetic material required to comply with the standard, with respect to the passive solution.

A consequence of the switching unit operation is that the maximum load power is limited by the high-order harmonics (in this case, the 15th harmonic). The output voltage is stabilized at about 315 V, thanks to the lower inductor voltage drop and to the boost effect of the switching unit. Nevertheless, the solution proposed in [6] achieves the compliance almost with the same inductance value and, being a little bit simpler, it is probably the preferred choice for this power range.

If the required output power is higher than 600 W, the load is considered in class A, no matter what the current waveform. The modified rectifier has no longer the aim of modifying the input current to stay out of the class D template, but simply to improve the current harmonic content. The boost converter proposed in [5] and [6] requires inductor values (in the range) around 4.5 mH to achieve this goal. The solution we discuss here requires almost the same inductor. For instance, at $P_o = 600$ W, 4 mH is enough to comply with the standard. The presence of the transformer makes the boost solution still preferable. Table I sums up all of these comparative considerations and also includes other relevant data. These data were obtained by using a MATLAB program, which, solving the system differential equations, generates the ideal input current waveforms of a passive L - C rectifier (P), of a boost rectifier (A_1), and of the proposed active rectifier (A_2). Spectral analysis of these current waveforms was then performed to find the parameter values which allow compliance with the standards. The analysis has

TABLE I

COMPARISON BETWEEN PASSIVE AND ACTIVE RECTIFIERS AT DIFFERENT POWER LEVELS (P = PASSIVE; A_1 = ACTIVE BOOST RECTIFIER; A_2 = ACTIVE PROPOSED SOLUTION; THD = TOTAL HARMONIC DISTORTION; $\cos(\phi_1)$ = DISPLACEMENT FACTOR; PF = POWER FACTOR)

P_o [W]	U_o [V]	L [mH]	I_{gpeak} [A]	I_{grms} [A]	K_L [mJ]	K_{TR} [mJ]	I_{Spk} [A]	U_{Spk}/U_o [V]	THD	$\cos(\phi_1)$	PF
300 - P	291.8	15.5	4.16	1.81	117				0.827	0.932	0.718
300 - A ₁	314.9	4	4.59	1.81	33.3		2.95	1	0.945	0.995	0.723
300 - A ₂	314.9	3.4	4.81	1.83	30	5.7	0.65	1.09	0.973	0.994	0.713
600 - P	294.83	6.5	8.62	3.68	206				0.869	0.938	0.708
600 - A ₁	303.4	4.5	8.84	3.63	144		1.33	1	0.9	0.964	0.716
600 - A ₂	306	4	8.86	3.61	128	1.9	0.53	1.06	0.908	0.971	0.719
900 - P	258.96	18.5	9.8	5.12	929				0.523	0.861	0.763
900 - A ₁	290	9	10.01	4.82	434		2.66	1	0.612	0.952	0.812
900 - A ₂	301	7	9.8	4.72	324	46.6	1.24	1.29	0.625	0.977	0.829
1200 - P	230.7	28	12.2	6.97	2381				0.314	0.799	0.762
1200 - A ₁	273.6	16	11.21	6.16	1105		3.53	1	0.435	0.923	0.846
1200 - A ₂	285	11	11.38	5.94	744	131	1.49	1.48	0.459	0.959	0.872

been performed at 230 V_{rms} input voltage and assuming a constant output voltage. For each power level listed in the table (ranging from 300 to 1200 W), the following data were collected: average output voltage U_o ; inductor current value ensuring compliance with the standard (Class D for the passive solution up to 600 W and Class A for the active ones and for higher output power); input current peak value I_{gpeak} ; input current rms value I_{grms} ; inductor and transformer coefficients K_L and K_{TR} ; switch current (I_{Spk}) and normalized voltage stresses (U_{Spk}/U_o); total harmonic distortion (THD); displacement factor $\cos(\phi_1)$; and power factor (PF). Coefficients K_L and K_{TR} are related to the core size and are proportional to the product between the iron cross section A_e and the core window area A_w , as shown in the following expressions:

1) for an inductor

$$A_w A_e = \left(\frac{N}{k_R} \frac{I_{Lrms}}{J} \right) \left(\frac{L I_{Lpk}}{N B_{max}} \right) = \frac{K_L}{k_R J B_{max}} \quad (6)$$

2) for a transformer

$$A_e A_w = \frac{U_o T_{ON}}{B_{max}} \left(I_{pri_{rms}} + \frac{I_{sec_{rms}}}{n} \right) \frac{1}{J k_R} = \frac{K_{TR}}{k_R J B_{max}} \quad (7)$$

where

- B_{max} maximum flux density;
- J desired current density;
- k_R window-filling coefficient.

In the following, we will use these parameters as a measure of the magnetic components volume in order to compare different topologies. Note that, for an inductance, K_L is also related to the inductor peak energy, i.e., $K_L = (2E_L/CF)$ where $CF = (I_{pk}/I_{rms})$ is the crest factor.

By comparing the results in Table I and taking into account the previous remark on the transformer size, it is possible to conclude that the solution we discuss here can be effectively applied to reduce the size of the magnetic components necessary for compliance with IEC 1000-3-2, in particular, in the power range from 600 to 1200 W. Note also the reduction of the switch current stress at the expense of an increased voltage stress.

IV. DESIGN CONSIDERATIONS

A. Selection of Reactive Element Values

To develop a fully compliant rectifier, the first step is the selection of the L and C reactive element values. As far as the output capacitor value is concerned, a good guess is the value obtained by the approximate analysis of the classical diode-bridge + capacitive filter rectifier, i.e.,

$$C_L = \frac{P_o}{2f_{LINE} U_o \Delta U_{opp}} \quad (8)$$

where ΔU_{opp} is the maximum allowed output voltage ripple (peak to peak). Note that, due to the extended diode conduction angle, caused by the filter inductor, and the switching unit operation, the effective output voltage ripple will be lower than the theoretical one.

The choice of the filter inductor is more difficult and the design guidelines given here have to be verified by simulation. In case the desired output power is lower than 600 W, the goal is to modify the waveshape of the input current so as to take advantage of the less restrictive Class A limits. This single condition normally allows compliance with the standard. Thus, a good starting point should be an inductance value, which, without the help of the switching unit, achieves at least 60° of conduction angle, which is the width of the Class D template. Only in this case, in fact, the switching unit can increase the conduction angle so as the current waveform stays outside the Class D template for at least 5% of the line half period without using high T_{ON} values which would cause an increase in the transformer size and of the high-frequency current harmonics. For power levels above 600 W, no difference exists between Class D and Class A limits, thus, the inductor value should be progressively increased as the power increases. In fact, the extension of the conduction angle and the reduction of the current rate of change during the switch on-time are mandatory in order to keep the current harmonics below the limits.

B. Transformer Design

The objective of this work is to provide compliance with the standards with a reduced overall magnetic components' volume

as compared to the passive solution. To this purpose, the transformer size should be minimized by choosing the minimum switch on-time which provides the desired current harmonic reduction. This, together with the desired turns ratio, determines the winding number of turns. Then, for a complete transformer size estimation, the winding rms currents are calculated, approximating with a linear rise the shape of the input current during T_{ON} (see Fig. 3). From this figure, we obtain

$$I_{\text{secRMS}} = \sqrt{\left(I_{g0} \sqrt{\frac{2}{3}} \frac{T_{ON}}{T_g}\right)^2 + \left(\frac{n \hat{I}_\mu}{2} \sqrt{\frac{\omega_g}{\omega_r}}\right)^2} \quad (9)$$

$$I_{\text{priRMS}} = \left(\frac{I_{g0}}{n} + \hat{I}_\mu\right) \sqrt{\frac{2}{3}} \frac{T_{ON}}{T_g} \quad (10)$$

where I_{g0} is the input current value at the end of the T_{ON} interval.

In order to give an idea of the transformer dimensions, let us consider a practical example.

Converter specifications:

$$U_i = 220 \text{ V}_{\text{rms}} \pm 20\%, \quad P_o = 800 \text{ W}, \quad L = 6 \text{ mH}, \\ T_d = 2.8 \text{ ms}, \quad T_{ON} = 0.5 \text{ ms}, \quad n = 4.$$

The material used for both the inductor and the transformer has the following parameter values:

$$\text{relative permeability: } \mu_r = 11\,674; \\ \text{flux density: } B = 1.35 \text{ T}.$$

The utilized window-filling coefficient k_R is 0.4, and the current density J is 3 A/mm². The transformer parameters are as follows:

$$\text{iron cross section: } A_e = 2.56 \cdot 10^{-4} \text{ m}^2; \\ \text{window area: } A_w = 1.92 \cdot 10^{-4} \text{ m}^2; \\ \text{mean magnetic path: } \ell_{\text{avg}} = 0.104 \text{ m}; \\ \text{primary number of turns: } N_1 = 435; \\ \text{secondary number of turns: } N_2 = 109; \\ \text{magnetizing inductance: } L_\mu = 0.56 \text{ H}; \\ \text{primary wire diameter: } \Phi_1 = 0.25 \text{ mm}; \\ \text{secondary wire diameter: } \Phi_2 = 0.6 \text{ mm}; \\ \text{total winding area: } A_{cu} = 1.3 \cdot 10^{-4} \text{ m}^2; \\ \text{external core volume: } Vol = 3.07 \cdot 10^{-5} \text{ m}^3.$$

Note that the total winding area A_{cu} is well below the available window area A_w , meaning that the transformer size could be further reduced.

The inductor parameter, calculated for the maximum input current (i.e., minimum input voltage), are as follows:

$$\text{iron cross section: } A_e = 7.7 \cdot 10^{-4} \text{ m}^2; \\ \text{window area: } A_w = 3.63 \cdot 10^{-4} \text{ m}^2; \\ \text{mean magnetic path: } \ell_{\text{avg}} = 0.143 \text{ m}; \\ \text{number of turns: } N = 67; \\ \text{air gap: } t_{\text{gap}} = 0.36 \text{ mm}; \\ \text{wire diameter: } \Phi = 1.6 \text{ mm}; \\ \text{total winding area: } A_{cu} = 3.37 \cdot 10^{-4} \text{ m}^2; \\ \text{external core volume: } Vol = 1.27 \cdot 10^{-4} \text{ m}^3.$$

The rectifier output voltage at the minimum input voltage and nominal power is 222 V.

For the sake of comparison, a similar design was carried out for the passive solution. The inductor value needed to comply with the standard for the same converter specification is 15 mH. The resulting inductor parameters are as follows:

$$\text{iron cross section: } A_e = 1.12 \cdot 10^{-3} \text{ m}^2; \\ \text{window area: } A_w = 5.88 \cdot 10^{-4} \text{ m}^2; \\ \text{mean magnetic path: } \ell_{\text{avg}} = 0.182 \text{ m}; \\ \text{number of turns: } N = 111; \\ \text{air gap: } t_{\text{gap}} = 0.58 \text{ mm}; \\ \text{wire diameter: } \Phi = 1.6 \text{ mm}; \\ \text{total winding area: } A_{cu} = 5.58 \cdot 10^{-4} \text{ m}^2; \\ \text{external core volume: } Vol = 2.35 \cdot 10^{-4} \text{ m}^3.$$

The rectifier output voltage at the minimum input voltage and nominal power is 198 V. Comparing the resulting volumes, the reduction implied by the proposed solution is about 33%.

C. Selection of Switching Unit Parameters

The design of the proposed converter and switching unit is characterized by several degrees of freedom. All the design parameters are somehow related to one another; therefore, different design strategies can be identified. A possible procedure is to select the duration of the switch on-time, which directly determines the size of the transformer, to be as small as possible.

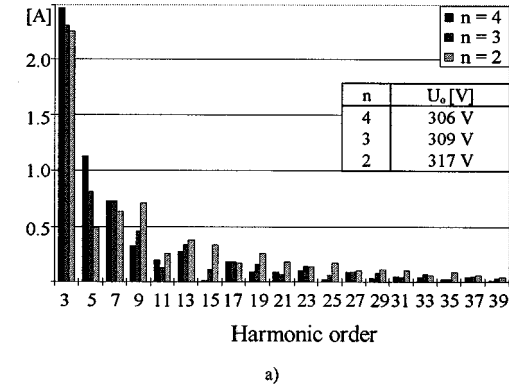
This choice again must be verified by simulations; once an on-time value is selected, the input current harmonic content must be evaluated to verify that it is within the standard limits. If this is the case, the on-time can be reduced until a suitable value is reached, which trades off the filter inductance value and the transformer size. When the switch on-time has been chosen, the transformer turns ratio $n = n_1/n_2$ has to be selected. The effect of the variation of this parameter is illustrated by Fig. 5. As can be seen, by increasing the turns ratio it is possible to improve the high-frequency harmonic content of the line current. This helps to limit the inductor value and/or the duration of the switch on-time needed to achieve compliance. The inevitable drawback is that, by increasing the turns ratio, the converter boost action reduces, and so the quality of the output voltage regulation worsens.

The effect of the turn-on delay T_d is described by Fig. 6. As can be seen, the increase of the delay initially reduces the harmonic content, but further increasing it implies an increase in the current peak value [Fig. 6(b)] and also in the harmonics.

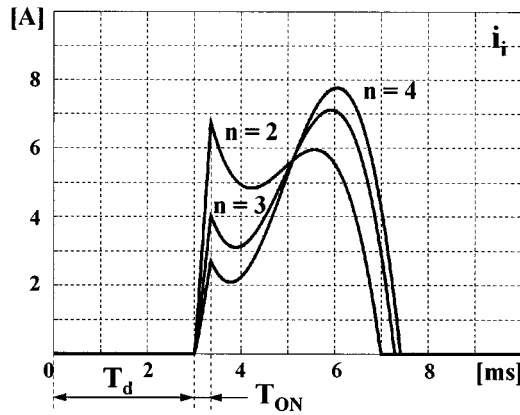
A further effect of the variation of the described control parameters is the variation of the output voltage achieved by the converter in open-loop conditions, which accounts for the boost capability of the rectifier. This is described by Figs. 5 and 6, too. As can be seen, both an increase of the delay and a reduction of the transformer turns ratio imply an increase in the boost action of the converter. This effect must be traded off against the previously discussed drawbacks.

D. Output Voltage Regulation

As far as the output voltage regulation is concerned, we must consider separately the effects of load and input voltage



a)

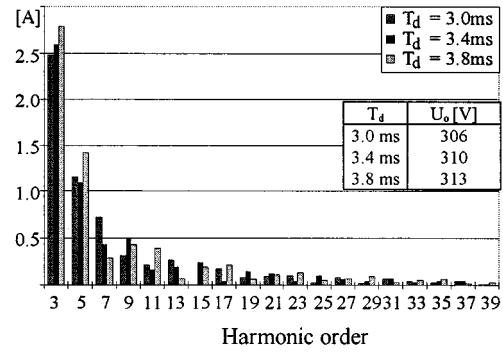


b)

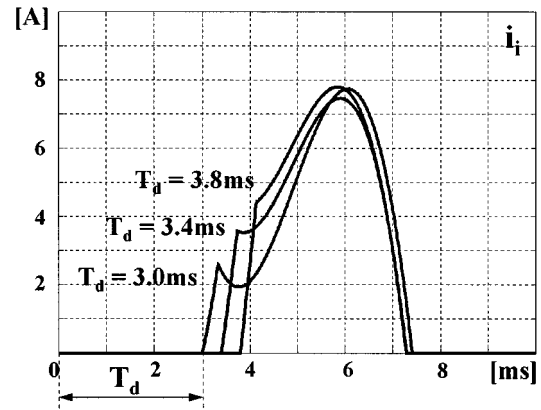
Fig. 5. Line current as a function of the transformer turns ratio. (a) Frequency domain. (b) Time domain ($U_i = 230 \text{ V}_{\text{rms}}$, $P_o = 600 \text{ W}$, $T_d = 3 \text{ ms}$, and $T_{\text{on}} = 360 \mu\text{s}$).

variations, having in mind the constraint imposed by the maximum switch on-time, which strongly affects the transformer size. Thus, once we have selected the maximum T_{ON} in order to achieve compliance with the standard at nominal load and prescribed input voltage, the control can only reduce the switch on-time at load current decreasing (delay time T_d is simply kept constant). A standard proportional–integral (PI) regulator having a bandwidth well below the line frequency, like any other PFC regulator, is sufficient to do this. Clearly, a minimum power level exists, below which the output voltage regulation cannot be maintained. It corresponds to the value for which the passive L – C rectifier (without the switching unit) achieves the same output voltage. At lower power levels, the output voltage increases toward the input voltage peak, like in any standard rectifier. For this reason, a high-output voltage reference is preferable, since it can be maintained for a broader load variation. To give an idea, the converter described in Section V can maintain the output voltage regulation approximately down to 30% of the nominal power.

Differently from the low-frequency boost converter presented in [5] and [6], the proposed topology does not achieve a high boost action unless a low transformer turns ratio is used (at the limit of a unity turns ratio the behavior of this structure becomes the same as in [5] and [6]). As a consequence, regulation of the output voltage can be maintained only for a small input voltage increase (which requires reduction of the switch



a)



b)

Fig. 6. Line current as a function of turn-on delay T_d . (a) Frequency domain. (b) Time domain ($U_i = 230 \text{ V}_{\text{rms}}$, $P_o = 600 \text{ W}$, $T_{\text{on}} = 360 \mu\text{s}$, and $n = 4$).

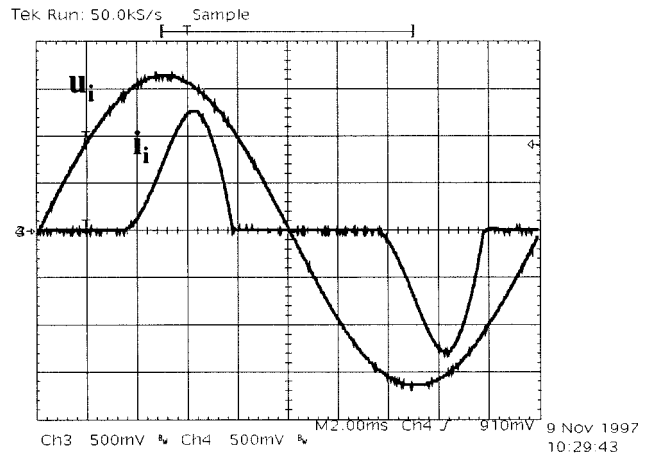


Fig. 7. Input voltage U_i (100 V/div) and current i_i (5 A/div) ($U_i = 230 \text{ V}_{\text{rms}}$ and $P_o = 900 \text{ W}$).

on-time), while, at low input voltage, T_{ON} is kept constant and equal to the maximum value allowed by the transformer design, causing the decrease of the output voltage, too.

V. EXPERIMENTAL MEASUREMENTS

In order to verify the results obtained by simulation, a prototype was built having the following specifications:

$$U_i = 230 \text{ V}_{\text{rms}}, \quad U_o = 300 \text{ V}, \quad P_o = 900 \text{ W}, \\ L = 5.3 \text{ mH}, \quad C_L = 2 \times 470 \mu\text{F}, \quad n = 4.$$

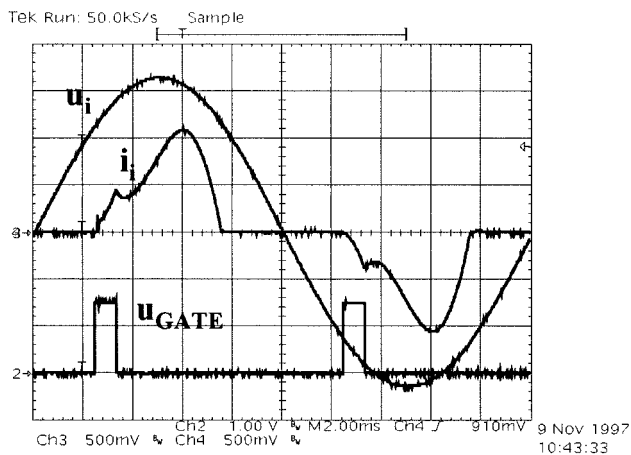


Fig. 8. Input voltage U_i (100 V/div), input current i_i (5 A/div), and gate signal U_{gate} (10 V/div) ($U_i = 230$ V_{rms} and $P_o = 900$ W)

TABLE II
MEASURED INPUT CURRENT HARMONICS AT DIFFERENT OUTPUT POWER LEVELS FOR THE PROPOSED RECTIFIER

P_o [W]	600	700	800	900	Class A limits
I_n	Har. [A _{rms}]	Har. [A _{rms}]	Har. [A _{rms}]	Har. [A _{rms}]	[A _{rms}]
I_1	2.736	3.209	3.595	4.100	
I_3	1.739	2.038	2.223	2.293	2.30
I_5	0.825	0.932	1.123	1.016	1.14
I_7	0.448	0.487	0.618	0.708	0.77
I_9	0.318	0.326	0.173	0.137	0.40
I_{11}	0.041	0.058	0.235	0.273	0.33
I_{13}	0.182	0.200	0.137	0.128	0.21
I_{15}	0.103	0.081	0.103	0.114	0.15
I_{17}	0.067	0.095	0.126	0.113	0.132
I_{19}	0.111	0.107	0.035	0.030	0.118
I_{21}	0.027	0.017	0.103	0.085	0.107
I_{23}	0.075	0.089	0.013	0.031	0.098
I_{25}	0.059	0.041	0.072	0.052	0.09

Note that, according to the conclusions reported at the end of Section III, a 900-W output power was selected, since the proposed line-frequency-commutated rectifier shows significant advantages over other existing solutions only for power values above 600 W.

Initially, the rectifier was tested without activating the switching unit. The line voltage and current measured in these conditions are shown in Fig. 7. It is important to notice that, in all the performed measurements, a controlled low-impedance voltage source is used as the test power supply. This allows an almost harmonic-free input voltage, as required by the IEC standards. For the passive L - C rectifier, the harmonic content of the current drawn from the utility grid is above the standard limits, in particular, in the third and fifth harmonic components, as predicted by the simulations.

TABLE III
EXPERIMENTAL COMPARISON OF ACTIVE AND PASSIVE RECTIFIERS AT DIFFERENT POWER LEVELS (P = PASSIVE; A_1 = PROPOSED SOLUTION)

P_{in} [W]	U_o [V]	I_o [A]	T_d [ms]	T_{ON} [μ s]	η [%]
621 (P)	299	2.02			97.2
618 (A_1)	307	1.96	3.00	360	97.4
725 (P)	297	2.37			97.1
724 (A_1)	304	2.31	3.00	360	97.0
827 (P)	295	2.72			97.0
826 (A_1)	303	2.64	2.80	380	96.8
928 (P)	294	3.07			97.3
931 (A_1)	301	3.00	2.45	890	97.0

When the switching unit is activated, the current waveform modifies as shown in Fig. 8, where the main converter waveforms at nominal conditions are depicted. The turn-on delay T_d of the gate signal was set to 2.8 ms. As can be seen, the input current waveform agrees well with the simulation results reported in Fig. 2, the main difference being the reduced T_{ON} value. This indicates that the converter behaves as expected, in agreement with the analysis reported in Section II and with the simulations. However, it is worth underlining that, in this case, the control parameters are different with respect to Fig. 2 because the goal here is to improve the current harmonic content so as to comply with the IEC Class A standard and not to get out of the Class D template, as was the case shown in Fig. 2. The 900-W output power, in fact, already qualifies the converter as a Class A piece of equipment. As expected, compliance with the standard is achieved and only the high-order components of the current spectrum get near to the allowed limit values. The harmonic components of the current spectrum can be seen in Table II, again for different power levels. Harmonics from the 19th up to the 25th are normally the closest to the corresponding limits, thus confirming the simulation results. However, for the higher power levels (i.e., 800 and 900 W in Table II), the margin on the low-order harmonics tends to reduce, thus limiting the power throughput of the converter. This is due to the fact that the adopted inductor is undersized for these output power levels, being only 5.3 mH. From Table I, in fact, it is possible to see that a 6 ÷ 7-mH value would probably be a safer choice. Anyway, as can be seen, the proposed solution allows compliance with the IEC-1000-3-2 standard with a quite low inductance compared to fully passive solutions. The 5.3-mH inductor adopted in the laboratory prototype allows increasing the power level to about 900 W, without exceeding the standard harmonic limits. It is worth noting that, as explained in Section IV, the size of the necessary transformer is a fraction of the inductor's size. Therefore, the overall size of the magnetic components of the power rectifier is greatly reduced as compared to the passive solutions. The measured efficiency of the modified rectifier when the switching unit is activated is always above 96%, as shown by Table III. Table III also shows that the difference between active and passive (i.e., with the switching unit turned off) solution efficiency is practically negligible. In addition to the efficiency, Table III reports other measured data which allow evaluation of the different performance of the active and passive rectifier; the boost capability of the active solution, for instance, is indicated

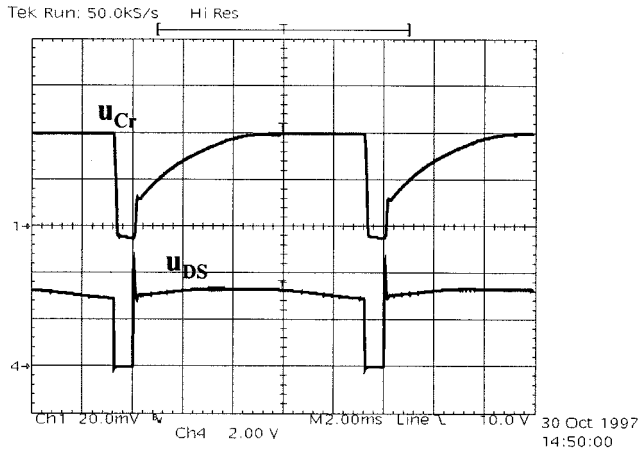


Fig. 9. Reset capacitor C_r voltage u_{Cr} (4 V/div) and drain-source voltage on the IGBT (200 V/div)

by the open-loop output voltage achieved by the rectifier. As can be seen, the difference between the output voltage in the active and passive rectifier for a given output power is in the range of $7 \div 8$ V, thanks to the switching unit operation. Finally, the behavior of the reset circuitry and of the adopted power switch [insulated gate bipolar transistor (IGBT)] snubber are shown by Fig. 9. The drain-source voltage exhibits a controlled overshoot which is kept by the snubber [100 nF, 390 Ω (1 W)] to an acceptable level for a 600-V switch. The voltage across the reset capacitor is quite low, the reset time being long as compared to the switch on-time.

VI. CONCLUSIONS

The proposed low-frequency switched PFC is a simple and low-cost solution to achieve compliance with EMC standards together with output voltage stabilization in ac/dc power supplies for household and general-purpose applications. As compared to a passive rectifier, it allows substantial reduction of the inductive components' volume at the expense of a limited increase of circuit complexity.

The added switch allows regulation of the output voltage against load variations, without affecting the converter efficiency. The solution seems to be more effective in the power range above 600 W.

APPENDIX

We first derive the input current equations during the different time intervals in the line half period, supposing the circuit behavior is as shown in Fig. 10. Different situations are considered afterwards. The output capacitor is considered big enough to maintain constant the output voltage. The input voltage is given by

$$u_g(t) = \hat{U}_g |\sin(\omega_g t)|.$$

1) Interval T_d : $0 \leq t \leq T_d$: In this interval, the input current remains zero and the reset capacitor voltage is U_{C0} . The switch is turned on after a delay T_{di} measured from the line

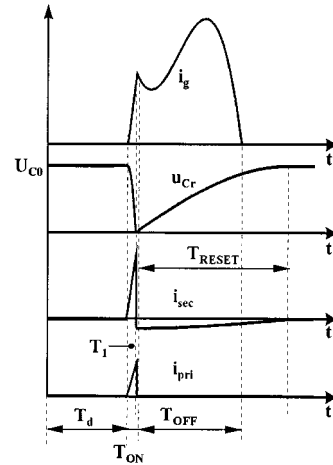


Fig. 10. Converter main waveforms in a line half period and corresponding subtopologies.

voltage zero crossing; however, the input starts to flow after a delay time T_d given by

$$T_d = \max\{T_{di}, T_{dn}\} \quad (\text{A.1})$$

where T_{dn} is the diode-bridge natural turn-on instant, i.e.,

$$T_{dn} = \frac{1}{\omega_g} a \sin\left(\frac{U_1}{\hat{U}_g}\right) \quad (\text{A.2})$$

where $U_1 = U_o(1 - (1/n)) - U_{C0}$. The corresponding topology is shown in Fig. 10.

2) $T_d \leq t \leq T_d + T_{ON}$: The first part of such interval is dominated by the resonance between the input inductor and the reset capacitor. The input current and the capacitor voltage are given by

$$\begin{aligned} i_g(t) = & a_i [\cos(\omega_g t') - \cos(\omega_a t')] \\ & + b_i \left[\sin(\omega_g t') - \frac{\omega_g}{\omega_a} \sin(\omega_a t') \right] \\ & + \left(\frac{U_{g0} - U_1}{\omega_a L} \right) \sin(\omega_a t') \end{aligned} \quad (\text{A.3a})$$

$$\begin{aligned} u_{Cr}(t) = & U_{C0} - a_u \left[\sin(\omega_g t') - \frac{\omega_g}{\omega_a} \sin(\omega_a t') \right] \\ & - b_u \left[(1 - \cos(\omega_g t')) - \left(\frac{\omega_g}{\omega_a} \right)^2 (1 - \cos(\omega_a t')) \right] \\ & - (U_{g0} - U_1) (1 - \cos(\omega_a t')) \end{aligned} \quad (\text{A.3b})$$

where $t' = t - T_d$ $U_{g0} = \hat{U}_g |\sin(\omega_g T_d)| \geq U_1$, $\omega_a = (1/\sqrt{LC_r})$ and

$$\begin{aligned} a_i &= -b_i \sqrt{\left(\frac{\hat{U}_g}{U_{g0}}\right)^2 - 1} \\ a_u &= -b_u \sqrt{\left(\frac{\hat{U}_g}{U_{g0}}\right)^2 - 1} \\ b_i &= -\frac{U_{g0}}{\omega_g L} \left(\frac{\omega_g^2}{\omega_a^2 - \omega_g^2}\right) \\ b_u &= -U_{g0} \left(\frac{\omega_a^2}{\omega_a^2 - \omega_g^2}\right). \end{aligned} \quad (\text{A.3c})$$

If C_r is completely discharged before the end of the switch on-time (let us call $T_1 < T_{\text{ON}}$ the duration of its discharge interval), then diode D1 turns on, short circuiting C_r , as shown in Fig. 10(b). The input current expression becomes

$$\begin{aligned} i_g(t) &= I_{g0} + \frac{\hat{U}_g}{\omega_g L} \left[\cos(\omega_g (T_d + T_1)) - \cos(\omega_g t) \right. \\ &\quad \left. - \frac{U_o}{\hat{U}_g} \left(1 - \frac{1}{n}\right) \omega_g (t - T_d - T_1) \right] \end{aligned} \quad (\text{A.4})$$

where I_{g0} is the current value given by (A.3a) at instant $t = T_d + T_1$.

3) $T_d + T_{\text{ON}} \leq t \leq T_d + T_{\text{ON}} + T_{\text{OFF}}$: In this interval, two distinct processes occur, i.e., the main resonance between the input inductor and the output filter capacitor and the secondary resonance between the transformer magnetizing inductance and the reset capacitor C_r , as described by (2). The corresponding subtopology is shown in Fig. 10(c); from it, the input current expression can be derived as

$$\begin{aligned} i_g(t) &= I_{g1} + \frac{\hat{U}_g}{\omega_g L} \left[\cos(\omega_g (T_d + T_{\text{ON}})) - \cos(\omega_g t) \right. \\ &\quad \left. - \frac{U_o}{\hat{U}_g} \omega_g (t - T_d - T_{\text{ON}}) \right] \end{aligned} \quad (\text{A.5})$$

where I_{g1} is the current value given by (A.4) at instant $t = T_d + T_{\text{ON}}$. The input current goes to zero at the instant $t = T_d + T_{\text{ON}} + T_{\text{OFF}}$, turning off the bridge diodes. Instead, the transformer reset continues until the magnetizing current reaches zero, as shown in Fig. 10.

Different situations with respect to what we have described above can occur depending on the component values. In particular, the reset capacitor could not be completely discharged during the switch on time. In this case (2) must be changed to

$$\begin{aligned} i_\mu(t) &= \hat{I}_\mu \cos(\omega_r t) - \frac{U_{C1}}{nZ_r} \sin(\omega_r t) \\ u_{C_r}(t) &= Z_r n \hat{I}_\mu \sin(\omega_r t) + U_{C1} \cos(\omega_r t) \end{aligned} \quad (\text{A.6})$$

where U_{C1} is the residual voltage across C_r at the end of the switch on-time, as given by (A.3b) for $t = T_d + T_{\text{ON}}$.

Lastly, if the magnetizing current reverses its polarity before the input current reaches zero, after an interval $T_2 < T_{\text{OFF}}$

from the switch turn-off instant, the two currents become equal in magnitude, but of opposite polarity, causing the turn off of diode D. After that, the situation is as shown in Fig. 10(d) in which the resonance between the sum of the input inductance and the magnetizing inductance reflected to the secondary side and the reset capacitor C_r occurs until the two currents go to zero. During such interval, the input current and the capacitor voltage are given by the following expression:

$$\begin{aligned} i_g(t) &= a_i [\cos(\omega_g t') - \cos(\omega_{a1} t')] \\ &\quad + b_i \left[\sin(\omega_g t') - \frac{\omega_g}{\omega_{a1}} \sin(\omega_{a1} t') \right] \\ &\quad + I_{g2} \cos(\omega_{a1} t') + \left(\frac{U_{g2} - U_2}{\omega_{a1} L_T} \right) \sin(\omega_{a1} t') \end{aligned} \quad (\text{A.7a})$$

$$\begin{aligned} u_{C_r}(t) &= U_{C2} - a_u \left[\sin(\omega_g t') - \frac{\omega_g}{\omega_{a1}} \sin(\omega_{a1} t') \right] \\ &\quad - b_u \left[(1 - \cos(\omega_g t')) - \left(\frac{\omega_g}{\omega_{a1}} \right)^2 (1 - \cos(\omega_{a1} t')) \right] \\ &\quad - Z_{a1} I_{g2} \sin(\omega_{a1} t') - (U_{g2} - U_2) (1 - \cos(\omega_{a1} t')) \end{aligned} \quad (\text{A.7b})$$

where I_{g2} , U_{g2} , and U_{C2} are the current value given by (A.5), the input voltage, and the reset capacitor voltage given by (A.6), respectively, calculated at instant $t = T_d + T_{\text{ON}} + T_2$, and

$$\begin{aligned} t' &= t - T_d - T_{\text{ON}} - T_2 \\ L_T &= L + \frac{L_\mu}{n^2} \\ \omega_{a1} &= \frac{1}{\sqrt{L_T C_r}} \\ Z_{a1} &= \sqrt{\frac{L_T}{C_r}} \end{aligned} \quad (\text{A.7c})$$

$$\begin{aligned} a_i &= -b_i \sqrt{\left(\frac{\hat{U}_g}{U_{g2}}\right)^2 - 1} \\ b_i &= -\frac{U_{g2}}{\omega_g L_T} \left(\frac{\omega_g^2}{\omega_{a1}^2 - \omega_g^2}\right) \\ a_u &= -b_u \sqrt{\left(\frac{\hat{U}_g}{U_{g2}}\right)^2 - 1} \\ b_u &= -U_{g2} \left(\frac{\omega_{a1}^2}{\omega_{a1}^2 - \omega_g^2}\right). \end{aligned} \quad (\text{A.7d})$$

REFERENCES

- [1] *Electromagnetic compatibility (EMC)-Part 3: Limits-Section 2: Limits for harmonic current emissions (equipment input current ≤ 16 A per phase)*, IEC1000-3-2 Document, 1st ed., 1995.
- [2] M. M. Jovanovic and D. E. Crow, "Merits and limitations of full-bridge rectifier with LC filter in meeting IEC 1000-3-2 harmonic-limit specifications," in *Proc. IEEE APEC'96*, Mar. 1996, pp. 354-360.

- [3] R. Redl and L. Balogh, "Power-factor correction in bridge and voltage-doubler rectifier circuits with inductors and capacitors," in *Proc. IEEE APEC'95*, Mar. 1995, pp. 466–472.
- [4] —, "An economical single-phase passive power-factor-corrected rectifier: Topology, operation, extensions, and design for compliance," in *Proc. IEEE APEC'98*, Feb. 1998, pp. 454–460.
- [5] I. Suga, M. Kimata, Y. Ohnishi, and R. Uchida, "New switching method for single-phase AC to DC converter," in *Proc. PCC-Yokohama*, 1993, pp. 93–98.
- [6] L. Rossetto, G. Spiazzi, and P. Tenti, "Boost PFC with 100 Hz switching frequency providing output voltage stabilization and compliance with EMC standards," in *Conf. Rec. 1998 IEEE-IAS Annu. Meeting*, St. Louis, MO, pp. 1567–1573.



Simone Buso (M'98) was born in Padova, Italy, in 1968. He received the M.S. degree in electronic engineering and the Ph.D. degree in industrial electronics from the University of Padova, Padova, Italy, in 1992 and 1997, respectively.

Since 1993, he has been with the Power Electronics Laboratory, University of Padova, where he is currently a Researcher in the Department of Electronics and Informatics. His main research interests include dc/dc converters, smart power IC's, digital control, and robust control of power converters.



Giorgio Spiazzi (S'91–M'93) was born in Legnago, Italy, in 1962. He graduated *cum laude* in electronic engineering and received the Ph.D. in industrial electronics and informatics from the University of Padova, Padova, Italy, in 1988 and 1993, respectively.

He is currently a Researcher in the Department of Electronics and Informatics, University of Padova. His main research interests are in the fields of advanced control techniques of dc/dc converters, power-factor correctors, soft-switching techniques, and electromagnetic compatibility in power electronics.