Power Factor Preregulators Based on Combined Buck-Flyback Topologies

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***Abstract*—The limitation imposed on the achievable power level by the IEC 1000-3-2 standard in buck-derived power factor preregulators, is overcome by using a combined buck-flyback power stage. Two different step-down converters are proposed in this paper, which incorporate an auxiliary flyback stage. The auxiliary stage uses the same switch of the main converter, plus an additional power switch commutated at the line frequency. As compared to a simple buck rectifier, with this solution the harmonic content of the absorbed line current, at a given power level, can be reduced, thanks to the resulting increased conduction angle of the input rectifier bridge.**

Experimental results based on a 1 kW prototype are reported to validate the theoretical analysis of the proposed topologies.

***Index Terms*—AC–DC converters, buck converter, electromagnetic compatibility, flyback converter, power factor correction.**

I. Introduction

OFF-LINE converters connected to the utility grid, which supply equipment having a rated current lower than 16A/phase, must provide a reduced input current harmonic content, so as to comply with international standards like the IEC 1000-3-2 [1]. High-quality rectifiers based on the boost topology have already been widely analyzed in the literature and are also commonly used in the industry due to their inherent advantages over other topologies, i.e., simplicity, input current filtering due to the input inductance, almost unity power factor when working in CCM (continuous conduction mode) with average current mode control [2], [3]. On the other hand, the lack of any limitation of the inrush current at start-up and of short-circuit protection calls for additional provisions, like a series switch, which increase cost and complexity of the complete rectifier. Moreover, the output voltage is constrained to be higher than the peak input voltage (i.e., $U_o = 380$–400 V for universal input voltage range).

The use of buck-type power factor preregulators (PFP's) allows to overcome the aforementioned drawbacks at the expense of a greater input current distortion, both at line and switching frequency. The low frequency distortion in the line current arises from its unavoidable notches around the zero crossings of the line voltage, caused by the inability of the buck converter to draw current when the instantaneous input voltage is lower than the output one. As a consequence, the power that a buck-type preregulator can handle while still complying with the IEC 1000-3-2 standard is limited.

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In order to overcome this limitation, two step-down topologies are proposed which include a main buck converter and an auxiliary flyback stage. The latter is used to absorb current even during the time intervals in which the main buck converter is inactive. In this way, the input current distortion is reduced, thus increasing the useful power range. Differently from the scheme proposed in [4], the auxiliary flyback stages considered in this work use the same switches of the main converter for the modulation and require only a single additional line-frequency-commutated switch. Moreover, in one of the proposed solutions, the auxiliary converter can be rated for a fraction of the total power.

In the first part of the paper, the operation of a buck-type preregulator is reviewed and the maximum power for which the IEC 1000-3-2 standard harmonic limits are met is calculated for different voltage conversion ratios and modulation strategies. Successively, the two proposed combined buck-flyback topologies are presented and suitable design criteria are given.

Lastly, the paper presents simulation and experimental results which confirm the theoretical expectations.

II. Review of Buck-Based Preregulators

The basic scheme of a buck converter used as a preregulator is shown in Fig. 1. It consists of a diode bridge rectifier followed by a standard buck converter.

As in boost-based preregulators, the output capacitor filters the low-frequency components of the input power. However, unlike the boost converter, the converter shown in Fig. 1 is able to draw current from the line only when the input voltage is greater than the output voltage. As a consequence, notches appear in the line current around zero crossing of the line voltage, causing distortion.

In the following analysis of the low frequency harmonic content of the line current generated by this kind of converter, two different modulation strategies will be considered, i.e., constant-current reference (also called input-current-clamping) and sinusoidal-current reference. The advantages of using constant-current reference are the reduced current stresses of the power semiconductors and the limited current level around the peak of the line voltage, which could partially compensate for the peak-clipping effect of conventional diode-capacitor rectifiers. On the other hand, a sinusoidal-current reference allows, for the same voltage conversion ratio, a higher input power without exceeding the harmonic limits.

Fig. 2(a) shows a typical filtered line current waveform of the converter, obtained by using a sinusoidal-current reference, which gives the lowest possible current distortion. A typical filtered input current waveform for constant-current reference is instead shown in Fig. 2(b).

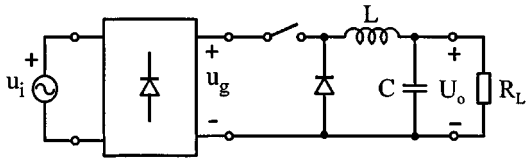


Fig. 1. Buck-based power factor preregulator.

As can be seen, in both cases, the input current remains zero until the input voltage becomes greater than the output one. Clearly, the dead angle $\theta_d = \omega t_d$ at the beginning and at the end of the line half-period is a function of the voltage conversion ratio M, i.e.,

$$\theta_d = \sin^{-1}(M), \qquad M = \frac{U_o}{\hat{U}_g} \tag{1}$$

where $\hat{U}_g$ is the line voltage peak. The initial limited slope of the input current is unavoidable since the inductor current can increase with a slope limited by $(u_g–U_o)/L$, which is very low at the beginning of the conduction phase (u_g close to U_o).

A comparison between the current spectrum and the limits imposed by IEC 1000-3-2 standard for Class A (Class D equipment limits are the same for a power greater than 600 W) shows that the Buck PFP solution, for this particular output power and voltage conversion ratio, does not meet the standards for high-order harmonics. Thus, it becomes interesting to find the maximum power that a Buck-based PFP converter can deliver while satisfying the standards for different voltage conversion ratios.

III. Analysis of the Current Absorbed by a Buck Preregulator

This section is dedicated to the analysis of the line current harmonic content of the Buck PFP, both for constant and sinusoidal current reference, and is aimed at determining the maximum output power which can be delivered to the load while meeting the IEC-1000-3-2 standard requirements. In the following analysis, the mark over the variables stands for averaging in the modulation period.

A. Constant-Current Reference

As we can see from Fig. 2(b), the average input current can be approximated by a square wave, for which the peak harmonic currents are given by

$$I_{n\_\text{peak}} = \frac{4I_{\text{REF}}}{n\pi} \cdot \cos(\theta_d). \tag{2}$$

In practice, the input current waveform has an equivalent dead angle greater than θ_d due to the limited inductor current slope when the current starts to flow. The duration of this operation mode depends on input and output voltages and inductance values.

From (2) it is possible to find the maximum input power that the buck converter can deliver without exceeding the standards (IEC 1000-3-2 Class A equipment). The results are shown in Fig. 3(a) as a function of the voltage conversion ratio for an input voltage level of 230 V_{RMS} (as requested by the standards). As we can see, with this type of modulation the load power cannot exceed some hundred Watts.

For higher voltage conversion ratios the dead angle θ_d increases, thus increasing the input current harmonic content. Note the peaks in the curves of Fig. 3(a) which occur at 50 and 71.5% of duty-cycle revealing some harmonics cancellation at these duty-cycle values. Results obtained with other idealized input current waveforms are given in [5].

The curves end for a duty-cycle equal to 85% in order to remain within the Class A specifications (for higher duty-cycles the input current waveform belongs to Class D).

B. Sinusoidal-Current Reference

Using a sinusoidal-current reference, the maximum input power achievable tends to infinity as M approaches zero, because the average input current becomes a pure sinusoid. Analyzing an ideal truncated sinusoidal waveform [approximation of the real behavior shown in Fig. 2(a)], as the one given by (3), the input current harmonic content is given by (4) and (5)

$$\bar{i}_g(\theta) = \begin{cases} \hat{I}_g|\sin(\theta)| & \text{for } \theta_d + h\pi \le \theta \le (h+1)\pi - \theta_d \\ 0 & \text{for } -\theta_d + h\pi \le \theta \le \theta_d + h\pi \end{cases} \qquad h = 0, 1, 2, \cdots \tag{3}$$

$$I_{1\_\text{peak}} = \hat{I}_g \cdot F, \quad F = \left|1 - \frac{2\theta_d}{\pi} + \frac{\sin(2\theta_d)}{\pi}\right| \tag{4}$$

$$I_{n\_\text{peak}} = \frac{2\hat{I}_g}{\pi} \cdot \left|\frac{\sin[(n+1)\theta_d]}{n+1} - \frac{\sin[(n-1)\theta_d]}{n-1}\right| \qquad n = 3, 5, 7 \cdots. \tag{5}$$

The peak of the average input current can be found from (4) and the power balance, and turns out to be

$$\hat{I}_g = \frac{2P_o}{\hat{U}_g} \frac{1}{F}. \tag{6}$$

The plot of the maximum input power calculated in the same conditions of Fig. 3(a) is reported in Fig. 3(b).

Combined sinusoidal- and constant-current reference techniques can be used in order to gain some advantages of both approaches. In this case the maximum power achievable lays between the corresponding curves of Fig. 3(a) and (b).

IV. Analysis of the Current Absorbed by a Combined Buck-Flyback Preregulator

In this section a modified PFP structure is considered where an auxiliary Flyback converter is parallel connected with the main Buck preregulator. The resulting combined structure can be schematically represented as in Fig. 4. The use of this structure as a PFP offers some advantages compared to the simple Buck PFP, as is shown in the following.

As we have seen, the dead angle of the input current strongly affects the maximum power delivered by a conventional converter. Thus, by allowing current absorption during the time intervals in which the main buck converter is inactive, the maximum power achievable can be greatly increased. A possible implementation of this principle is presented in [4] where the

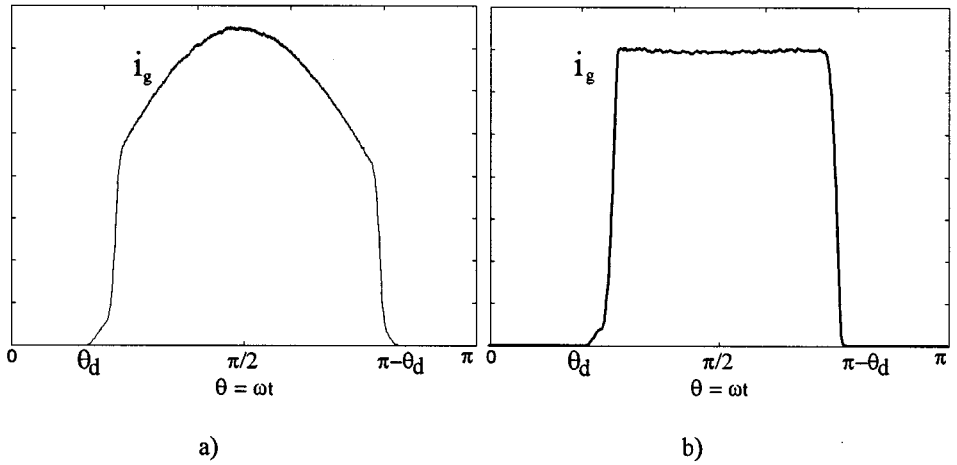


Fig. 2. Filtered line current waveform of the buck preregulator: (a) sinusoidal-current reference and (b) constant-current reference.

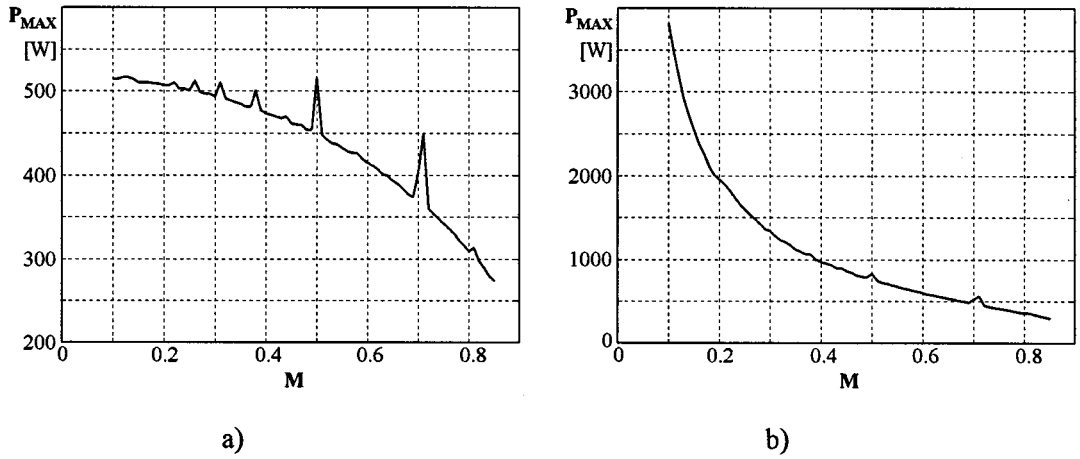


Fig. 3. Maximum input power as a function of voltage conversion ratio $M(U_g = 230\ \mathrm{V_{RMS}})$: (a) constant-current reference modulation and (b) sinusoidal-current reference modulation.

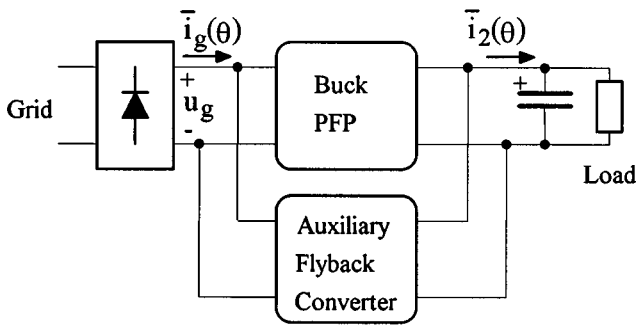


Fig. 4. Schematic of the combined buck-flyback PFP.

proposed topology includes, besides the main buck converter, an auxiliary parallel flyback converter feeding the same load, exactly as in Fig. 4. This auxiliary power stage is activated only in the interval of the line period in which the main converter is idle and thus can be designed to handle a power which is just a small fraction of the total input power. One of the drawbacks of the solution given in [4] is that a complete second power stage is needed, thus increasing the cost of the converter. In this work instead, different solutions are considered, which integrate the buck and the flyback stages, thus reducing the components' count.

However, independently from the selected topology, a typical filtered input current waveform for this combined PFP, is shown in Fig. 5 (in case of sinusoidal-current reference). As we can see, the sinusoidal reference peak value for the flyback operation is kept intentionally lower than that for the buck operation, in order to limit the power handled by the flyback stage to the minimum required to satisfy the harmonic standards and, at the same time, not to worsen the peak current stress of the main converter switch.

The harmonic analysis of the line current can be performed on an idealized waveform, which approximates the behavior shown in Fig. 5. The expression for the idealized current is given in (7)

$$\bar{i}_g(\theta) = \begin{cases} \hat{I}_g|\sin(\theta)| & \text{for } \theta_d + h\pi \le \theta \le (h+1)\pi - \theta_d \\ k\hat{I}_g|\sin(\theta)| & \text{for } -\theta_d + h\pi \le \theta \le \theta_d + h\pi \end{cases} \quad h = 0, 1, 2, \cdots \tag{7}$$

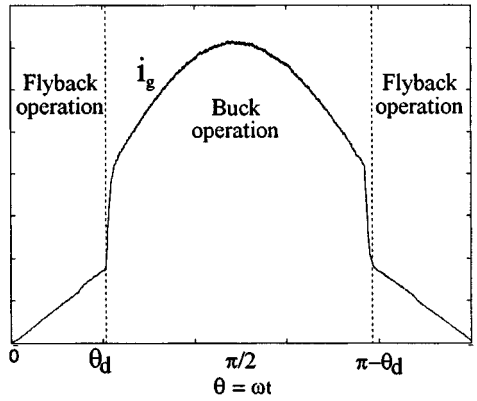


Fig. 5. Simulated filtered line current waveform for the buck-flyback converter in case of sinusoidal-current reference ($k = 0.25$).

where k is the ratio between the sinusoidal reference peak value for the flyback operation and the sinusoidal reference peak value for the buck operation. Note that, for $k = 1$, the ideal absorbed current becomes a pure sinusoid.

As far as the analysis results are concerned, the expressions derived in the Buck PFP analysis remain essentially valid, provided that the factor F is modified as

$$F = \left| 1 - \frac{2\theta_d(1-k)}{\pi} + \frac{(1-k)\sin(2\theta_d)}{\pi} \right|. \tag{8}$$

Therefore, the harmonic content of the line current can be expressed as in (9) and (10)

$$I_{1\_\text{peak}} = \hat{I}_g \cdot F \tag{9}$$

$$I_{n\_\text{peak}} = \frac{2\hat{I}_g(1-k)}{\pi} \cdot \left| \frac{\sin[(n+1)\theta_d]}{n+1} - \frac{\sin[(n-1)\theta_d]}{n-1} \right| \quad n = 3, 5, 7 \cdots. \tag{10}$$

The peak $\hat{I}_g$ of the average input current is again given by (6).

Comparing (4) with (8) and (9), the peak of the fundamental component of the input current absorbed by the flyback stage is given by

$$I_{1\_\text{fly}} = \frac{k\hat{I}_g}{\pi} \cdot |-2\theta_d + \sin(2\theta_d)|. \tag{11}$$

Thus, the ratio between the power handled by the flyback stage and the total input power is simply given by

$$\frac{P_{\text{fly}}}{P_{tot}} = \frac{I_{1\_\text{fly}}}{I_{1\_\text{peak}}}. \tag{12}$$

A plot of this power ratio as a function of the voltage conversion ratio is reported in Fig. 6(a) for different values of parameter k. These curves show that, if M is not too high, it is possible to design a converter for whatever power level is needed, while keeping the power rating of the auxiliary stage at a small fraction of the total power.

The curves in Fig. 6(b) show the maximum power achievable with the converter of Fig. 4. From this plot it is possible to derive, for given input and output voltages, the value of parameter k which ensures input current harmonics complying with the standards. Then, the plots of Fig. 6(a) allow to find the power rating of the flyback stage components.

It is important to note that similar results can be obtained also for the constant reference current. However, in this case, for the same power, a greater utilization of the flyback stage is needed in order to comply with the standards. Moreover, the maximum power is in any case limited, because of the square-wave shape of the absorbed current [see Fig. 3(a)]. More information about this modulation technique can be found in [4].

In order to simplify the analysis carried out in the following sections, some modifications of the classical relations of PFP's are needed to take into account the modified input current waveform shown in Fig. 5. In particular, since the converters in Fig. 4 store negligible energy at line frequency, the average output current $\bar{i}_2(\theta)$ can be calculated from power balance as

$$\bar{i}_2(\theta) = \frac{p_{\text{in}}(\theta)}{U_o} = \frac{\hat{U}_g \hat{I}_g \sin^2(\theta)}{U_o}\,\alpha \tag{13}$$

where $\alpha = 1$ during buck operation and $\alpha = k$ during flyback operation. As a consequence, the apparent load seen by the converter results

$$r_L(\theta) = \frac{U_o}{\bar{i}_2(\theta)} = \frac{R_L}{2\alpha \sin^2(\theta)}\,F \tag{14}$$

which differs from the usual form for the presence of correcting factors α and F.

V. Combined Buck-Flyback Implementations

The first proposed converter topology which implements the scheme of Fig. 4 is shown in Fig. 7. Diode bridge (D_1–D_4), switch S_1 and components D_6, L and C form the main buck power stage, while the remaining components constitute the auxiliary flyback converter. One important difference with respect to the solution proposed in [4] is that the flyback stage exploits the same switch of the buck converter (S_1) to perform the modulation, while switch S_A is operated at line frequency in order to enable and disable the auxiliary flyback converter. Diode D_6 was added in order to prevent the discharge of the output capacitor during the flyback operation.

Another possible topology implementing the scheme of Fig. 4 is depicted in Fig. 8. It represents a modified tapped-inductor buck converter in which a diode D_6 and an auxiliary line commutated switch S_A are added. The principle of the converter's operation is similar to that of the preceding scheme. When S_A is kept closed, the converter becomes a flyback stage in which diode D_6 acts as rectifying diode. Instead, when S_A is open the converter operates in a conventional tapped-inductor buck PFP mode. The latter, behaves very similarly to a standard buck, with the exception of the current waveform in the windings. In fact, during the switch on-time, the current in the two windings N_1 and N_2 is the same and increases with a slope equal to $(u_g–U_o)/L$, while during the switch off-time, the input current zeroes, and current i_2 steps up to maintain the flux continuity in the core. As a consequence, the voltage conversion ratio, for continuous conduction mode (CCM), modifies as

$$m(\theta) = \frac{U_o}{u_g(\theta)} = \frac{d(\theta)}{1 + \dfrac{1-d(\theta)}{n}} \tag{15}$$

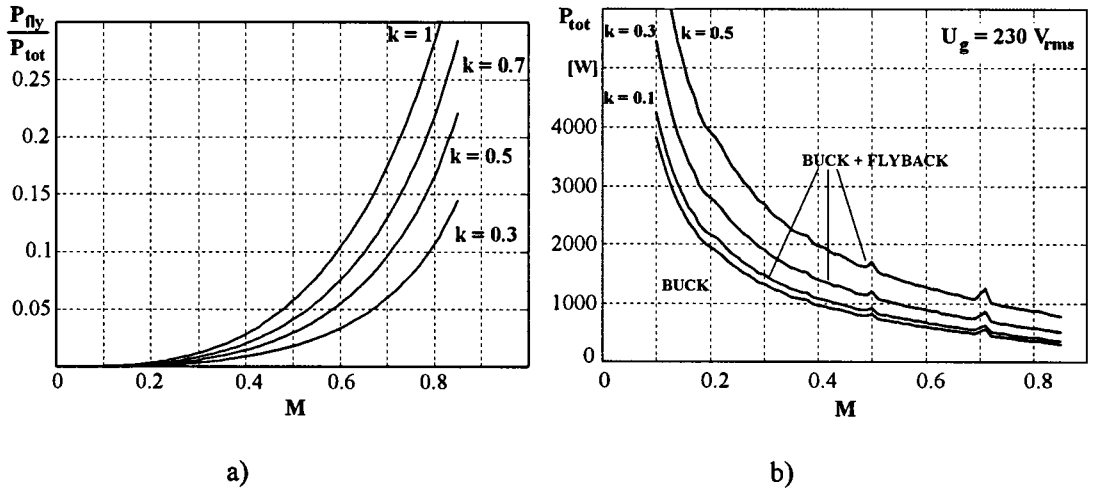


Fig. 6. (a) Normalized power of flyback stage as a function of output voltage conversion ratio M for different values of parameter k and (b) maximum input power as a function of voltage conversion ratio M in case of sinusoidal-current reference.

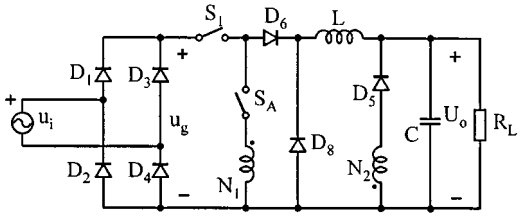


Fig. 7. Proposed combined buck-flyback converter (solution A).

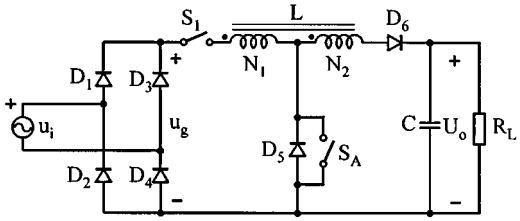


Fig. 8. Proposed combined buck-flyback converter (solution B).

where $d(\theta)$ is the duty-cycle and $n = N_2/N_1$ is the turns ratio. The switch current and voltage stresses become

$$\hat{i}_S(\theta) = U_o \left[\frac{1}{r_L(\theta)} \frac{n + m(\theta)}{n+1} + \frac{1 - m(\theta)}{2Lf_S} \left(\frac{1+n}{n+m(\theta)} \right) \right] \tag{16}$$

$$\hat{u}_S(\theta) = u_g(\theta) + \frac{U_o}{n}. \tag{17}$$

VI. Design Guidelines

In the following, suitable design guidelines for the two buck-based power factor preregulators are given. The converter shown in Fig. 7 is indicated as solution A, while that shown in Fig. 8 is indicated as solution B.

A. Solution A

1) Inductor: The peak of the average inductor current can be calculated from (13) by letting $\theta = \pi/2$, i.e.,

$$\hat{I}_L = \bar{i}_2(\theta)|_{\theta=\pi/2} = \frac{\hat{I}_g}{M} \tag{18}$$

where $\hat{I}_g$ is given by (6) and (8). The maximum value of its instantaneous current ripple results

$$\Delta i_{L\,\max} = \Delta i_L|_{\theta=\pi/2} = \frac{U_o}{Lf_s}(1 - M). \tag{19}$$

The inductor value can then be calculated from the desired maximum current ripple

$$L = \frac{U_o}{\hat{I}_g} \frac{M}{2f_s r_i}(1 - M) \tag{20}$$

where

$$r_i = \frac{\Delta i_{L\,\max}}{2\hat{I}_L}. \tag{21}$$

The maximum instantaneous inductor current, which coincides with the primary switch current stress, can be calculated from (18) and (19).

2) Capacitor: As usual, the output filter capacitor is selected from the constraint regarding the low-frequency output voltage ripple. The latter is derived by integrating the capacitor current over part of a half-line period. The expression for the capacitor current is as follows:

$$\bar{i}_C(\theta) = \bar{i}_2(\theta) - I_o. \tag{22}$$

The worst case peak-to-peak voltage ripple is given by

$$\Delta u_o = \frac{1}{2\omega C} \left[(\pi - 2\theta_1)(\hat{I}_2 - 2I_o) + \hat{I}_2 \sin(2\theta_1) \right] \tag{23}$$

where ω is the line angular frequency, $\hat{I}_2$ is the peak value of $\bar{i}_2(\theta)$, and

$$\theta_1 = \sin^{-1}\left(\sqrt{\frac{I_o}{\hat{I}_2}} \right). \tag{24}$$

Capacitor C is then selected from (23) based on the desired output voltage ripple.

3) Transformer Turns Ratio: The selection of the transformer turns ratio is a trade-off between voltage and current switch stresses; in particular, during flyback operation the maximum switch voltage stress is given by

$$\hat{u}_{s\,\max}(\theta) = \hat{u}_s(\theta_d) = u_g(\theta_d) + \frac{N_1}{N_2} U_o = \left(1 + \frac{N_1}{N_2}\right) U_o \tag{25}$$

while, during buck operation, the maximum voltage stress is limited to $\hat{U}_g$.

4) Transformer Magnetizing Inductance L_μ: Assuming a discontinuous conduction mode of operation (DCM) for the auxiliary flyback stage, the main switch current stress, during the flyback mode, is given by

$$\hat{i}_S(\theta) = S_{\text{fly}}(\theta)\, d(\theta) T_S \tag{26}$$

where $S_{\text{fly}}(\theta)$ is the current slope given by

$$S_{\text{fly}}(\theta) = \frac{u_g(\theta)}{L_\mu}. \tag{27}$$

The average input current during the flyback operation is

$$\hat{i}_g(\theta) = \hat{i}_S(\theta)\, \frac{d(\theta)}{2} = k \hat{I}_g |\sin(\theta)|. \tag{28}$$

Thus, from (26)–(28), the maximum switch current stress results

$$\hat{i}_{S\,\max} = \hat{i}_S(\theta_d) = \sqrt{2k\hat{I}_g |\sin(\theta_d)| S_{\text{fly}}(\theta_d) T_S} \tag{29}$$

from which the transformer magnetizing inductance can be found by imposing a switch current stress equal to that calculated during the buck operation.

B. Solution B

1) Inductor: Differently from the previous case, in the converter shown in Fig. 8, buck and flyback operating mode are achieved using the same power stage components. As a consequence, some degrees of freedom in the converter design are lost. In particular, the inductor value L and the turns ratio n now determine current and voltage stresses during both buck and flyback operation. Thus, during buck mode, the switch current stress can be found by substituting the voltage conversion ratio

$$m(\theta) = \frac{U_o}{u_g(\theta)} = \frac{M}{|\sin(\theta)|} \tag{30}$$

and the apparent load expression (14) into (16), thus obtaining the following equation for $\theta = \pi/2$:

$$\hat{i}_{S\,\max} = U_o \left[\frac{2}{R_L} \frac{n+M}{n+1} F + \frac{1-M}{2Lf_S} \left(\frac{1+n}{n+M}\right)\right]. \tag{31}$$

During the flyback mode, instead, assuming DCM operation, the switch current stress is given by (29), where the current slope S_{fly} is now

$$S_{\text{fly}}(\theta) = \frac{u_g(\theta)}{L_1} = \frac{u_g(\theta)}{L} (1+n)^2 \tag{32}$$

which is much higher as compared to that of the buck operation.

As far as the switch voltage stress is concerned, it is given by (17) calculated for $\theta = \pi/2$. From all the above equations the following converter design procedure can be outlined.

1) Given the nominal power and voltage conversion ratio, the minimum value of k is calculated which makes compliance with the standards.
2) The value of turns ratio n is selected from the desired switch voltage stress.
3) The inductor value is calculated from the desired switch current stress in the buck mode (31).
4) The maximum switch current stress during the flyback mode is checked: if it is lower then the value given by (31) a higher value of n can be selected; in the other case, a lower value of n should be chosen, thus increasing the voltage stress, or a higher current stress should be accepted. An optimum design should give the same current stress during both flyback and buck modes.

2) Capacitor: It is selected following the same guidelines outlined for the first proposed converter [see (22)–(24)].

It is worth noting that the proposed solutions present different advantages and drawbacks. Solution A is more complicated but offers the possibility of limiting the active component current and voltage stresses to that of a simple buck converter. Solution B instead, is topologically simple, but increases the component voltage stress to the level of the incorporated flyback converter; the voltage stress, therefore, must be carefully controlled by a proper design.

Finally, as far as a comparison with boost preregulators is concerned, the following aspects regarding the buck-type preregulators must be taken into account.

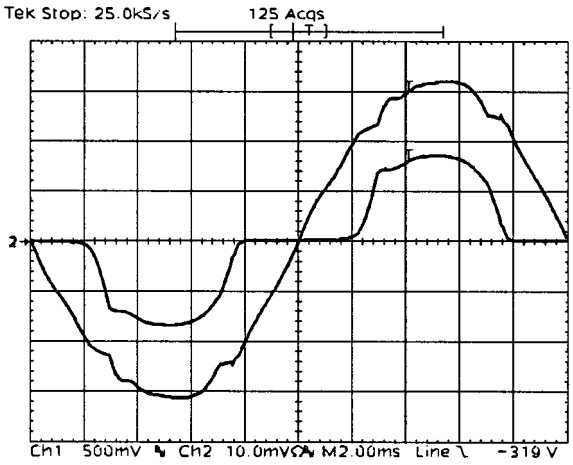
1) The required EMI filter is heavier as compared to the boost PFP's due to the high-frequency chopped input current; consequently, their overall efficiency may turn out to be lower.
2) The required output capacitor value, for a given relative output voltage ripple and output power, is higher as compared to the boost PFP's, because of the higher output current (consequence of a lower output voltage) as well as of the reduced value of current $\bar{i}_2(\theta)$ during flyback operation [see (13)]. Moreover, for applications in which the hold-up time is an issue, the low output voltage of the buck preregulators calls for a much higher capacitor value as compared with the boost PFP's to get the same stored energy.

VII. Experimental Results

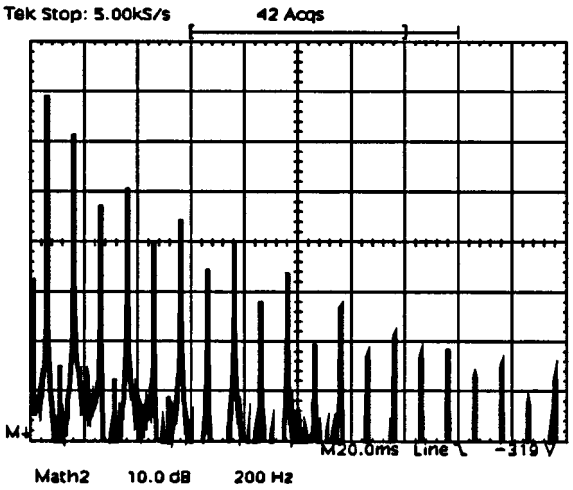
The lastly proposed topology (solution B) has been experimentally tested. A converter having the specifications and parameters listed in Table I was built in order to verify the theoretical expectations.

TABLE I
CONVERTER PARAMETERS

U_g = 176÷264 V_{RMS}	U_o = 185 V	P_o = 1000 W
L = 580 μH	C = 2·680 μF	f_s = 50 kHz
n = 0.8		



a)



b)

Fig. 9. (a) Line voltage [100 V/div] and current [5 A/div] during buck operation and (b) spectrum of the line current—top line corresponds to 24 dBA_{RMS} [10 dB/div].

A charge control is used in order to force a sinusoidal average input current for both buck and flyback operation modes, i.e., the input current is sensed and integrated cycle by cycle. The main switch S_1 is turned on at constant frequency and turned off when the integral of the switch current reaches a suitable sinusoidal reference (after that the integrator is reset) [6]. To implement such control, a standard PFC controller like the MC34261, which is normally used in boost PFC's designed to operate at the boundary between continuous and discontinuous conduction modes, was employed with some external circuitry.

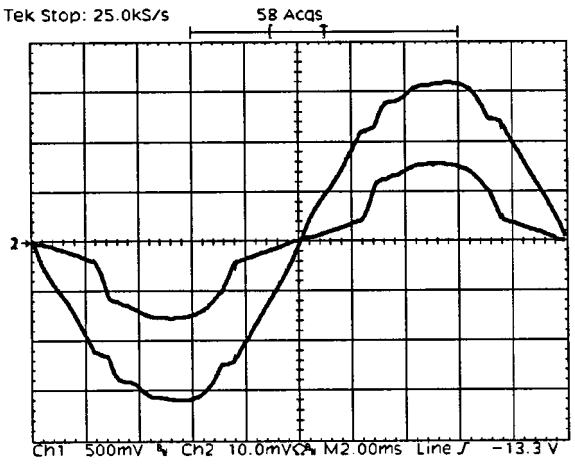
TABLE II
LINE CURRENT HARMONICS

Harmonic Order	Buck [A_{RMS}]	Buck+ Flyback [A_{RMS}]	IEC 1000-3-2 [A_{RMS}]
1	4.695	4.650	
3	1.930	1.195	2.30
5	0.374	0.160	1.14
7	0.560	0.335	0.77
9	0.162	0.035	0.40
11	0.278	0.175	0.33
13	0.082	0.050	0.21
15	**0.166**	**0.110**	**0.15**
17	0.040	0.025	0.13
19	0.088	0.065	0.12
21	0.016	0.010	0.11

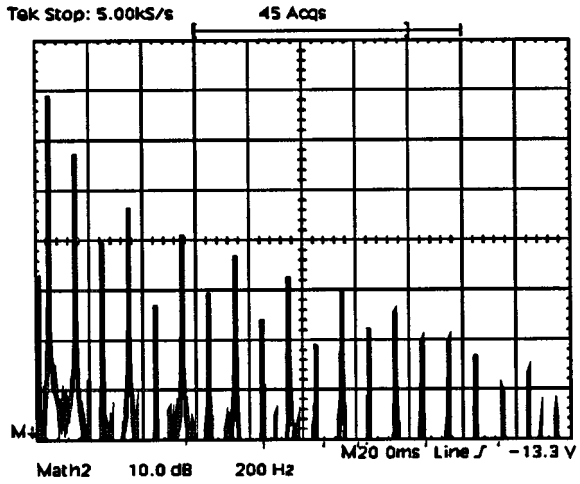
The converter was tested at first in the tapped inductor buck PFP configuration. The outcoming filtered line current is shown in Fig. 9(a) together with the line voltage. The distortion in the voltage waveform is due to the impedance of the transformer used to connect the converter to the grid. The spectrum of the line current is shown in Fig. 9(b). Note that in the following measurements the input voltage amplitude is set to 230 V_{RMS}, as requested by the standards. As it is possible to see, the line current exhibits a noticeable low frequency distortion due to the dead-zone around the voltage zero crossings.

Nevertheless, as is confirmed by Table II which reports the amplitude of the first 19 harmonics, it is only the 15th harmonic which is above the limit imposed by the IEC 1000-3-2 standard. This basically depends on the output voltage level which, being fairly low with respect to the line voltage peak amplitude, allows a quite large conduction interval for the buck converter. For higher output voltage levels this may no longer be the case and lower order harmonics can be expected to exceed the standard limits.

The filtered input current waveform during operation of both buck and flyback stages is shown in Fig. 10(a) together with its spectrum [Fig. 10(b)]; as it is possible to verify in Table II, the converter now complies with the standards.



a)



b)

Fig. 10. (a) Line voltage [100 V/div] and current [5 A/div] during buck-flyback operation and (b) spectrum of the line current—top line corresponds to 24 $\mathrm{dBA_{RMS}}$ [10 dB/div].

VIII. Conclusion

The use of buck-type converters as power factor preregulators is limited by their inherent input current distortion to a maximum input power level, depending on the required voltage conversion ratio. Exceeding such power limit implies the violation of the IEC 1000-3-2 standards, normally in the high order harmonic range.

The use of combined buck-flyback preregulators allows to extend the power handling capability of such rectifiers by drawing current from the input during the whole line period.

Experimental results taken from a converter prototype based on one of the presented buck-flyback topologies demonstrate the validity of the proposed solution.

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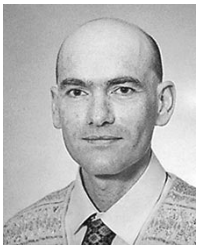

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