Titolo: Smart Monitoring and Production Optimization for Zero-waste Semiconductor Manufacturing: SMART-IC

Codice Progetto: 2022T7YSHJ

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Coordinatore nazionale: Politecnico di Torino

Partner-Unità di ricerca: Università degli Studi di Verona - Università degli Studi di Padova

CUP: C53D23003670006

Bando: PRIN 2022 - Decreto Direttoriale n. 104 del 02-02-2022

Durata: 28/09/2023 - 27/09/2025 (24 mesi)

Budget totale progetto: 285.899,00 €

Budget UNIPD: 89.977,00 €

Abstract del progetto: In recent years, data became the main driver of innovation in manufacturing, particularly with the advent of Machine Learning-based technologies for process optimization. This is the revolution, called Industry 4.0 (I4.0), introduced decentralized, self-organizing and self-learning systems for production control, with new machine learning algorithms getting increasingly powerful to solve real world problems, like predictive maintenance and anomaly detection. On the other hand, many data-driven applications are still far from being optimized to cover many aspects and the complexity of modern industries. In particular, data-driven dynamic scheduling and allocation in complex manufacturing scenarios have been only partially developed by the literature. Moreover, the correlations between smart monitoring, production scheduling and anomaly detection/predictive maintenance have been only partially exploited, while they could be beneficial to improve effectiveness and reduce production machinery wear. The integration of all such aspects into a coherent analysis and optimization production flow is a challenging task.

The SMART-IC is to develop new data-driven approaches for smart monitoring and production optimization. Themain objective focus of the project is semiconductor manufacturing, one of the most technologically advanced and data-intensive industrial sectors, where process quality, control and simulation tools are critical for decreasing costs and increasing yield. Additionally, the increased semiconductor demand and the simultaneous global chip shortage make waste reduction and effectiveness improvement extremely critical. In SMART-IC we aim at reducing defect generation at the electronic component level and, therefore, its propagation to the system level and then to the system-of-system (SoS) level. SMART-IC main ambition is to inspect, detect and reduce all relevant wafer level defects, and among those, to identify and contain the 'latent' defects on mask and wafers during the components manufacturing. With advanced inspections, consisting of massive inspection systems, interconnected sensors and component functional safety real time monitoring module, vast amount of generated data will allow to model, monitor and feedback earlier phases of the IC manufacturing, to minimize the number of defects at each process steps and by that to reduce the waste products at all levels, which will require to be recalled from the field, recycled or re-used. It is important to note that this goal falls in the indications of the Chips Act and of the Industrial Strategy, promulgated in February 2022 by the European Commission: both documents underline the need for "devices [...] designed for energy efficiency and durability, repairability, upgradability, maintenance, reuse and recycling".

This project has also very high industrial value as reported by the endorsement letter of STMicroelectronics.