RF building blocks and techniques for low power wireless transceiver

Green Technologies Enabling Energy Saving

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- **Bias sharing**
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  - Filtering base-band ADC
- **Adaptive optimization**
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Introduction

The reduction of power consumption in modern wireless transceivers can be achieved following **two main strategies**

Power recycling

- Lower instants dissipation
- Low level of optimization
- Less complexity and devices

Power re-configurability

- Lower average dissipation
- High level of optimization
- Increment of system complexity

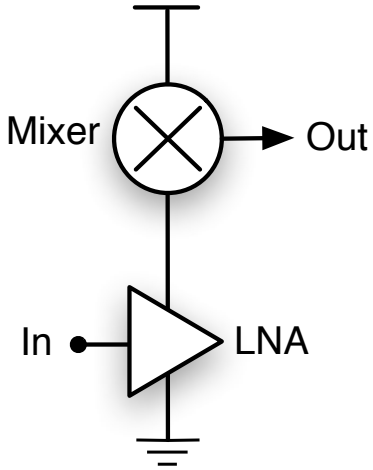
Share and re-use

Sharing bias current and devices for very low power RF front-ends

Low power strategies

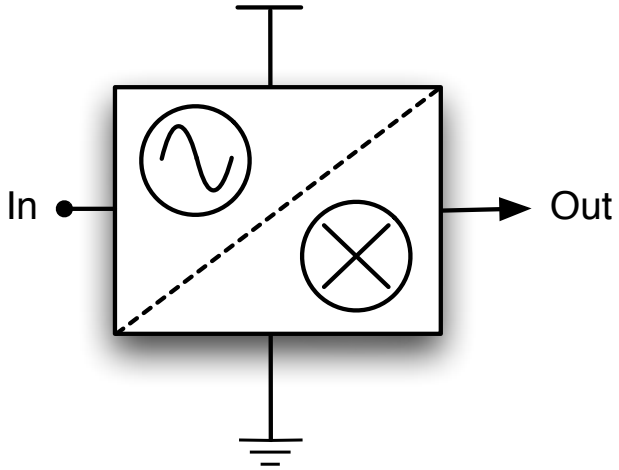
Wireless sensor network (WSN), ZigBee, GPS, demand very low power transceivers to increase battery life

Stacking Blocks



(e.g. bias sharing)

Merging Functionalities



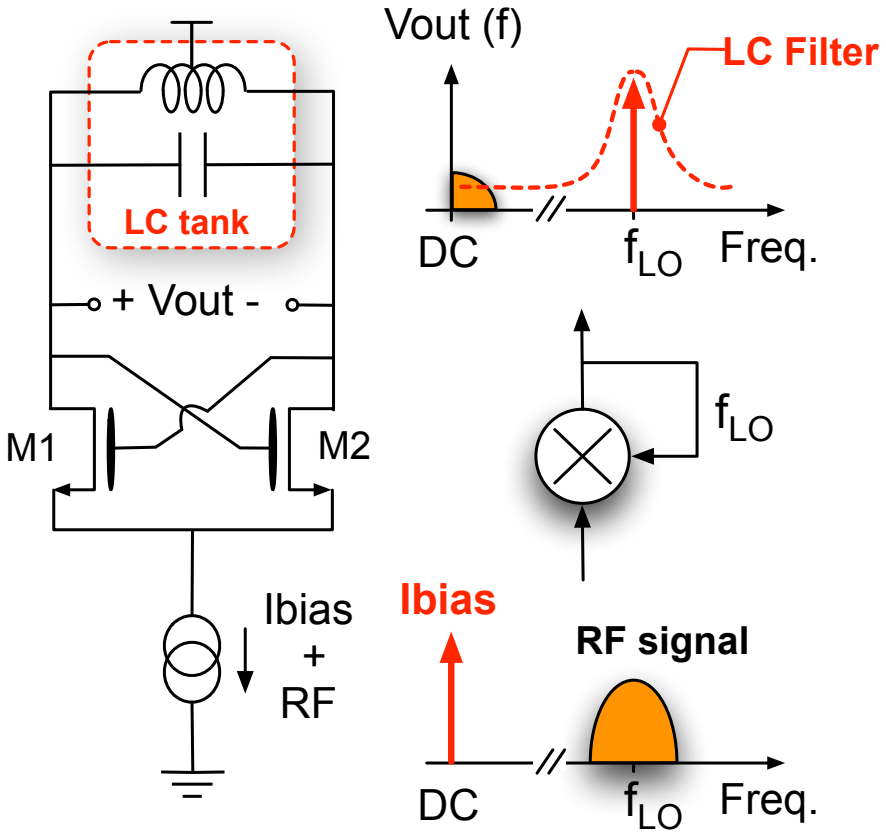
(e.g. self-oscillating mixer)

Our target: to combine "stacking" and "merging functionality" in a single stage RF quadrature front-end

LNA-Mixer-VCO cell

Sharing bias current and devices for very low power RF front-ends

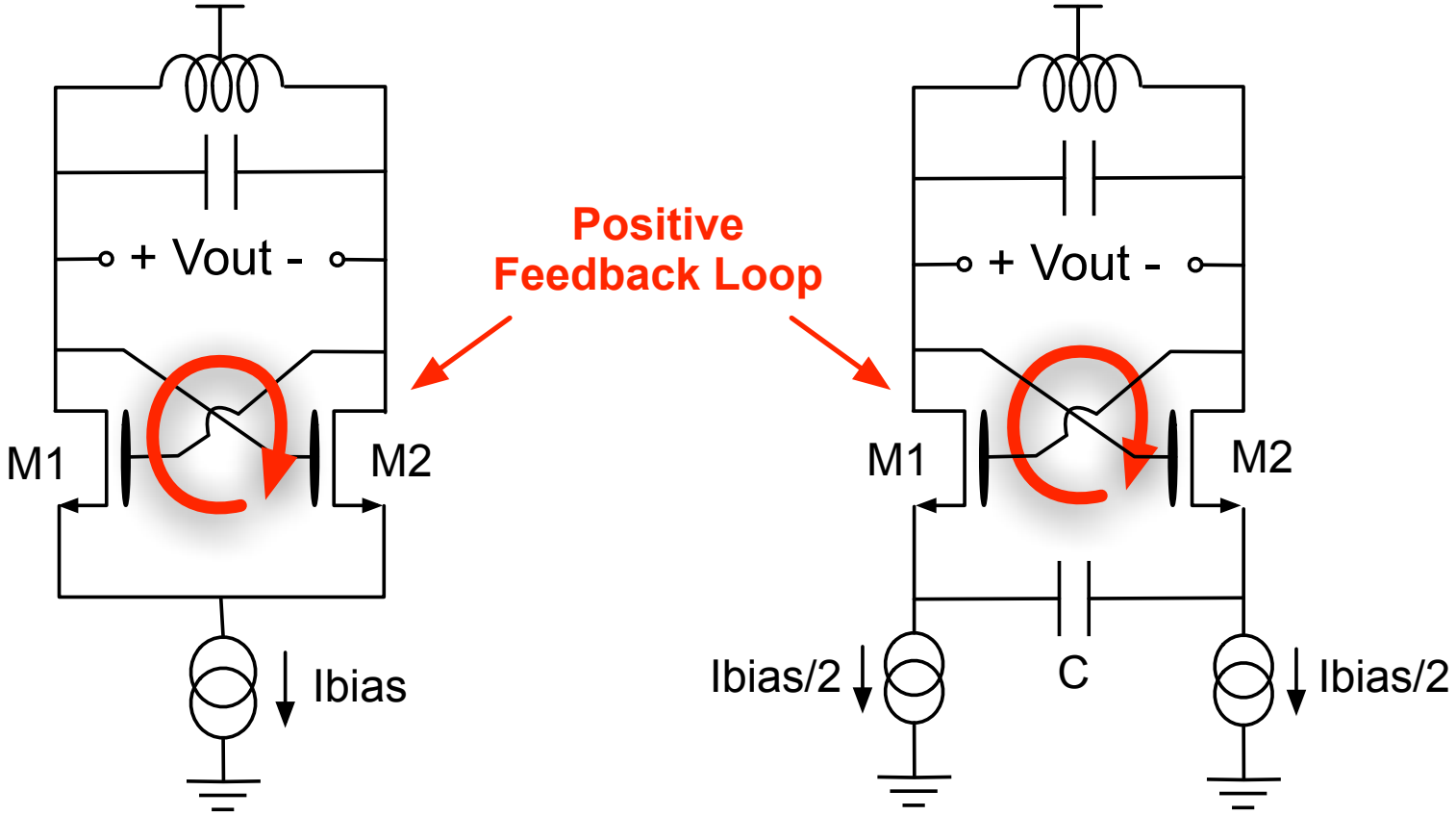
The LC tank oscillator as a mixer



- An oscillator can be seen as a mixer that up-convert its bias
- RF signal in the bias current can be down-converted
- LC tank attenuates the down-converted signal

How sense the down-converted signal preserving oscillation?

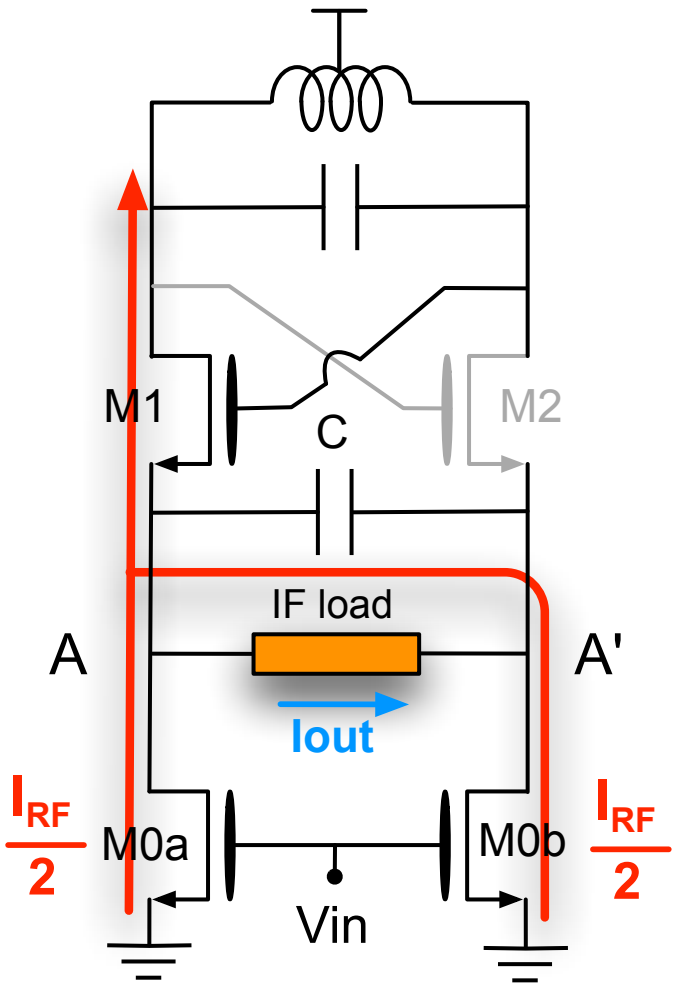
Bias splitting



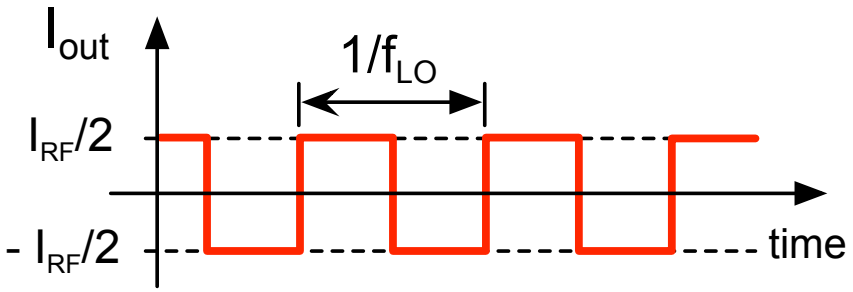
The capacitance C closes the loop at RF preserving the oscillation

(Oscillation condition $C >> gm_{1,2}/\omega_{LO}$)

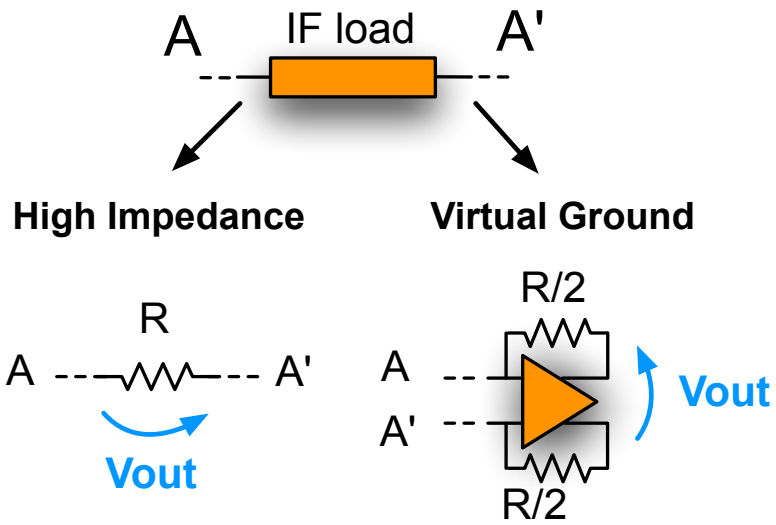
Bias split oscillator as mixer



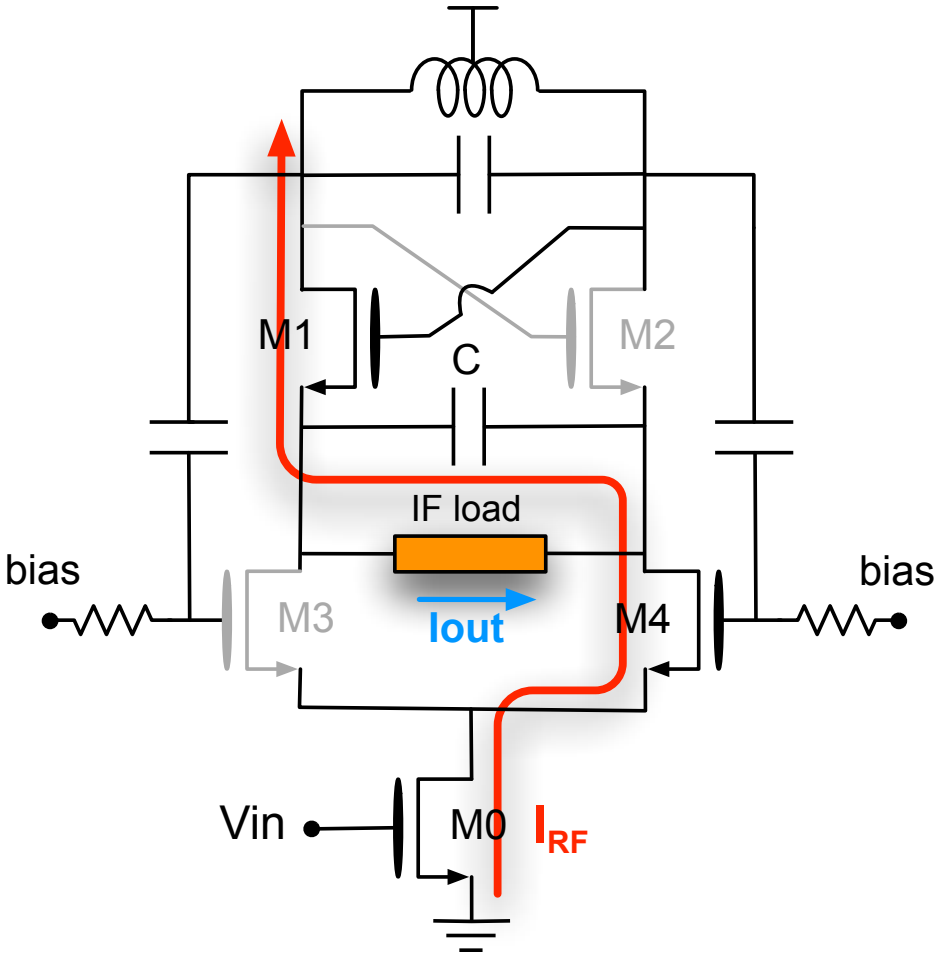
(Semi-period with M1 on)

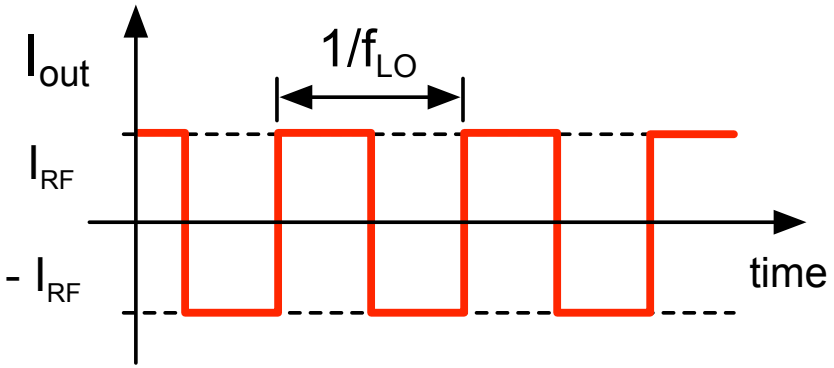


Only half of the signal current flows through IF load



Double switching pair



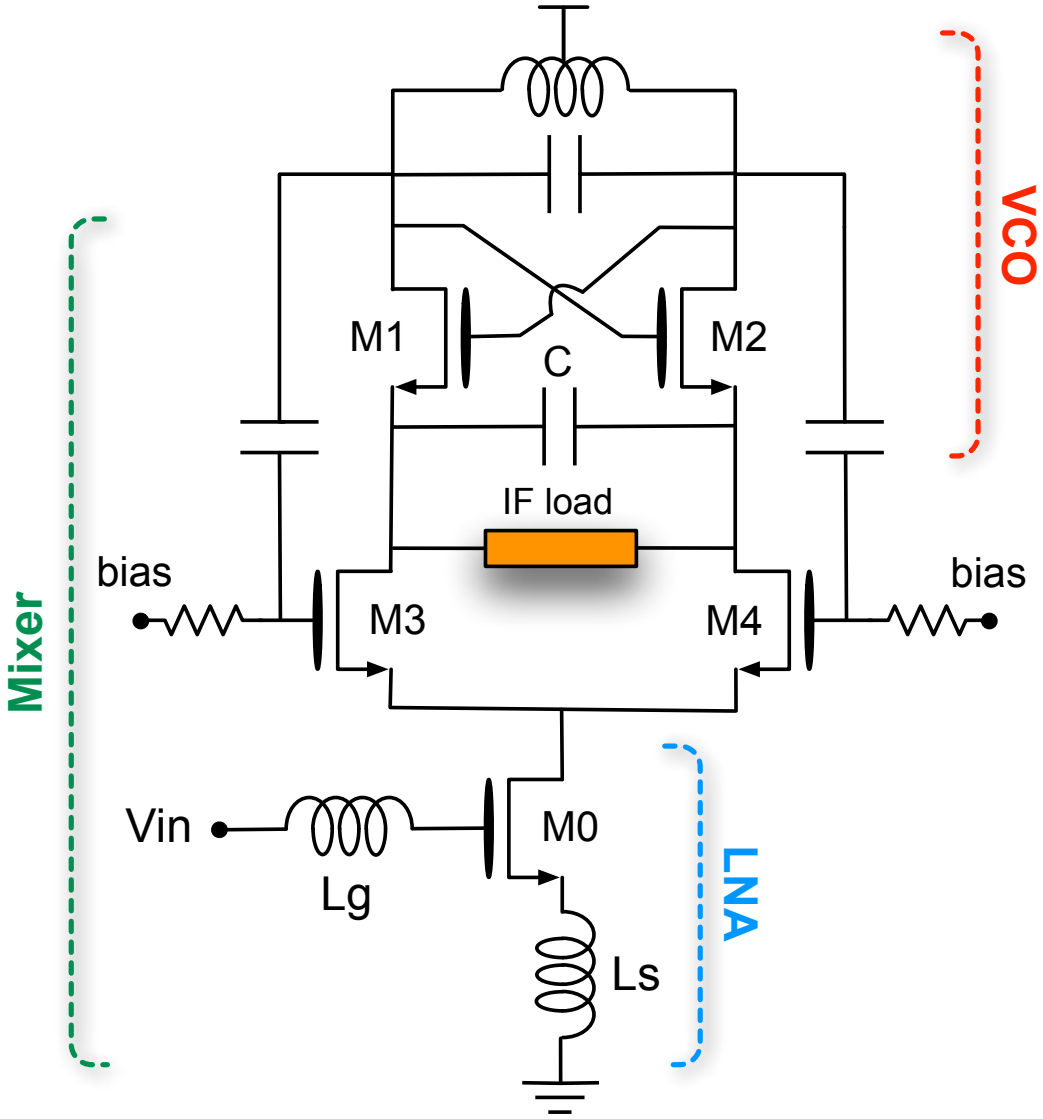


All RF signal current is down converted leading to an ideal gain equal to:

$$\frac{Iout}{Vin} = \frac{2}{\pi} gm_0$$

(Semi-period with M1 and M4 on)

LNA-Mixer-VCO (LMV) cell



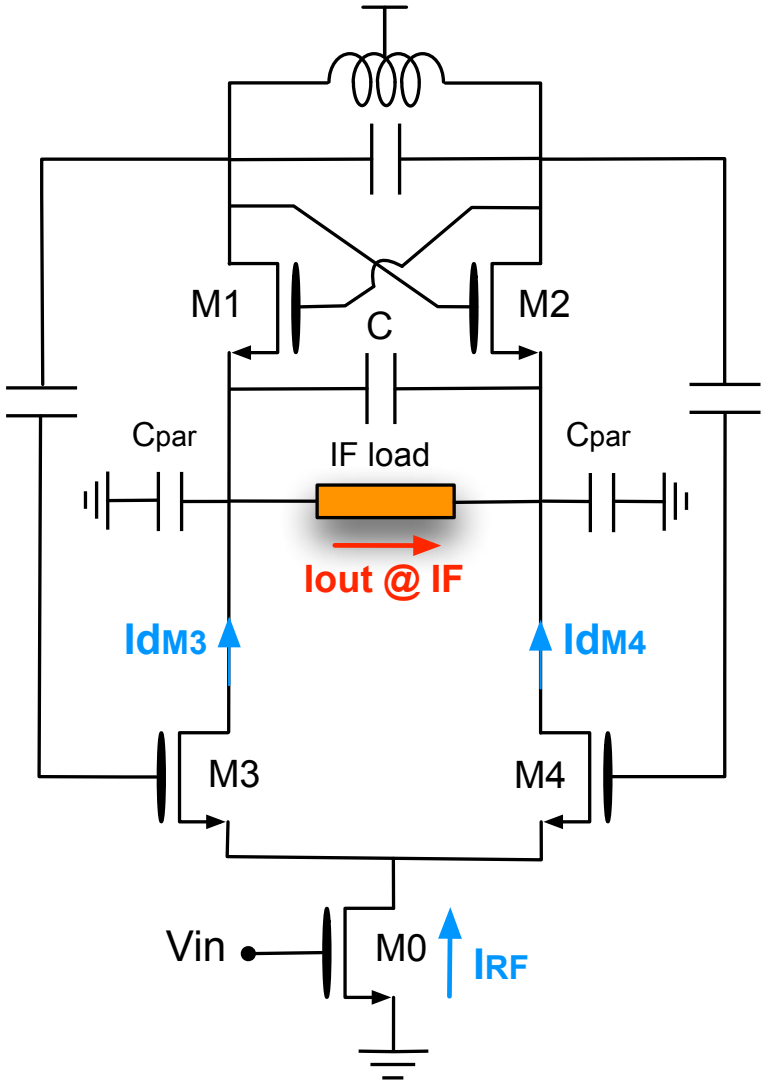
LNA, Mixer and VCO share bias and devices:

1) LNA is implemented re-using M0 in a inductive degenerated topology.

2) Three transistor stacked but minimum V_{DD} is 1 V_{TH} plus 3 V_{OV}

3) Above the capacitance C the structure acts exactly as a classic LC oscillator

Conversion gain losses



The evaluation of the LMV cell conversion gain in presence of non-idealities in challenging:

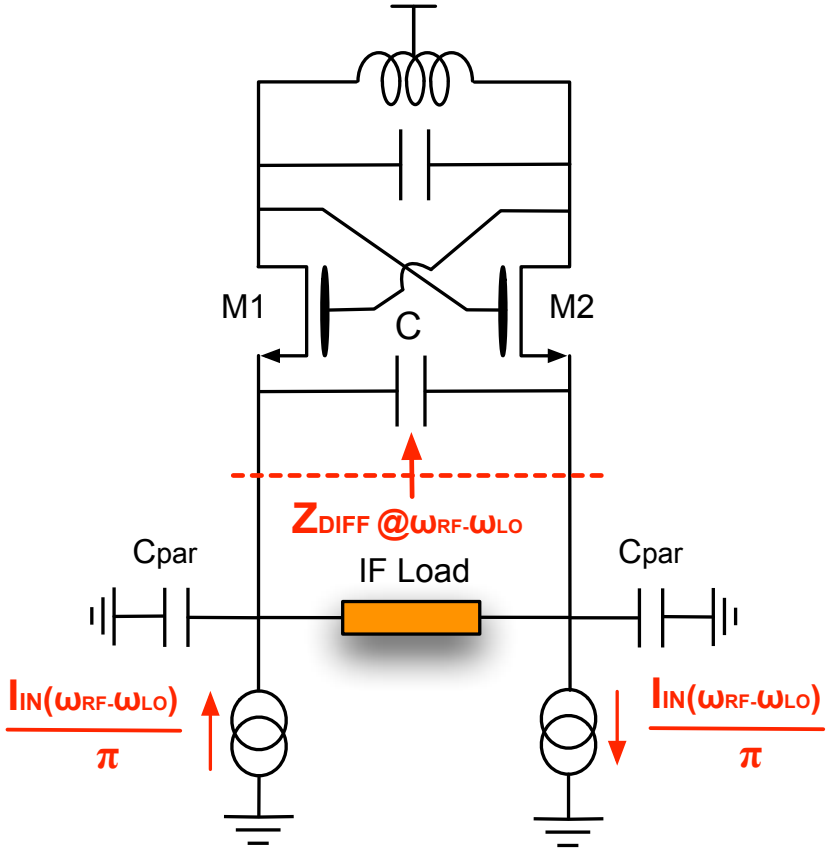
- Time-variant system
- Not separated RF and IF domains

Simplification:
Considering ideal M3-M4 mixing, it follows that

$$Id_{M3} = \frac{I_{RF}(\omega_{RF})}{2} + \frac{I_{RF}(\omega_{RF} - \omega_{LO})}{\pi} + \ldots$$

$$Id_{M4} = \frac{I_{RF}(\omega_{RF})}{2} - \frac{I_{RF}(\omega_{RF} - \omega_{LO})}{\pi} + \ldots$$

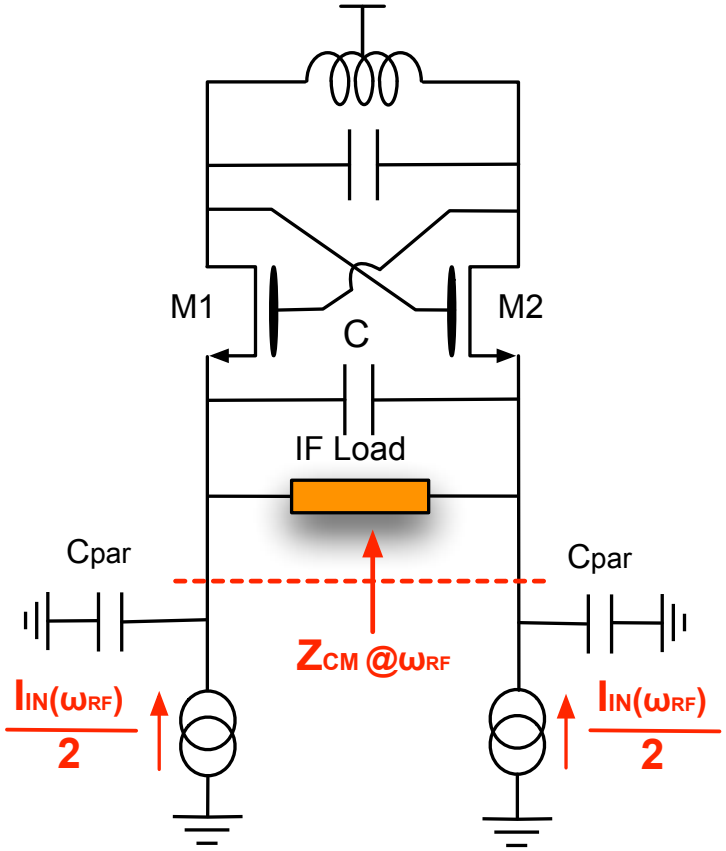
Conversion gain non-idealities



M3-M4 down-conversion

Losses from current partition at IF between **IF load** and $\mathbf{Z_{DIFF}}$

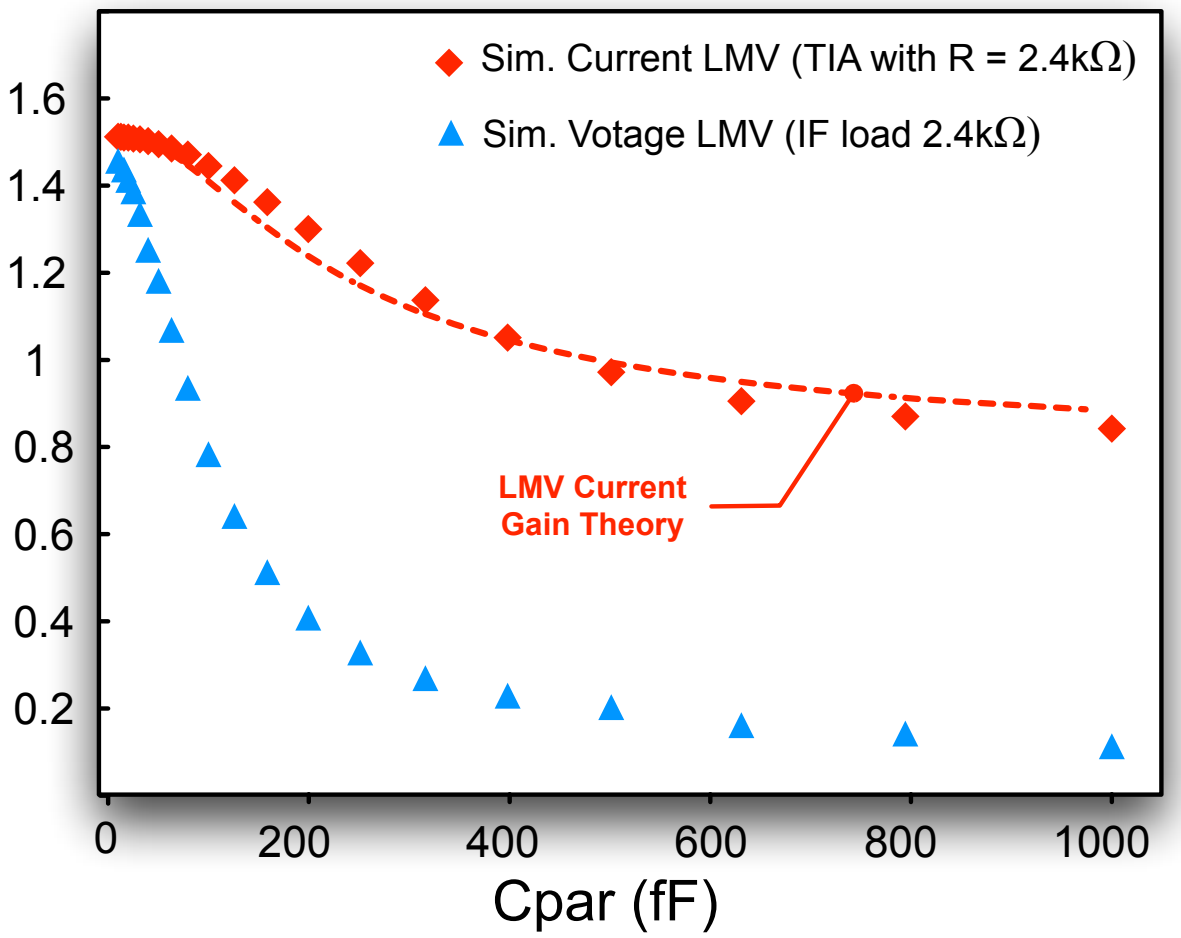
+



M1-M2 down-conversion

Losses from current partition at RF between **Cpar** and $\mathbf{Z_{CM}}$

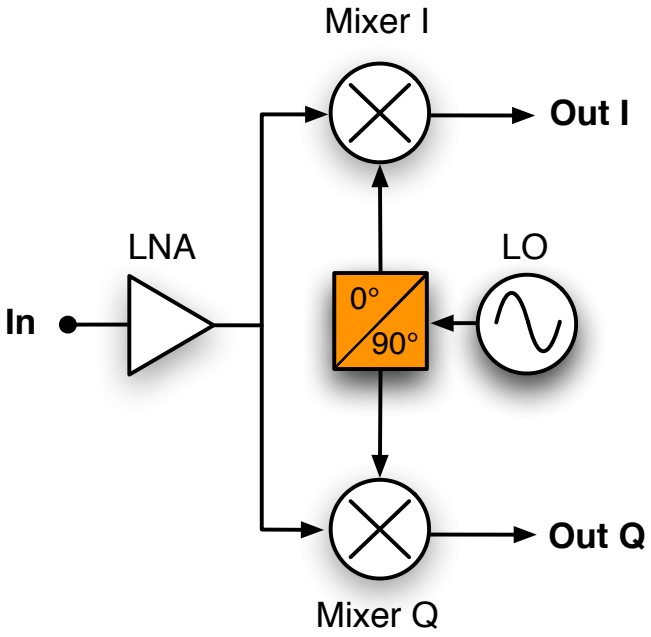
Conversion gain non-idealities (cont.)



Using a current approach eliminates IF losses due to the partition between IF load and others IF impedances

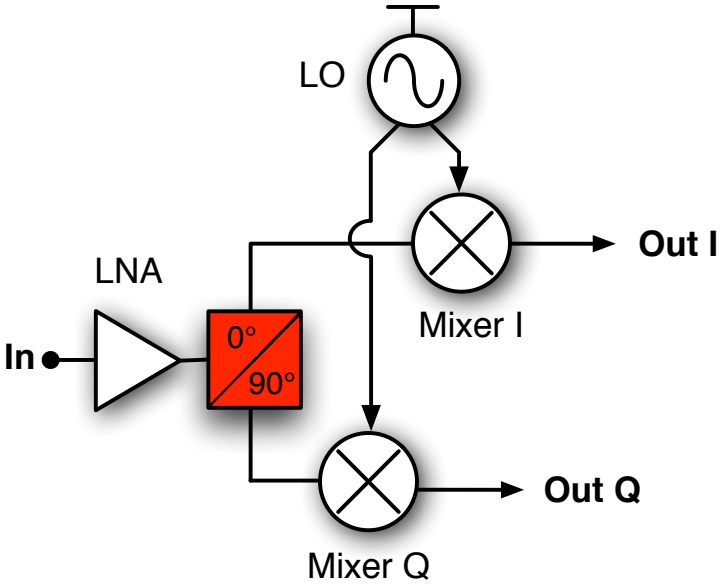
Quadrature Receivers

Quadrature on LO path



- Good quadrature accuracy
- Several architectures available *(Quadrature VCOs, Dividers…)*

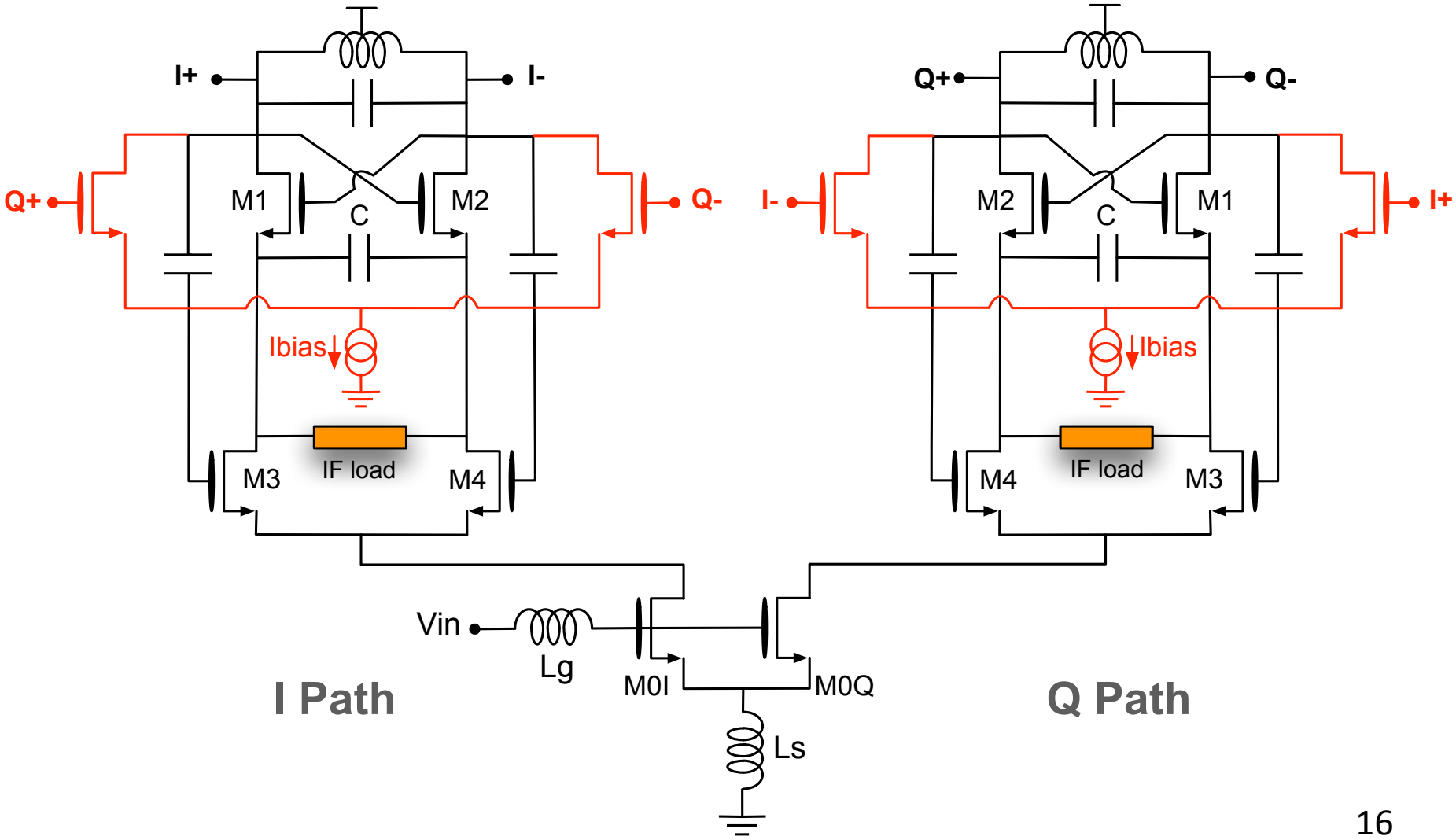
Quadrature on RF path



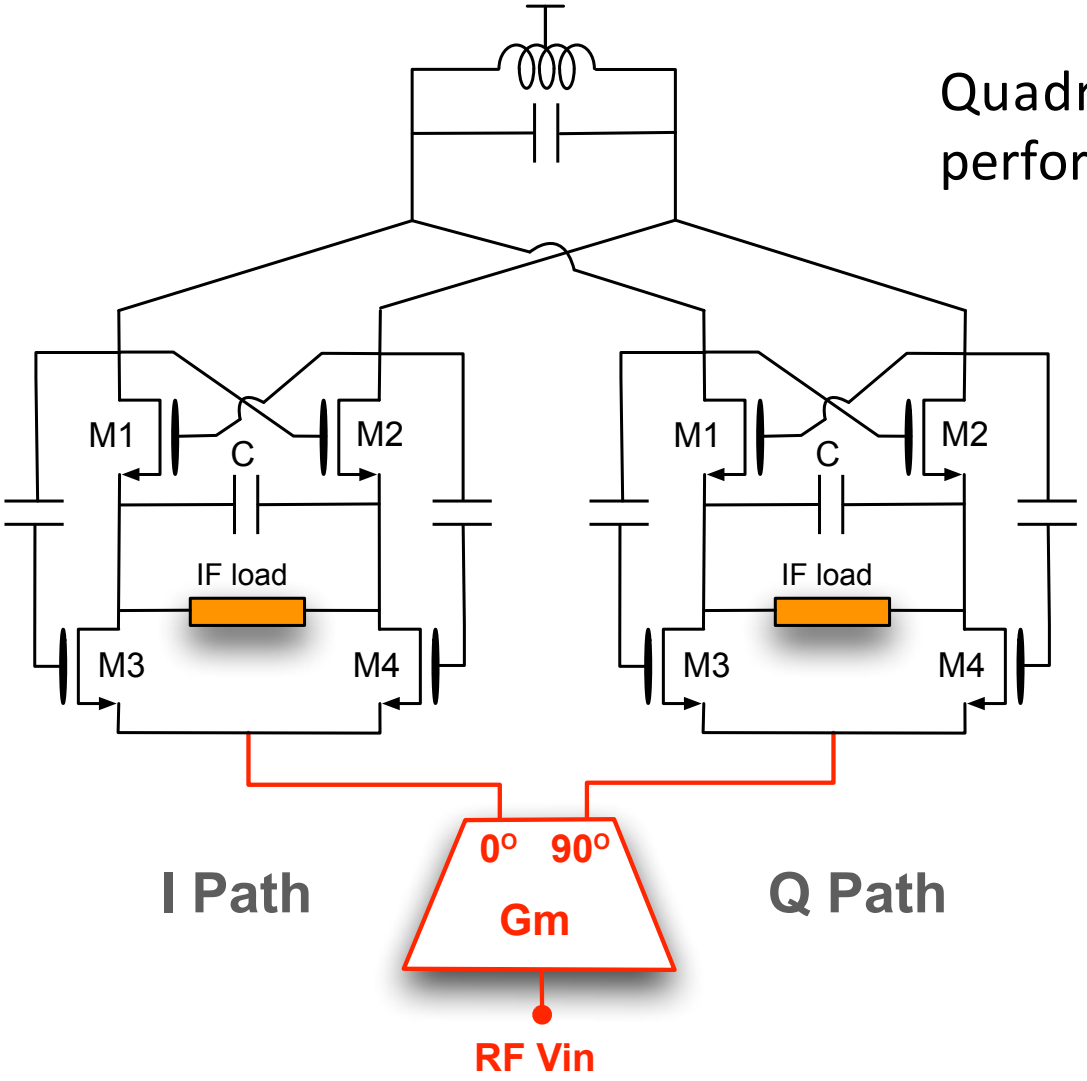
- Only two phase for LO signal
- Losses on RF path

Quadrature generation on oscillator

Two LMV cell can be cross-coupled realizing a quadrature RF front-end



Quadrature generation on signal path



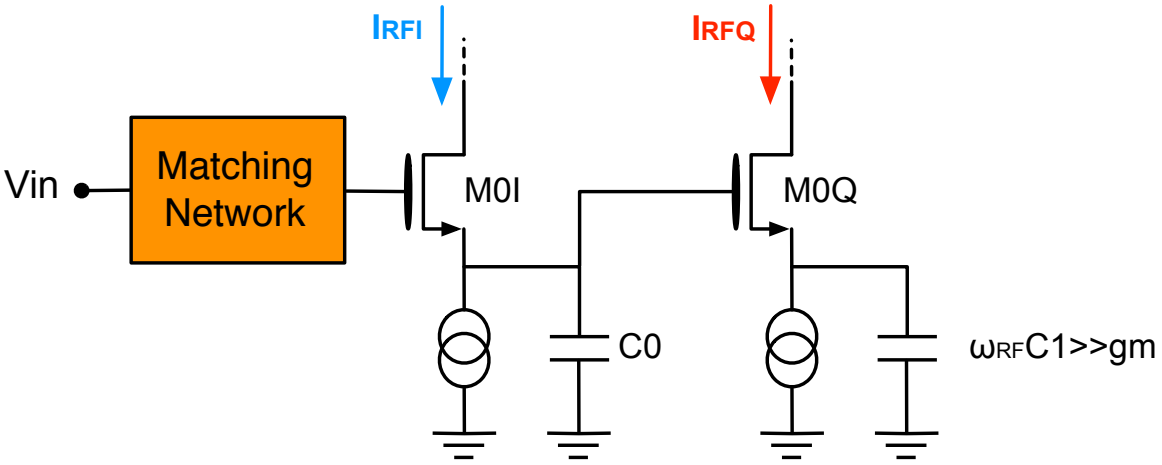
Quadrature generation can be performed also on RF signal path:

- Noise penalty
- Modest accuracy

but …

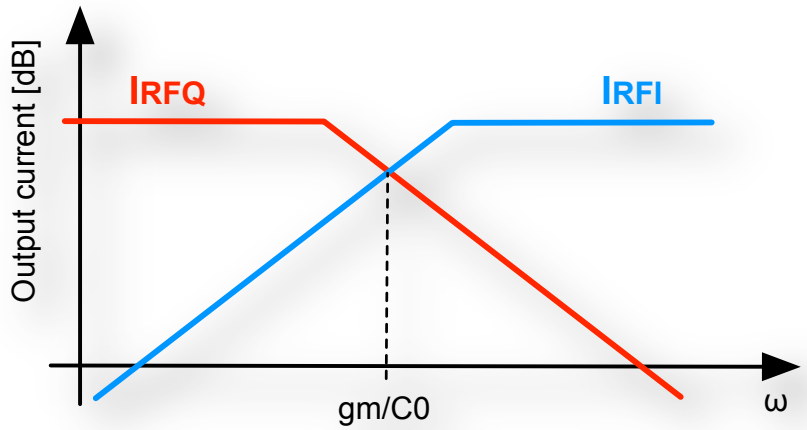
- **Less area (1 inductor)**
- **Less power required to sustain the oscillation**

Quadrature generation at RF



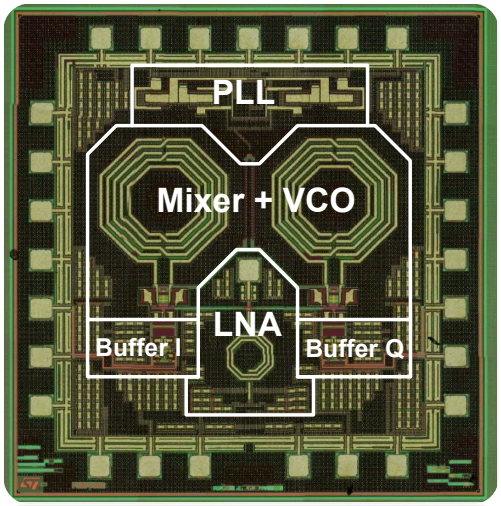
$$I_{RFI} = \frac{j\omega C_0}{1 + j\omega C_0 / gm} V_{in}$$

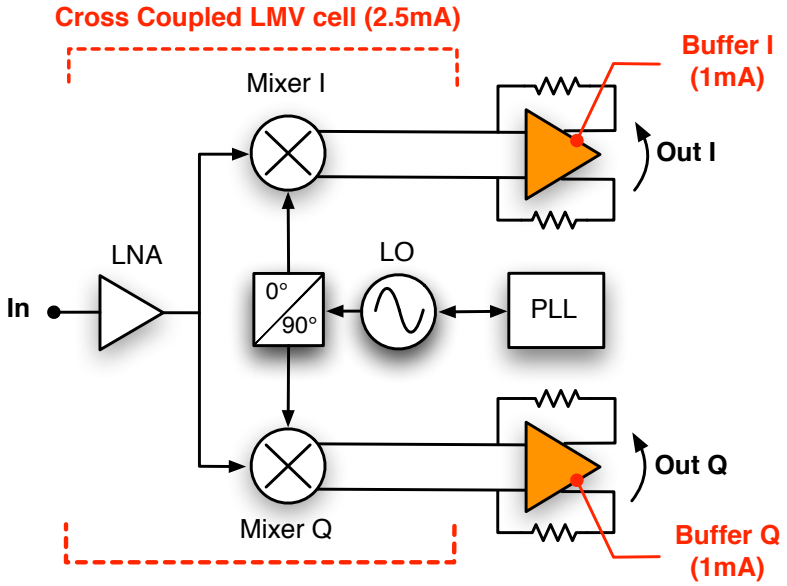
$$I_{RFQ} = \frac{gm}{j\omega C_0} I_{RFI}$$



- Signal quadrature guaranteed on a wide range
- Amplitude matching obtained only closed to gm/C0

Integrated prototype I





Application: GPS Receiver

Design: 0.13um CMOS (Vdd = 1.2V) / Active area = 1.5mm^2

Power diss. : **5.6mW (LMV cell + Buffers)** + 4.6mW PLL core

Gain: 36dB (IF @ 4MHz – BW 2MHz)

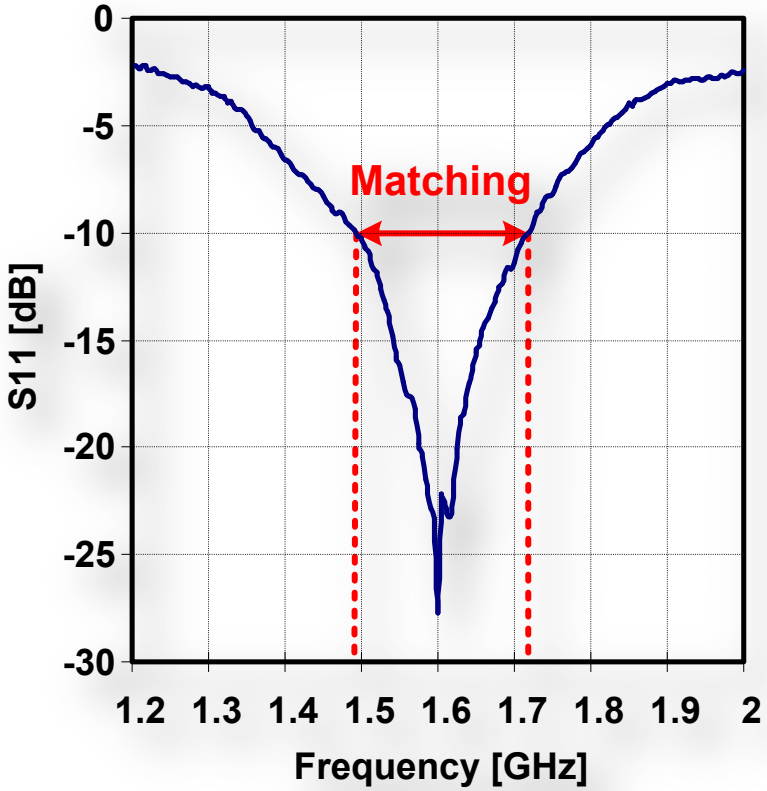
Noise Figure: **4.8dB (integrated in band)**

Linearity: IIP3 = -19dBm / 1dBCp = -31dBm

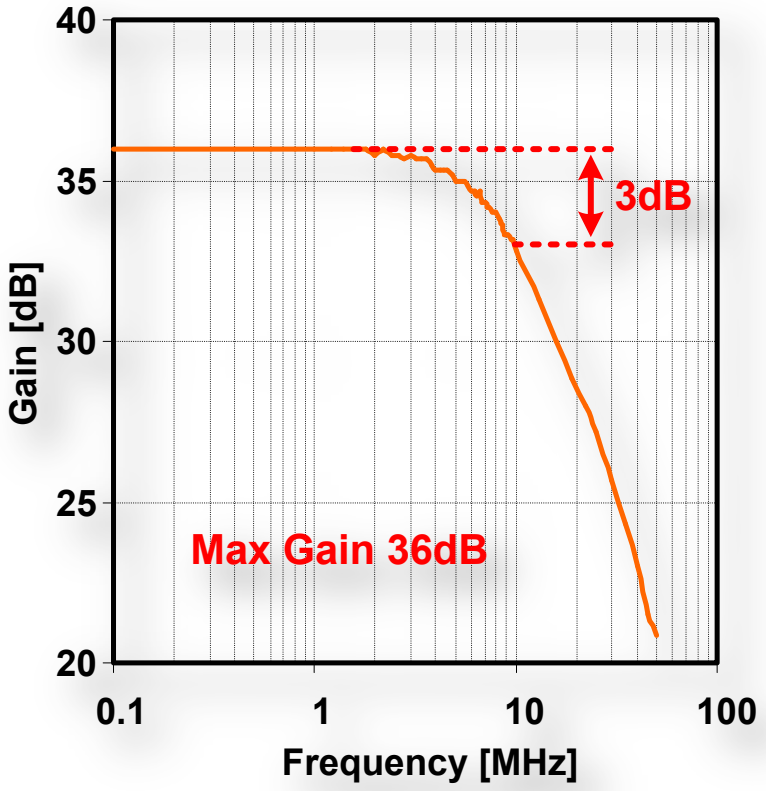
Oscillator: Phase Noise = -104dBc/Hz @1MHz / LO leakage = -55dBm

Measurements: Matching and Gain

Input Matching

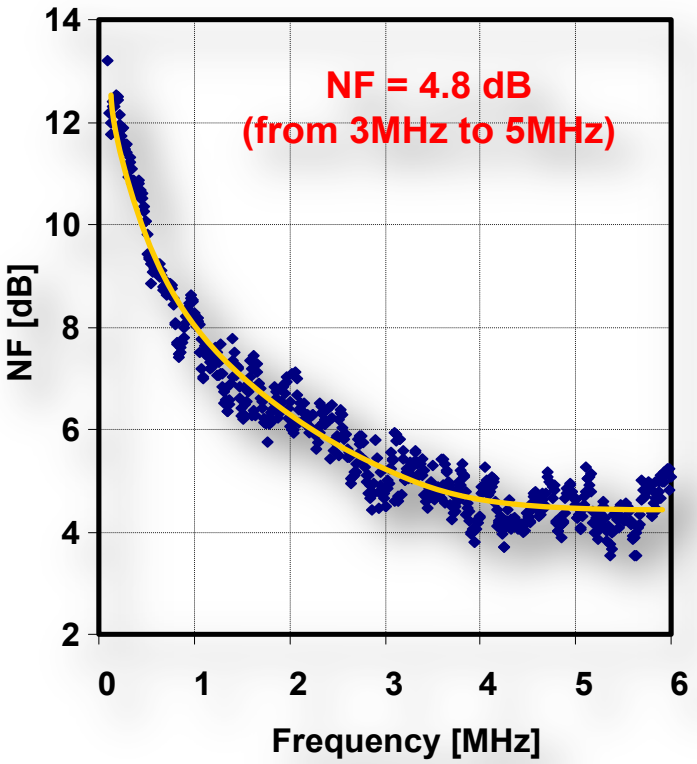


Output Gain

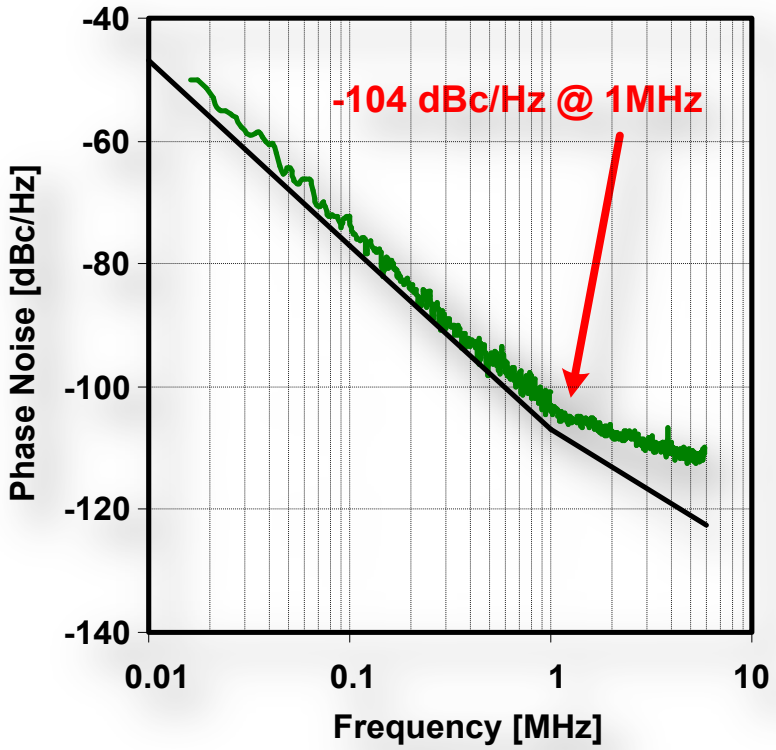


Measurements: Noise and Phase Noise

Noise Figure



Phase Noise



Comparison with the state of the art

	[1]	[2]	[3]	This Work
Gain	(25)+60 dB	(50)+80 dB	(33)+60 dB	36dB
NF	4dB	4dB	8.5dB	4.8dB
IIP3	n.a.	-15dBm	n.a.	-19dBm
1dB Comp. Point	-28dBm	n.a.	n.a.	-31dBm
PN @ 1MHz	-95dBc/Hz	-107dBc/Hz	-109dBc/Hz	-104dBc/Hz
LO leak. at input	-66dBm	n.a.	n.a.	-55dBm
Total Power	**35mW**	**27mW**	**19 mW**	**11mW***

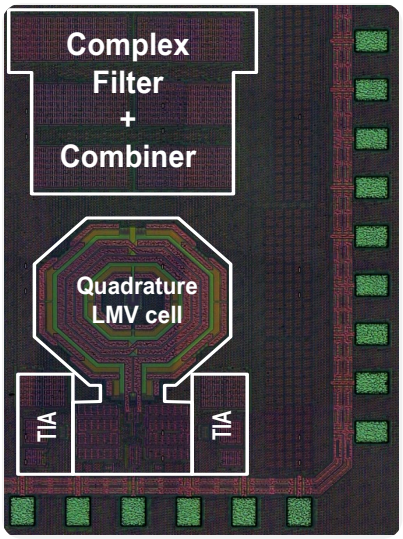
[1] G. Montagna *et al.* JSSC, July 2003 (CMOS 018 mm)

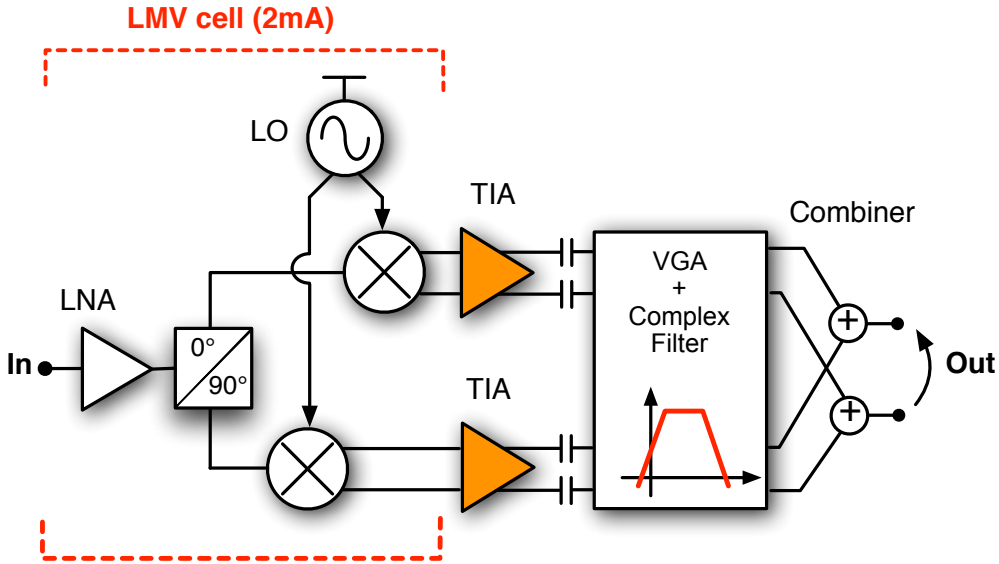
[2] F. Behbahani *et al.* JSSC, Dec. 2002 (CMOS 0.35 mm)

[3] J. Ko *et al*. JSSC, July 2005 (CMOS 0.18 mm)

* Included PLL (4.6 mW)

Integrated prototype II





Application: ZigBee Receiver

Design: 90nm CMOS (1.2V) / Active area = **0.35mm²**

Power diss. : 2.4mW (LMV cell + Buffers) + 1.2mW (TIA +filter)

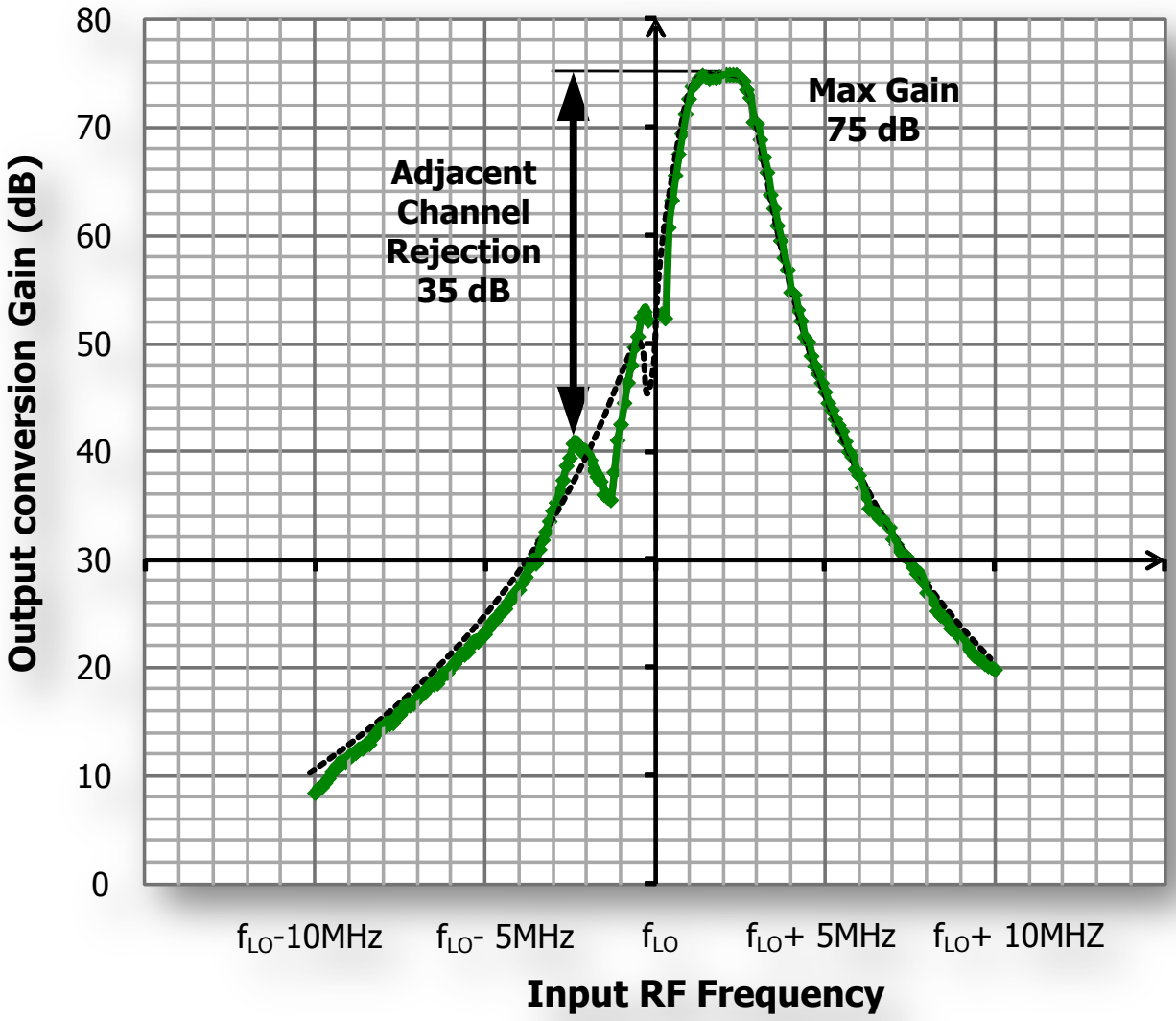
Gain: : In-band = 75dB / Image rejection = 35dB

Noise Figure: 9dB

Linearity: IIP3 -12.5dBm / 1dBCp -31dBm

Oscillator: Phase Noise -102dBc/Hz @3.5MHz

Measurements : IF Gain Profile



Comparison with the state of the art

	[1]	[2]	This work
NF (dB)	24.7	5.7	9
Sensitivity (dBm)	-82	-101	-94.7
IIP3(dBm)	-4,5	-16	-12,5
SFDR (dB)	50.3	55.3	53.5
Image Rejection (dB)	---	36	35
PN(3.5MHz) (dBc/Hz)	--	--	-107.8
Vdd (V)	1.8	1.8	1.2
Power dissipation (mW)	15	17	3.6
Number of inductors	6	4	1
Area (mm2)	2,1	0,8	0.35
Technology	0.18	0.18	0.09

[1] *P. Choi, et al.,* JSSC, Dec 2003 (802.15.4)
[2] W. *Kluge, et al.,*JSSC, Dec. 2006 (ZigBee)

LMV cell main features

- Matching, RF amplification, mixing, oscillator and quadrature generations share the same bias current
- Good trade-off between performance and power consumption suitable for ultra low-power applications (e.g. WSN, ZigBee GSS)

- Main References:

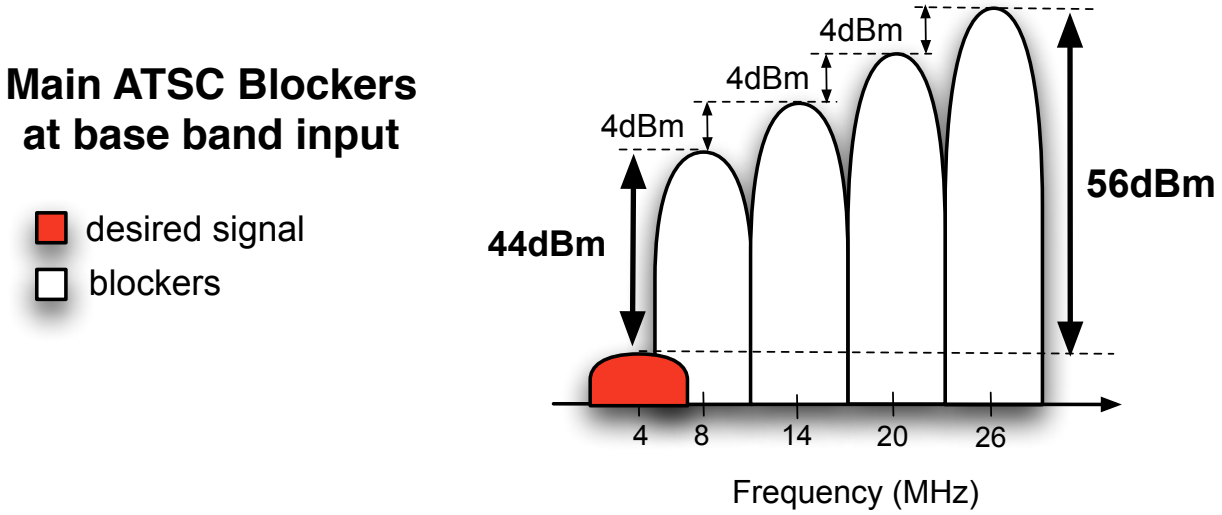
Liscidini, A.; Mazzanti, A.; Tonietto, R.; Vandi, L.; Andreani, P.; Castello, R.; , "Single-Stage Low-Power Quadrature RF Receiver Front-End: The LMV Cell," *Solid-State Circuits, IEEE Journal of* , vol.41, no.12, pp.2832-2841, Dec. 2006

Tedeschi, M.; Liscidini, A.; Castello, R.; , "Low-Power Quadrature Receivers for ZigBee (IEEE 802.15.4) Applications," *Solid-State Circuits, IEEE Journal of* , vol.45, no.9, pp.1710-1719, Sept. 2010

Filtering ΣΔ ADC

Merging digital and analog domain in favor of a more flexible analog base-band

Example of input signal for analog base-band



In band **SNDR**: **75dB (12.2 ENOB)**

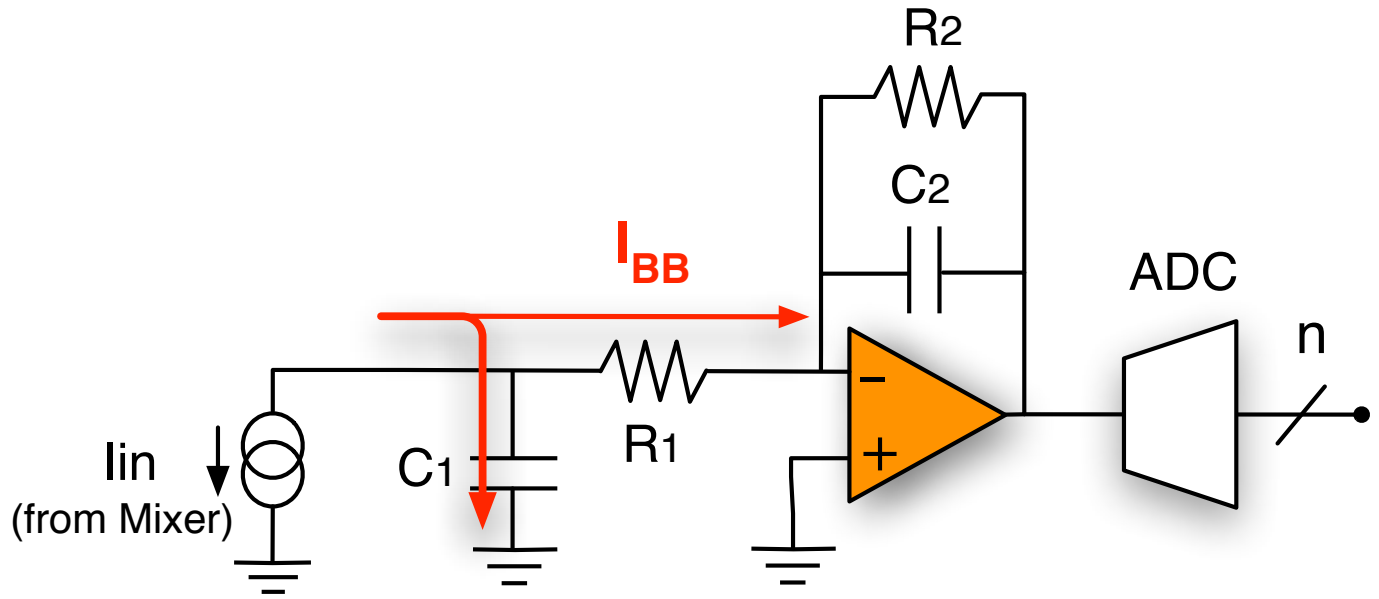
(18dB SNRmin + 12dB PAR + 44dB adjacent channel + 3dB Margin)

Out of band **SNDR**: **75dB** + **13dB** = **88dB (14.4 ENOB)**

Generally dynamic range specs are frequency dependent demanding an analog filtering before the ADC

Starting point

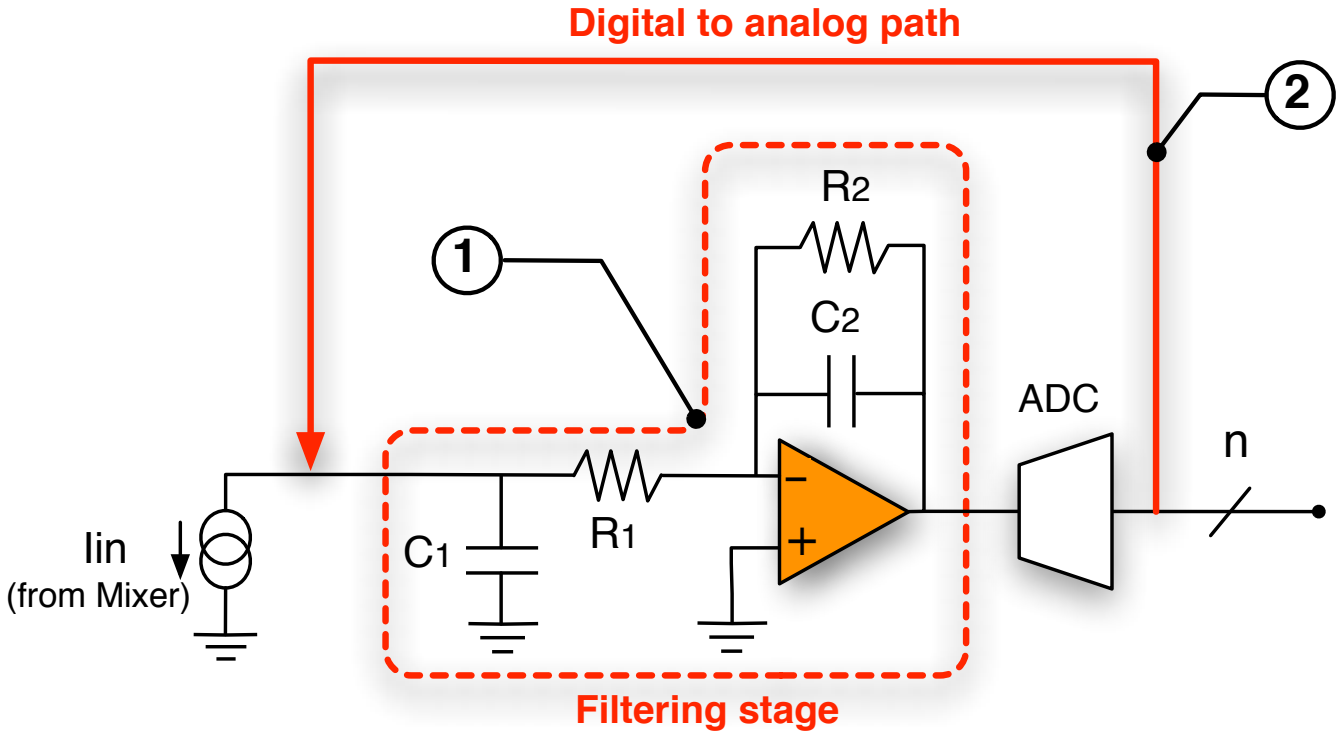
[ISSCC 2011: Cicalini et al, Ivin Siu-Chuang Lu et al]



Passive filtering of the largest out of band blockers at the beginning of the base-band analog section

Cascade of two-real-poles (selectivity reduced if in-band flatness is required)

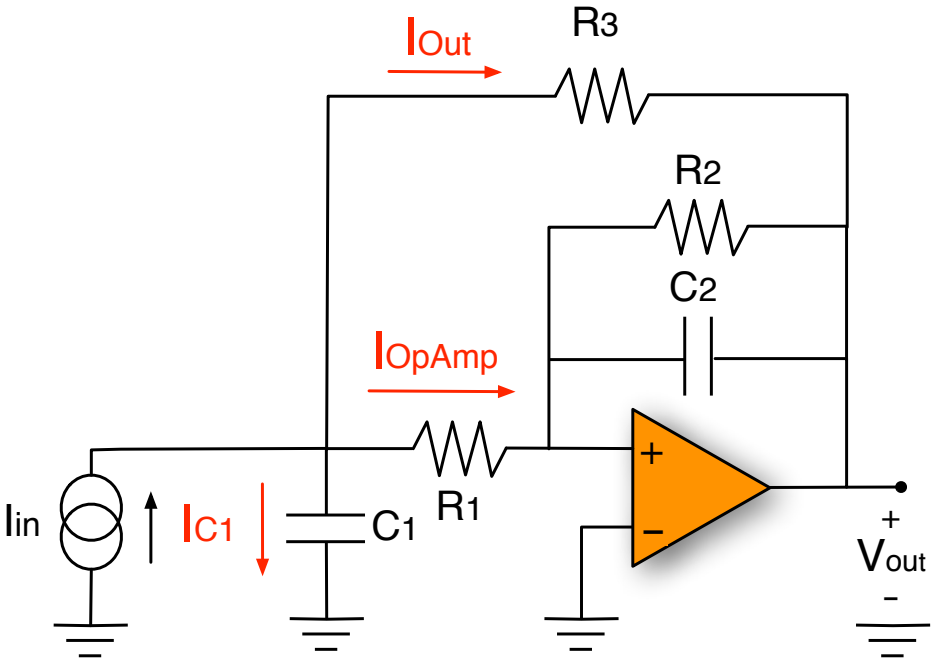
Two steps towards a filtering ADC

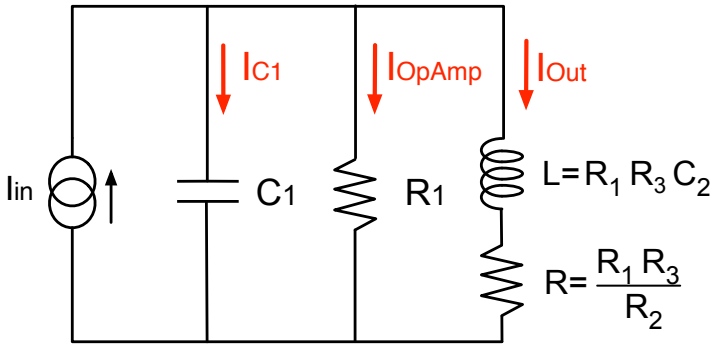


1) **Improving filtering stage selectivity** compared to a 2 real-poles cascade

2) **Including** the obtained **filter in a mixed analog/digital loop** for a filtering ADC as a complete analog base -band

1) Improving selectivity





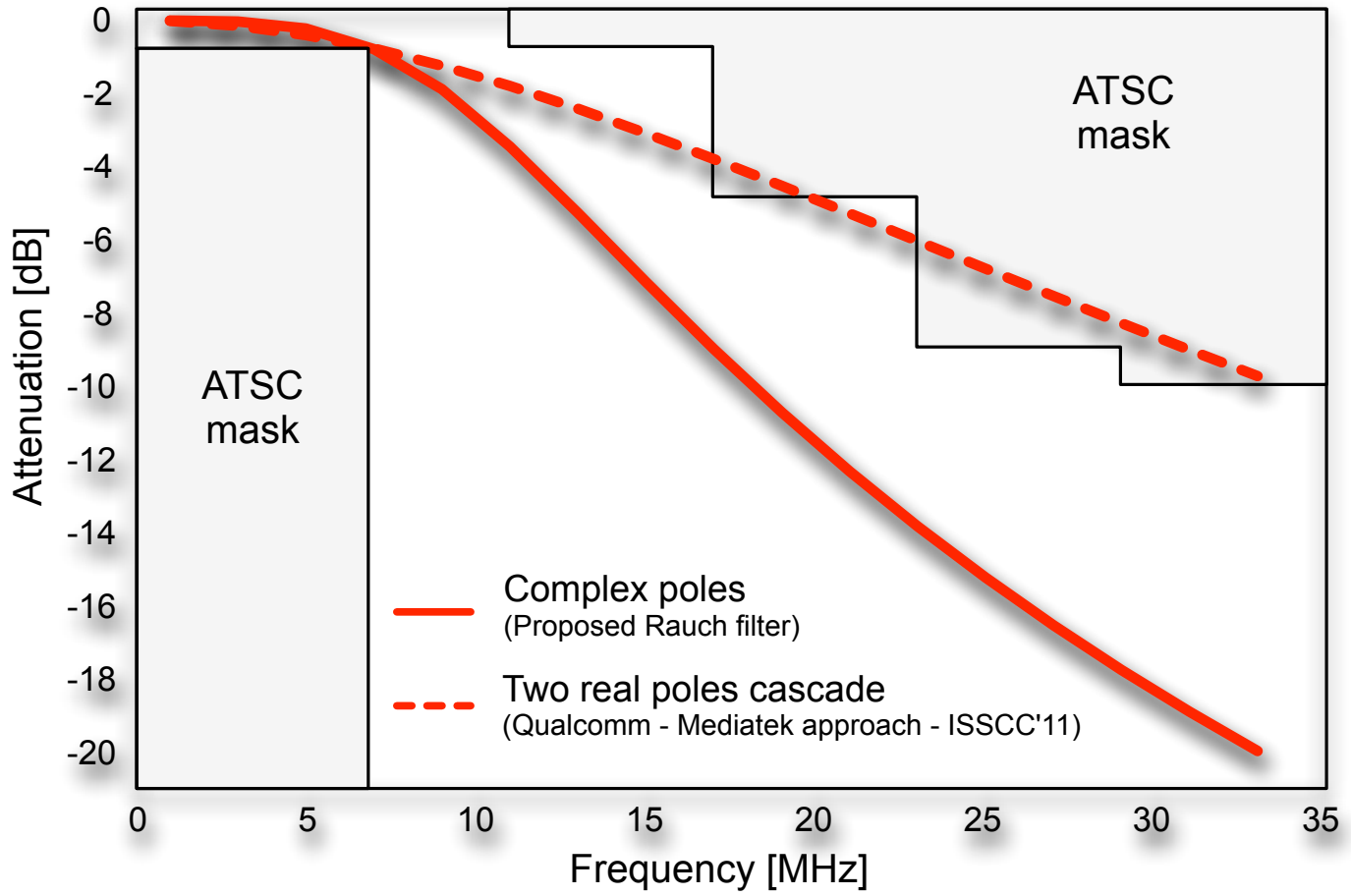
$$\omega_0 \cong \sqrt{\frac{1}{C_1 C_2 R_1 R_3}} \qquad Q \cong \omega_0 C_2 R_2$$

Two complex poles realized adding **resistor R3.**

The output can be sensed as a current flowing through the main feedback resistor (R3)

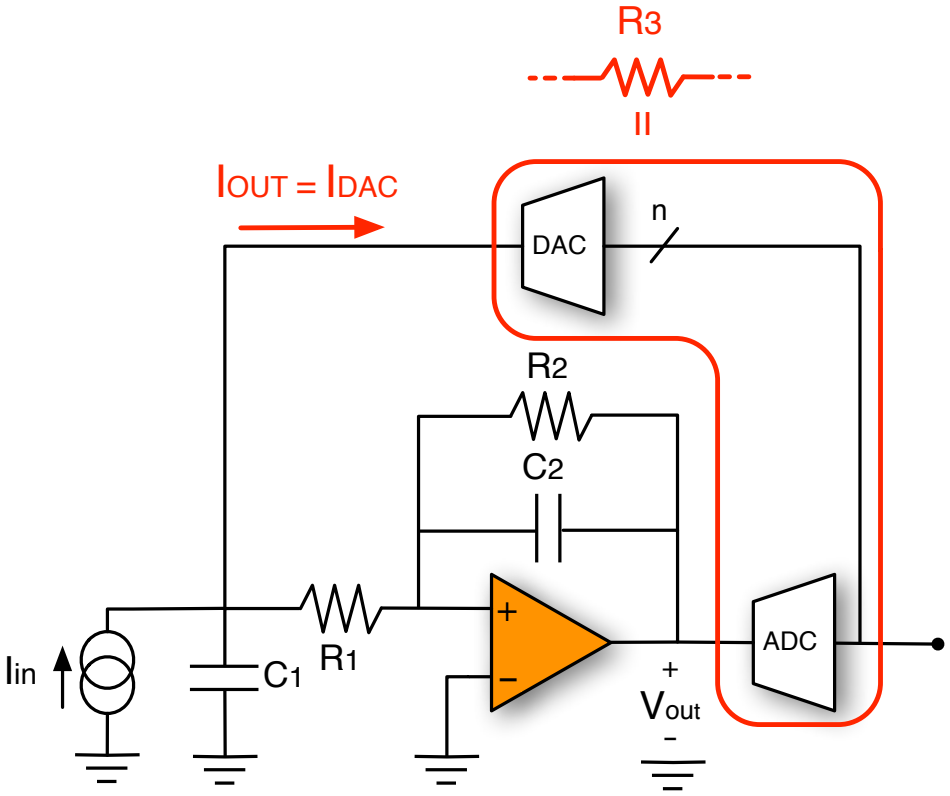
Input current is **passively filtered by C1** before entering the active devices

Filter selectivity vs. the state of the art



For a given mask the two complex poles offers a better filtering than the simple cascade of two real poles

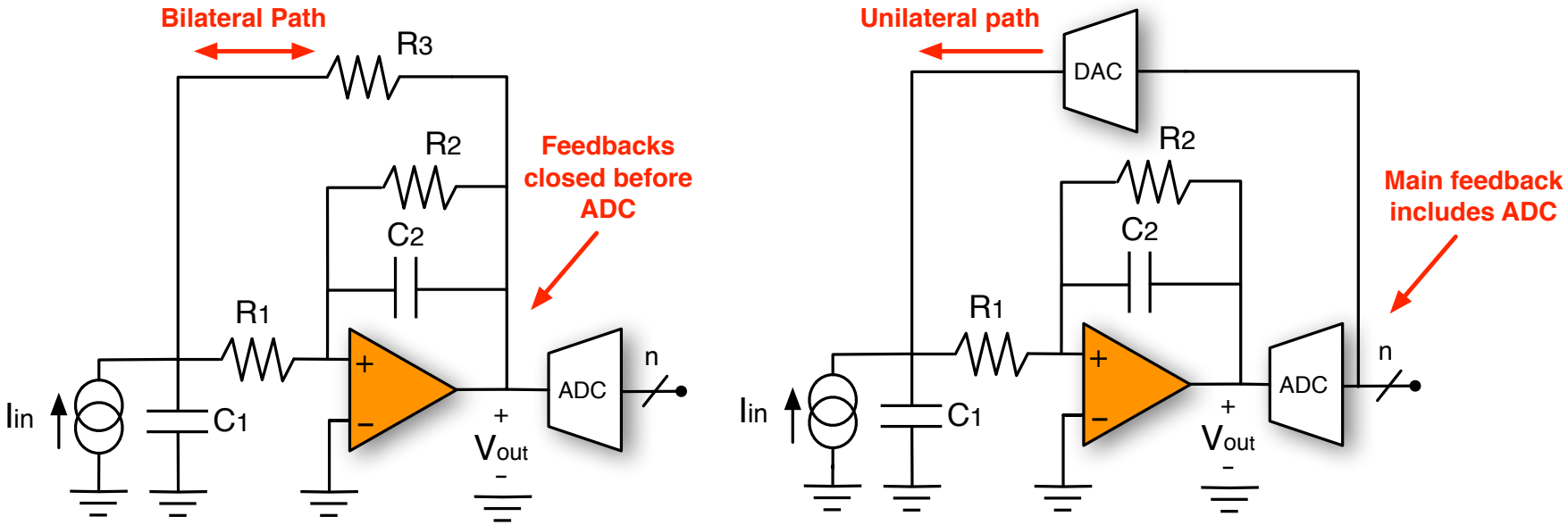
2) Embedding ADC in the filter



The ADC is embedded in the filter by **substituting R3 with an ADC-DAC cascade**

The dynamic range of the **DAC** is set by in-band signals, since it absorbed the **current filtered with a 2nd order profile**

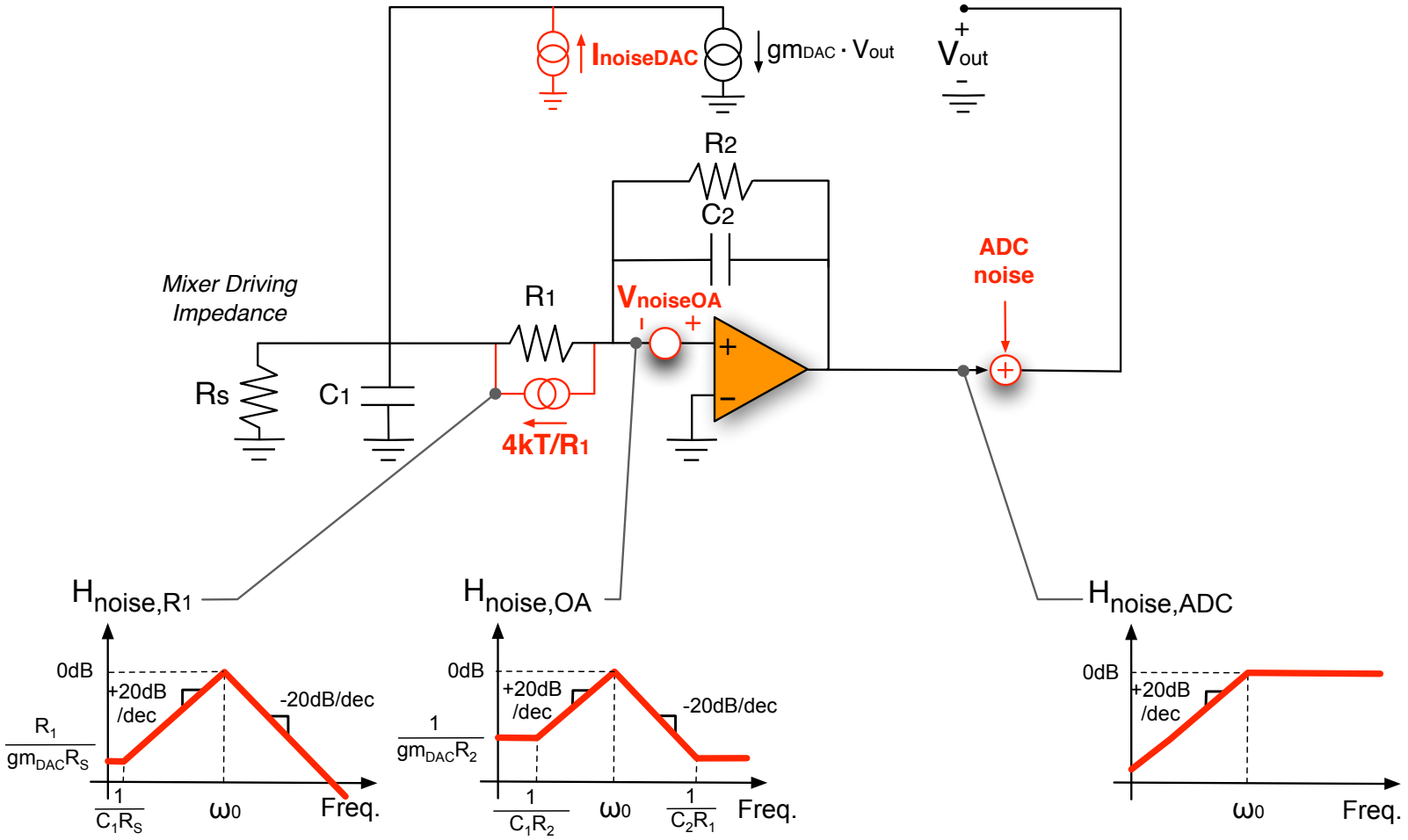
Filter-ADC cascade vs. Filtering ADC



1) **Absence of feed-forward path** in main loop reduces analog noise of filter (as in pipe filters)

2) ADC in **main feedback loop shapes** ADC analog and quantization **noise**

Analog noise



1) Absence of feed-forward path

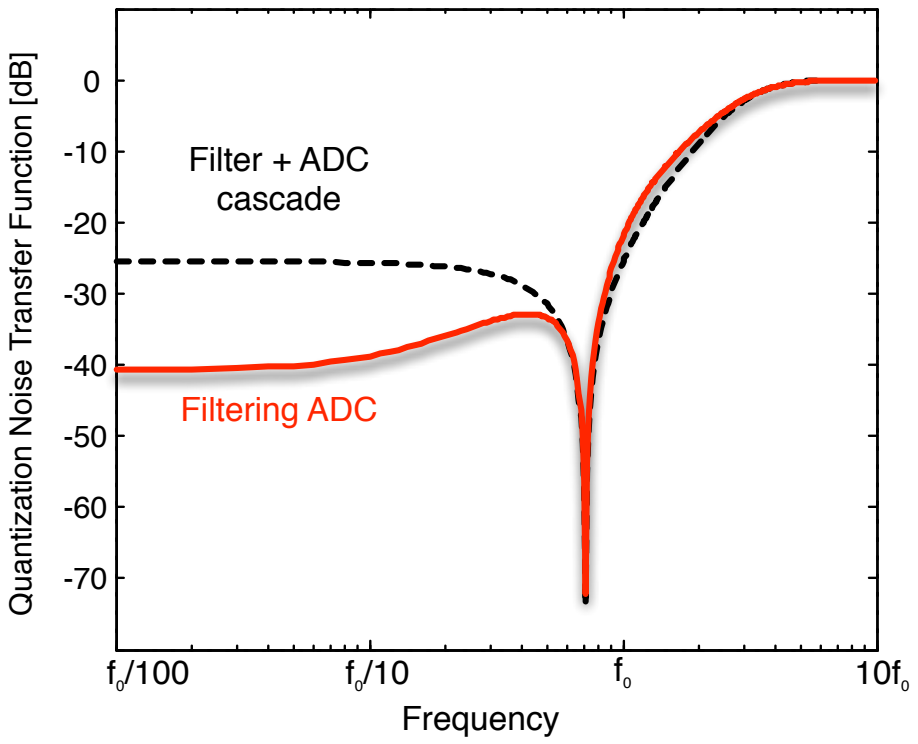
Filter noise reduction (1dB)

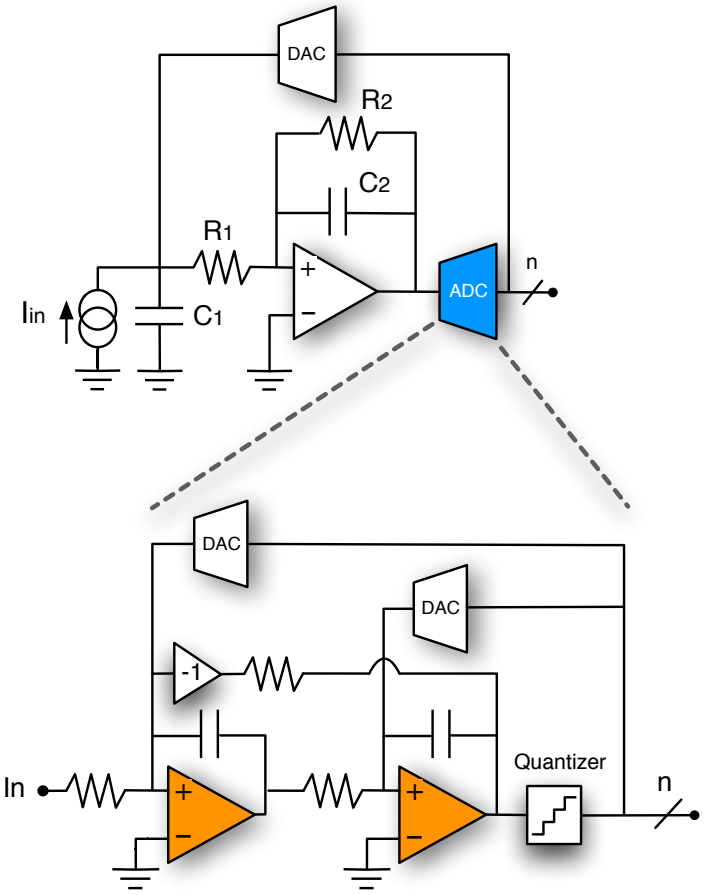
2) ADC in the main loop

ADC noise shaping (6.6dB)

Quantization noise

The quantization noise introduced depends on the architecture chosen for the ADC core

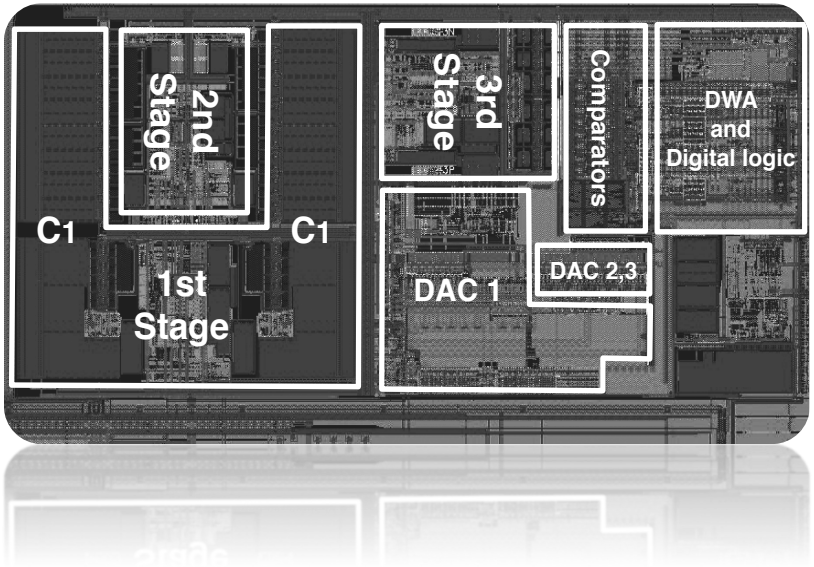


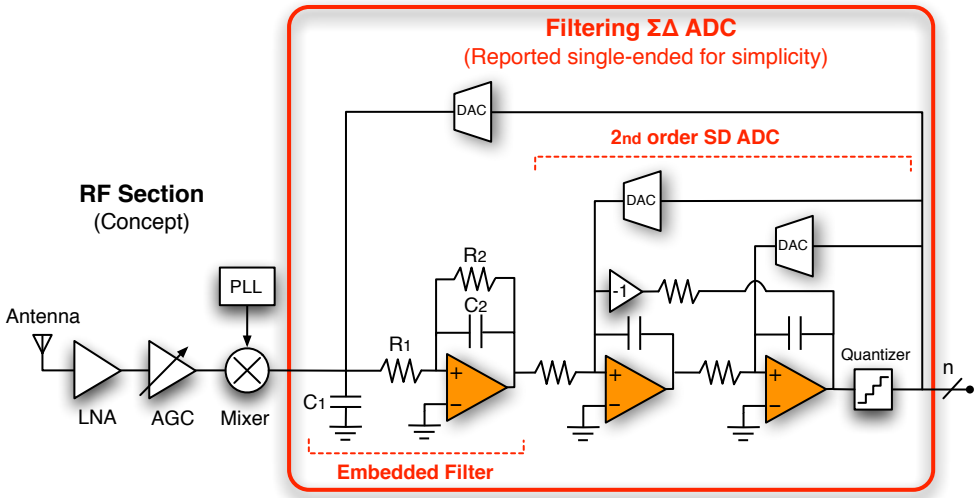


Noise shaping improvement depend on the band of integration:

14.5dB	8dB	2.5dB
(from 0 to $f_0/10$)	(from 0 to $f_0/2$)	(from 0 to f_0)

Integrated prototype





Application: DVB-T ATSC analog base-band

Design: 90nm CMOS (Vdd = 1.8V/1.2V) / Active area = 0.21mm^2

Power diss. : 54mW

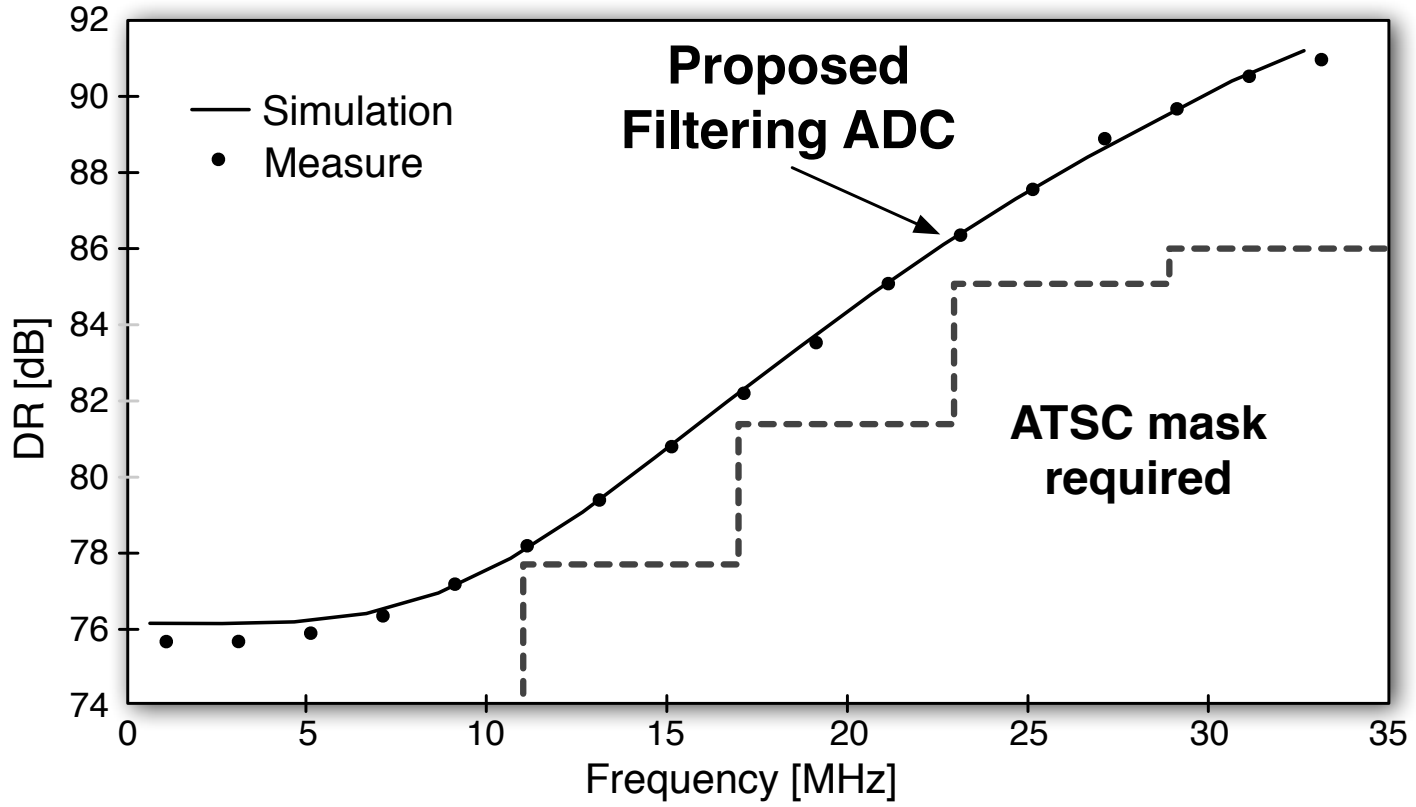
SNDR (freq. dependent): 74.6dB In-band / 80dB @15MHz / 89dB @30MHz

FoM (freq. dependent): 1.03pJ/c-stp In band / 0.2pJ/c-stp @30MHz

Channel bandwidth: 1MHz-7MHz (Filter band 10MHz)

Clock frequency: 405MHz (ΣΔ band 30MHz)

Measures



The **frequency dependent SNDR** optimizes performance to standard requirements

Comparison with the state of the art

	BW [MHz]	Fclock[MHz]	Power[mW]	SNDR [dB]	In-band FoM [pJ/step]	Out-of-band FoM [pJ/step]	Area [mm^2]	Technology
This	6*	405	54**	74.6	1.03	0.2	0.21	90nm
JSSC 04	1	64	2	59	1.37	0.7	0.14	0.18um
TCAS 09	6.5	96	122.4	70.9	3.28	-	2.15	0.18um
ISSCC 06	8.5	264	375	84	1.7	1.7	2.5	0.13um
ISSCC 08	10	640	100	82	0.49	0.49	0.7	0.18um
JSSC 06	20	640	20	74	0.12	0.12	1.2	0.13um
ISSCC 07	20	340	56	69	0.61	0.61	1.2	0.13um
JSSC 10	25	400	7	52	1.08	1.08	-	90nm
JSSC 10	10	950	40	72	0.61	0.61	0.42	0.13um
ISSCC 09	20	250	10.5	60	0.32	0.32	0.15	65nm

* 1MHz-7MHz (ATSC) in low-IF, reconfigurable to 5MHz,7MHz,8MHz

** From 1.8V analog and 1.2V digital supply

Filtering ADC main features

- Filtering ADC with frequency dependent dynamic range. Noise reduction compared to filter-ADC cascade

- Frequency shaped dynamic range is suitable for the replacement of the entire analog based of a wireless receiver with a filter ADC

- Main References:

Sosio, M.; Liscidini, A.; Castello, R.; De Bernardinis, F.; , "A complete DVB-T/ATSC tuner analog base-band implemented with a single filtering ADC," *ESSCIRC (ESSCIRC), 2011 Proceedings of the* , vol., no., pp.391-394, 12-16 Sept. 2011

Sosio, M.; Liscidini, A.; Castello, R.; , "A 2G/3G Cellular Analog Baseband Based on a Filtering ADC," accepted on *Circuits and Systems II: Express Briefs, IEEE Transactions on*

Adapt

Reconfiguring performance as function of the operative conditions

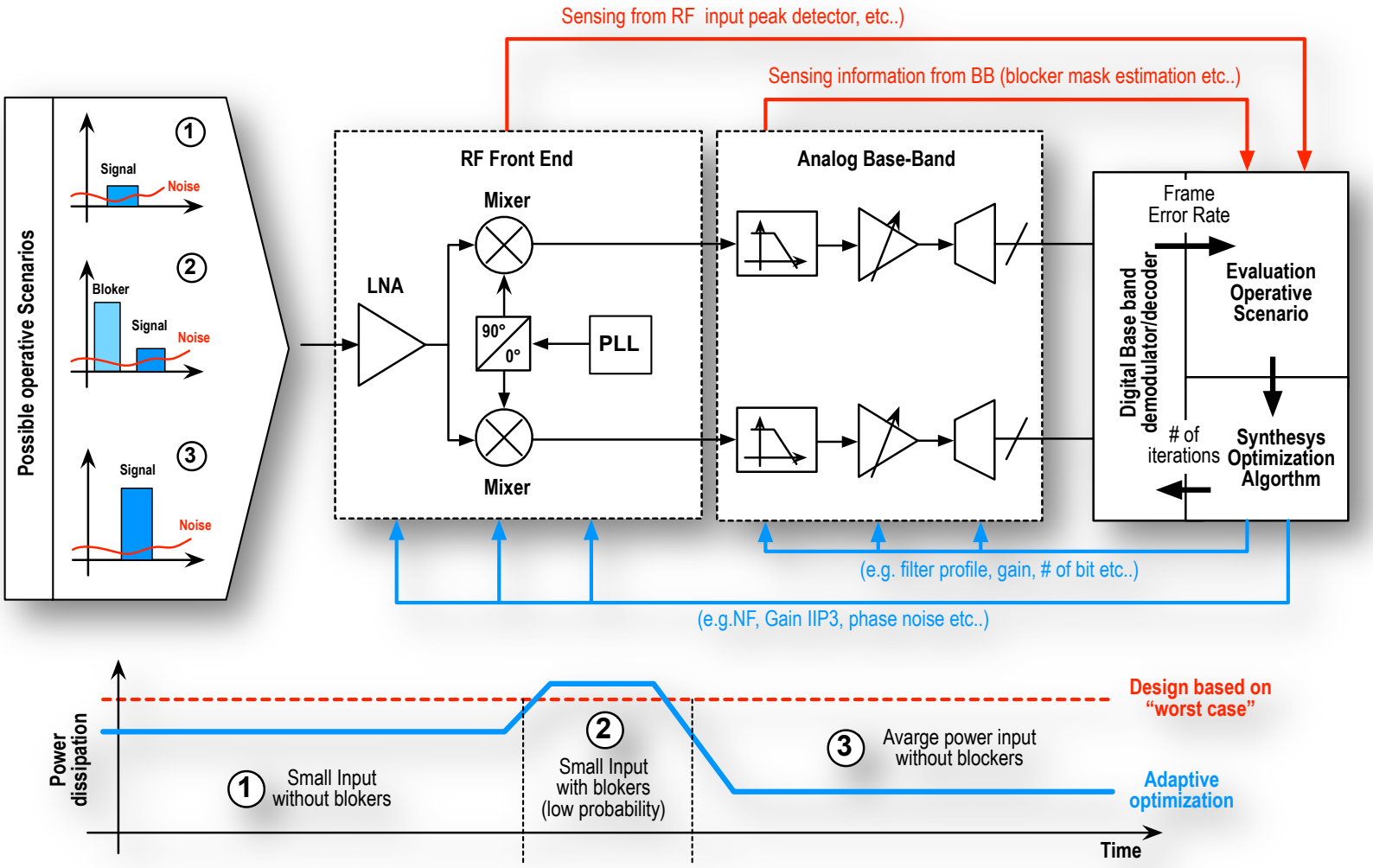
Adaptive Receiver – Basic Idea

Existing adaptive transmission techniques target the best use of available communication resources
(maximization of data rates).

Our **adaptive transceiver idea** corresponds to configure the system for **minimum energy consumption** having as a target the Quality of Service (QoS) level required to satisfy the user demand.

Adapting receiver within the operative scenario for a minimum power consumption

Adaptive receiver scheme



Optimize the **average** power consumption!

Analog and Digital Requirements

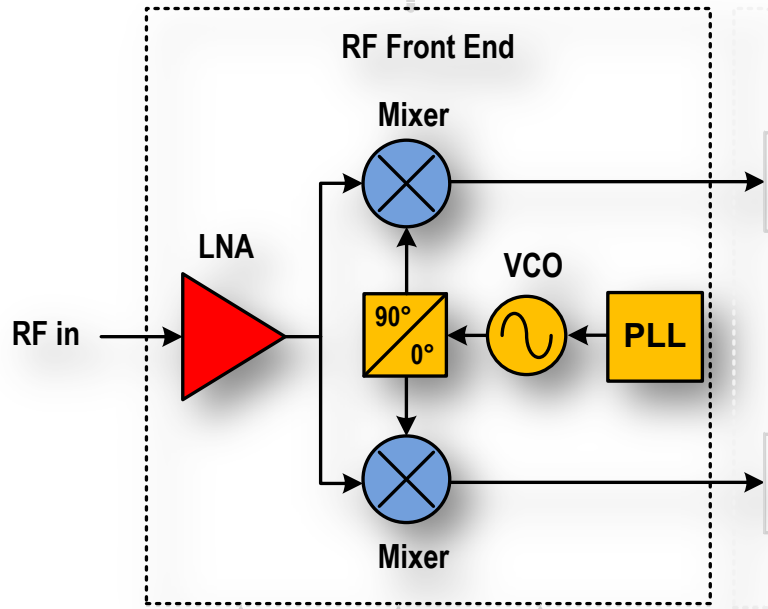
Analog Section

- Performance Configurability
- Local loop to prevent block saturation
- Partial "digital" **detection** of the **operative scenario**

Digital Section

- Performance Configurability
- Identify the operative scenario
- **Optimization algorithm** based on a RX model
- **Control loops** closed around analog building block

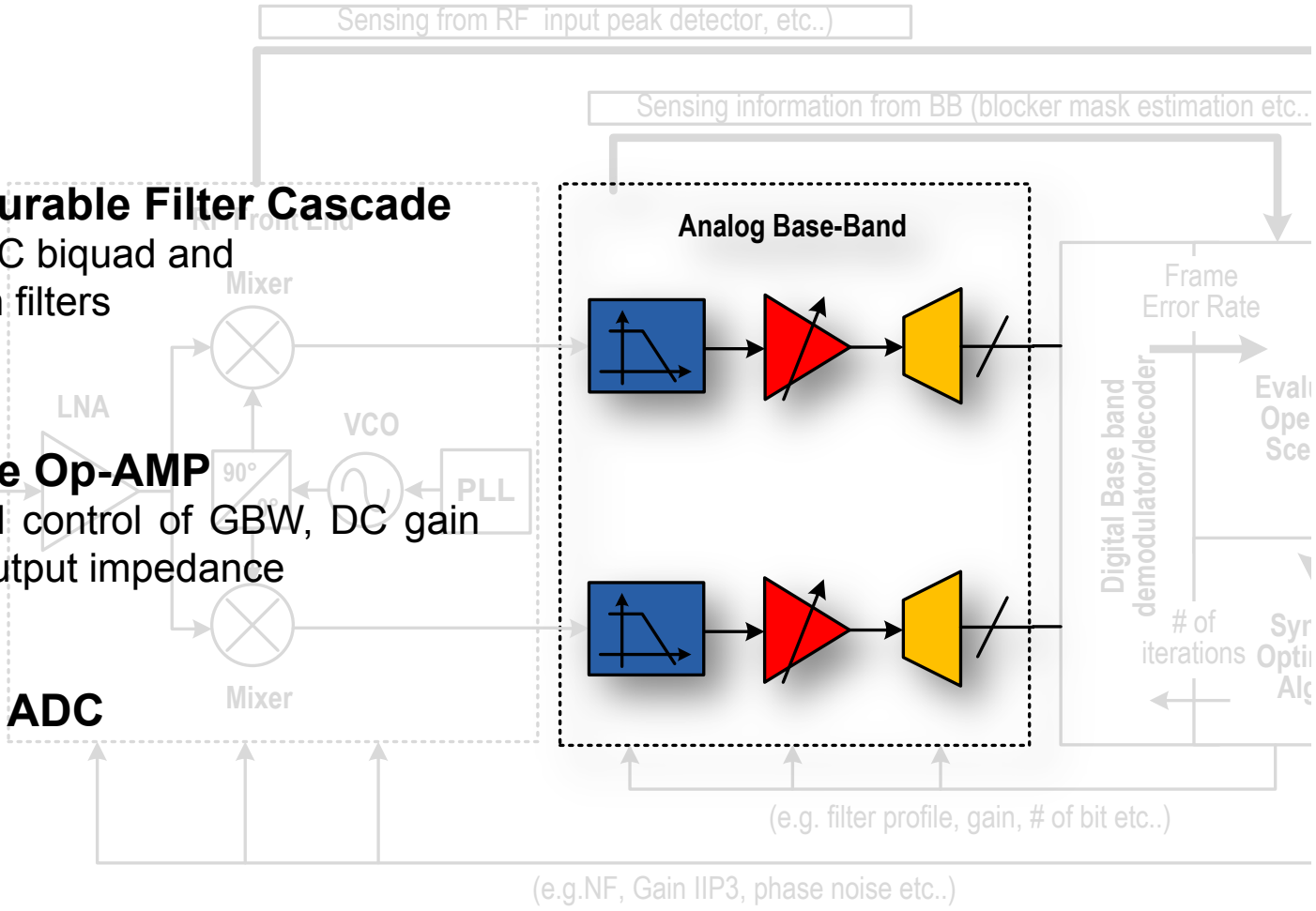
Adaptive RF Front-End



- **Multi Feedback Common Gate LNA**
  - High level of configurability
  - Independent controls for NF, Gain and linearity
- **Passive Mixers**
  - Performance controlled acting on IF virtual ground
- **All Digital PLL**
  - High level of flexibility
  - Easy interface with digital optimization

Adaptive IF Analog Front-End

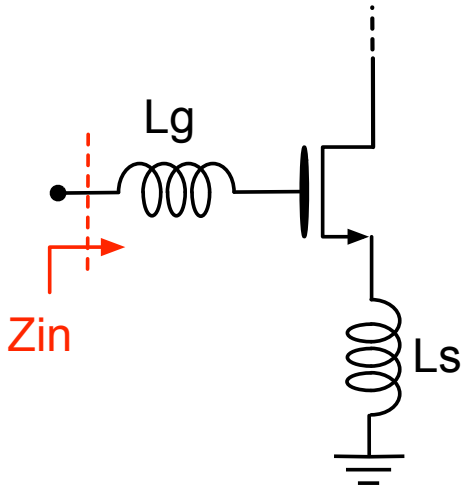
- **Configurable Filter Cascade**
  - Gm-RC biquad and Rauch filters
- **Flexible Op-AMP**
  - Digital control of GBW, DC gain and output impedance
- **Hybrid ADC**



Reconfigurable LNAs

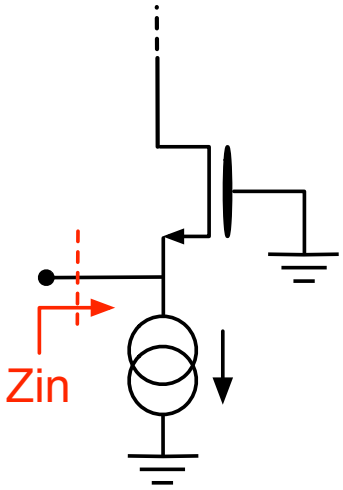
Scaling efficiently performances and power
for multistandard and adaptive radios

Choosing the starting point



Inductive degenerated LNA

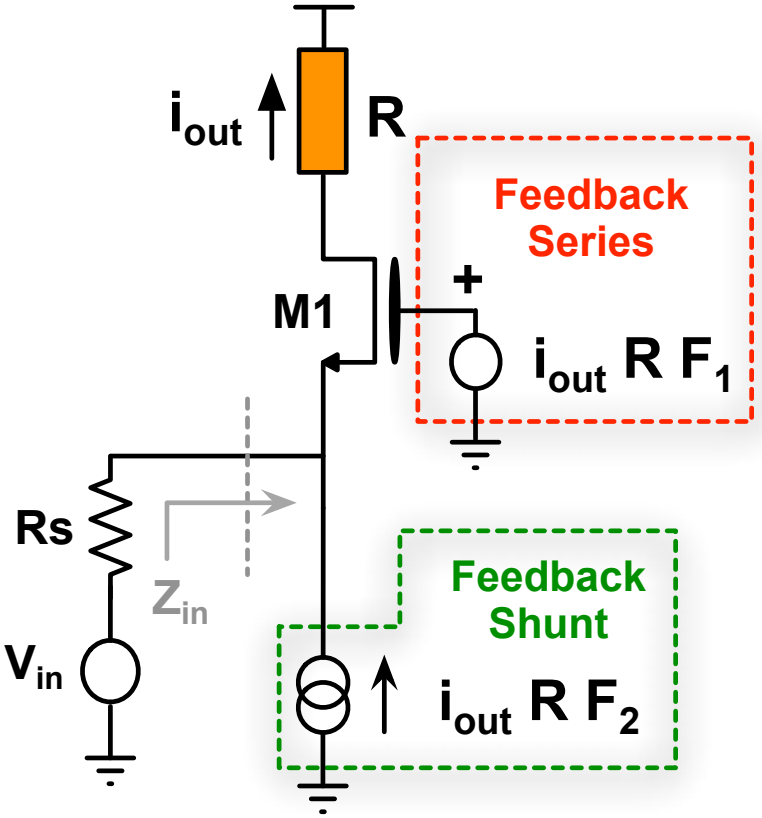
- Very low noise figure
- Narrow band input matching
- Low level of re-configurability



Common gate LNA

- Relatively high noise figure
- Wide band input matching
- Re-configurability with feedback introduction

Feedback around common gate LNA



Voltage (series) feedback

return to the gate (negative when F1>0)

Current (shunt) feedback

return to the source (positive when F2>0)

The output of the system is taken as the current iout

Input Impedance and Matching

Series feedback

$$Zin = \frac{1}{gm} \cdot \frac{1 + F1 \cdot R \cdot gm}{1 - F2 \cdot R}$$

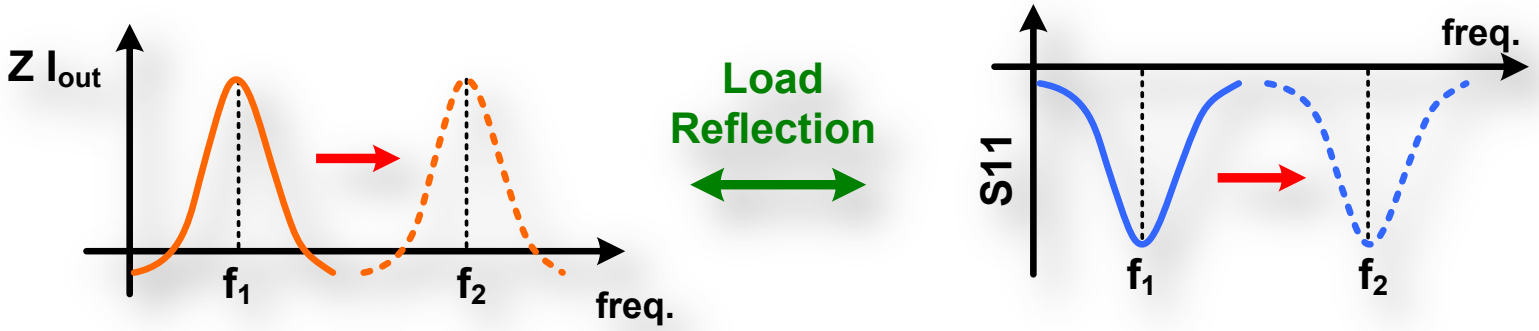
Open loop

Shunt feedback

Matching condition Zin =Rs

$$gm = \frac{1}{Rs - (F1 + F2Rs)R}$$

The load dependency allows input impedance frequency shaping (in presence of resonant load



Noise Figure under matching

1) gm dependency

Noise Transistor — Noise Load

$$NF = 1 + \frac{\gamma}{gmRs} + \frac{Rs}{R}\left(1 + \frac{1}{gmRs}\right)$$

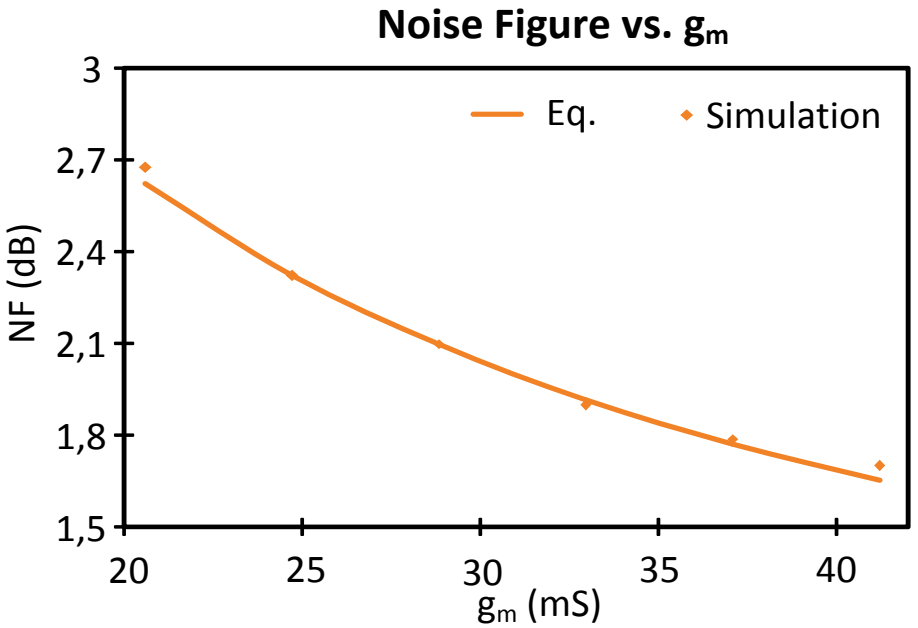
2) Feedback dependency

Noise Transistor — Noise Load

$$NF = 1 + \gamma\left(1 - \frac{R}{Rs}(F1 + F2Rs)\right) + \frac{Rs}{R}\left(2 - \frac{R}{Rs}(F1 + F2Rs)\right)^2$$

The feedbacks allow to choose a $g_m > 1/Rs$ reducing NF under matching condition

$$gm = \frac{1}{Rs - (F1 + F2Rs)R}$$



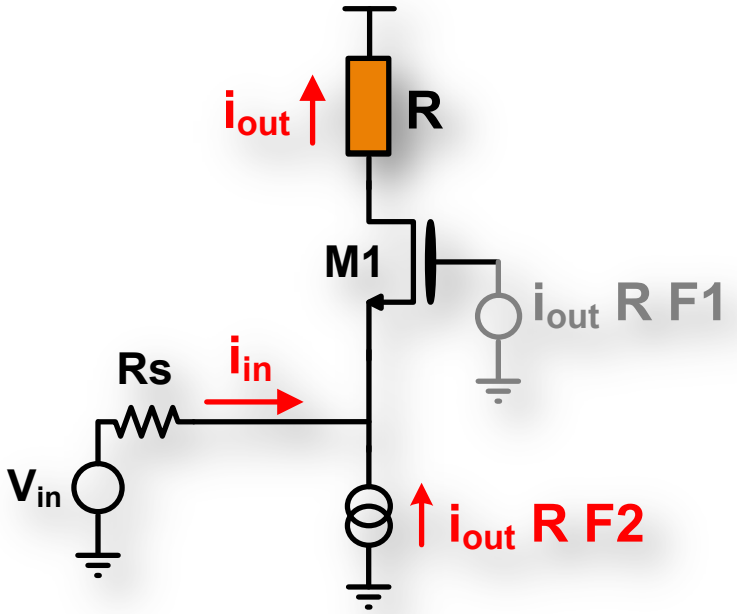
Transconductance Gain

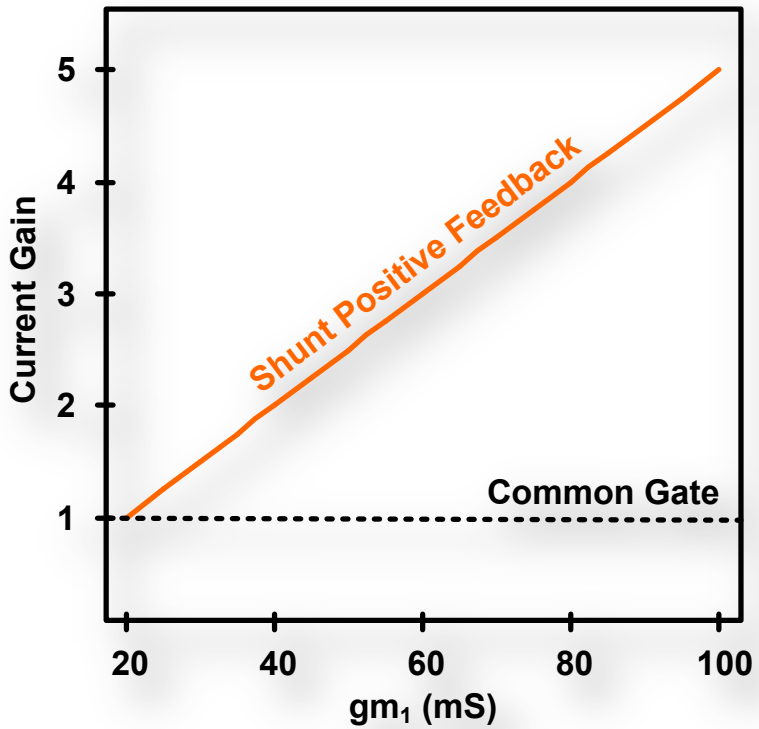
Open loop

Shunt Feedback

$$Gm\Big|_{Matching} = \frac{1}{2Rs} \cdot \frac{1}{1 - R \cdot F2}$$

Only shunt feedback acts on the transconductance gain





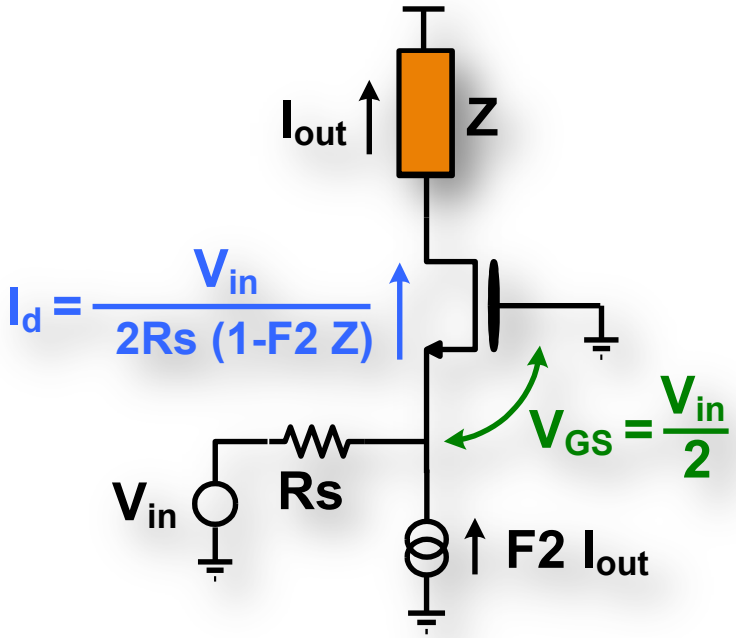
Linearity

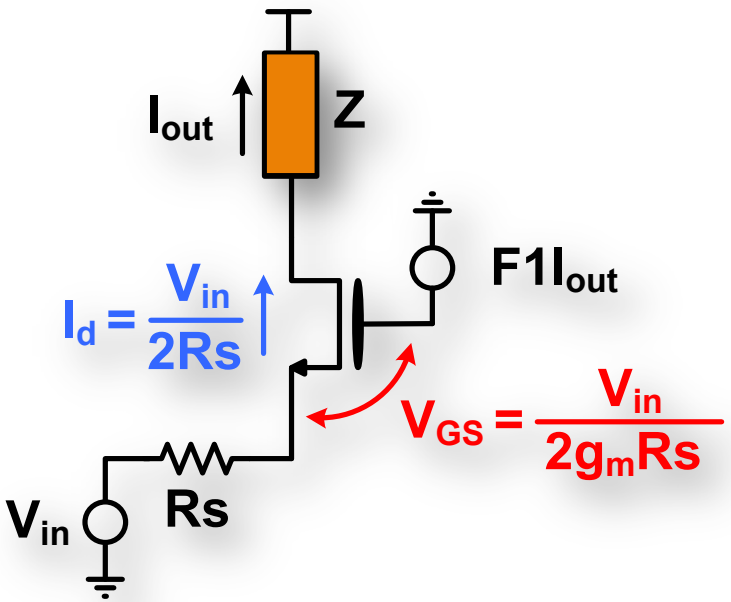
Open loop

$$IIP3_{CG} = \left| \frac{16V_{OV}^2(2+\theta V_{OV})}{3Rs} \right|$$

Series Feedback

$$IIP3_{F1} \approx IIP3_{CG} \left| 1 + R \cdot F1 \right|^3$$





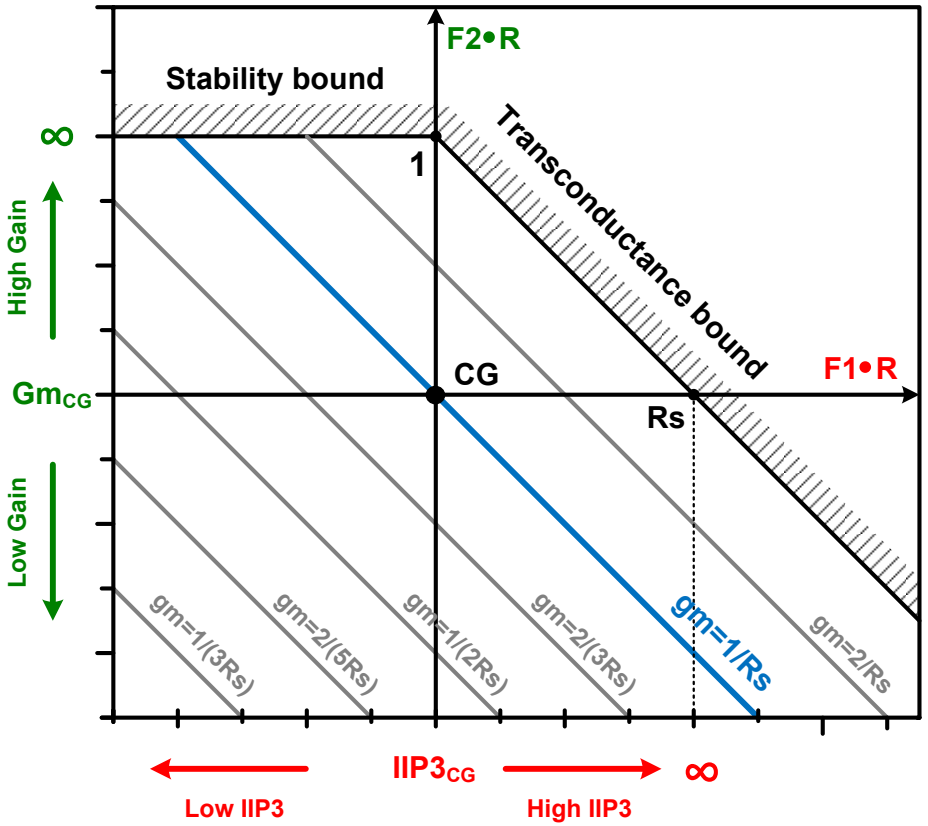
For a given operating point only F1 influence the IIP3!!

Feedback Plane

Feedbacks F1, F2 sets IIP3 and gain.

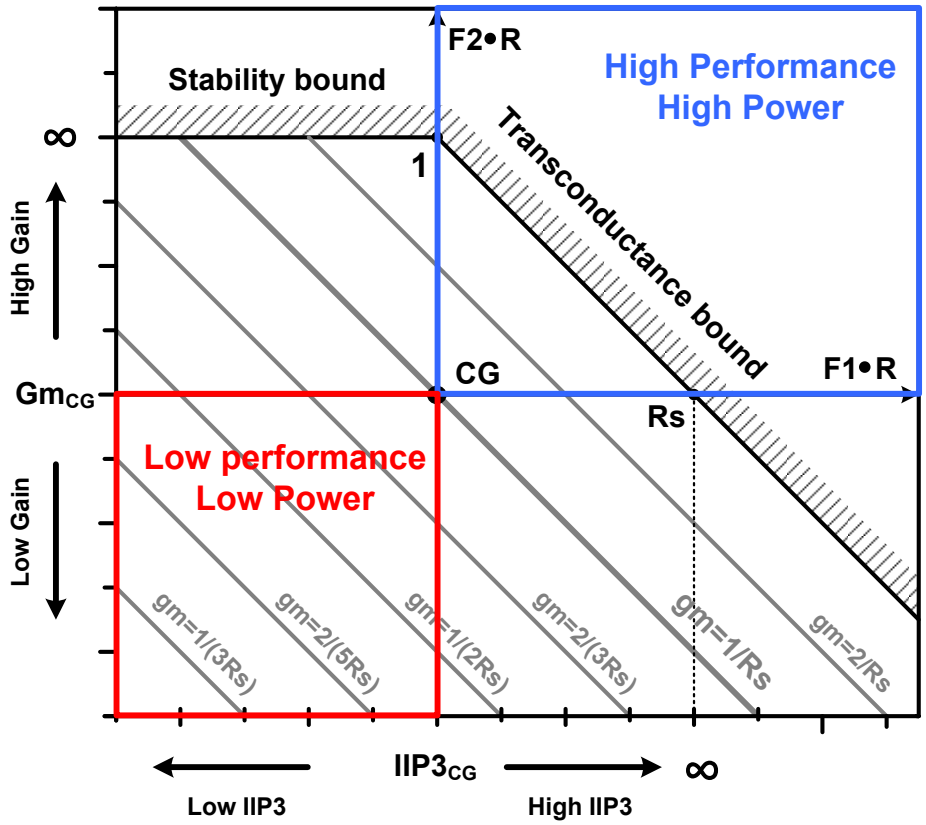
The diagram includes the gm curves, that complete the design

Two bounds are presents, for stability and gm values



For a given overdrive each feedback sets independently one design parameter!

Design Strategies

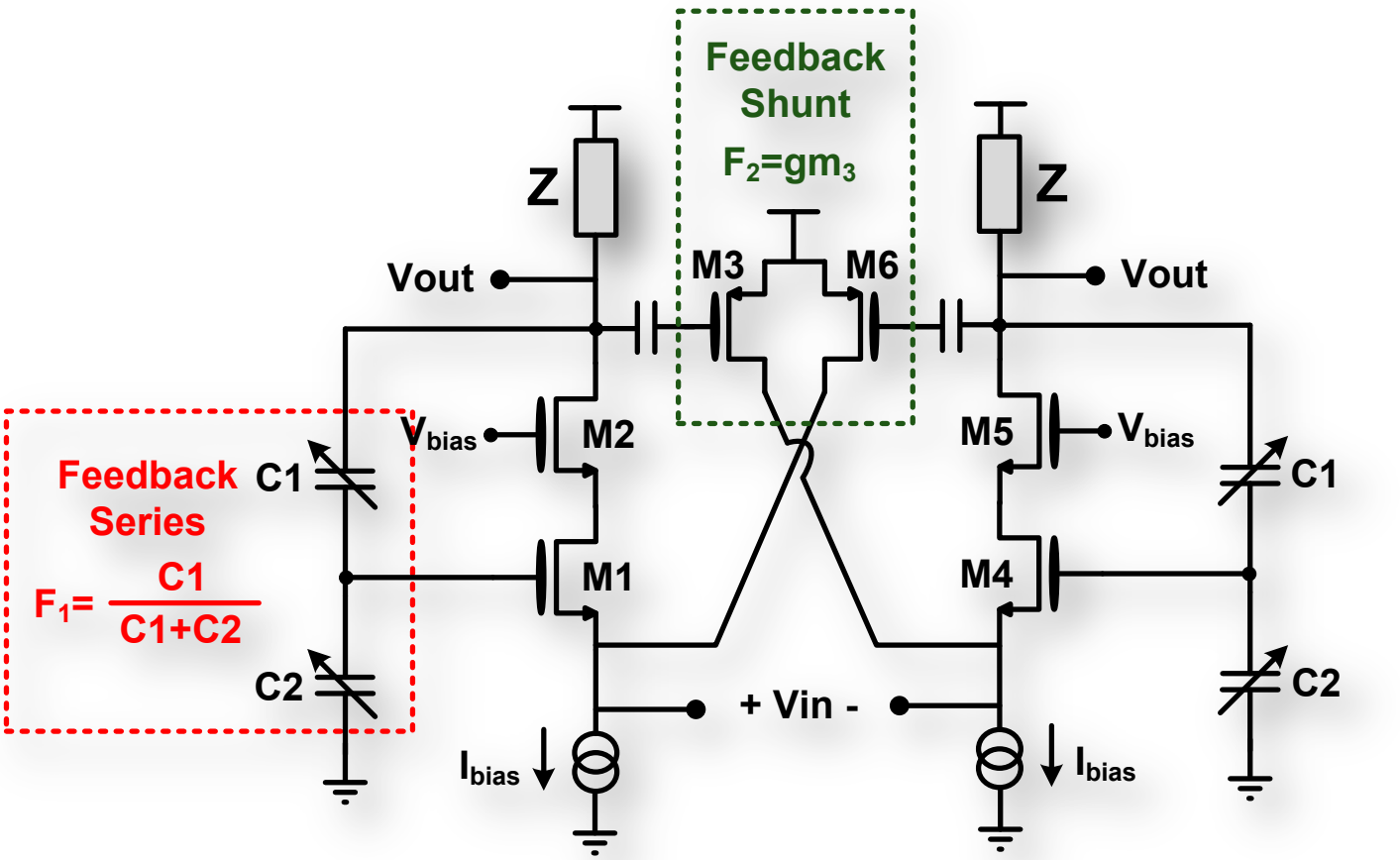


Feedback plane allows an easy design optimization

For a given overdrive higher g_m required higher power consumption.

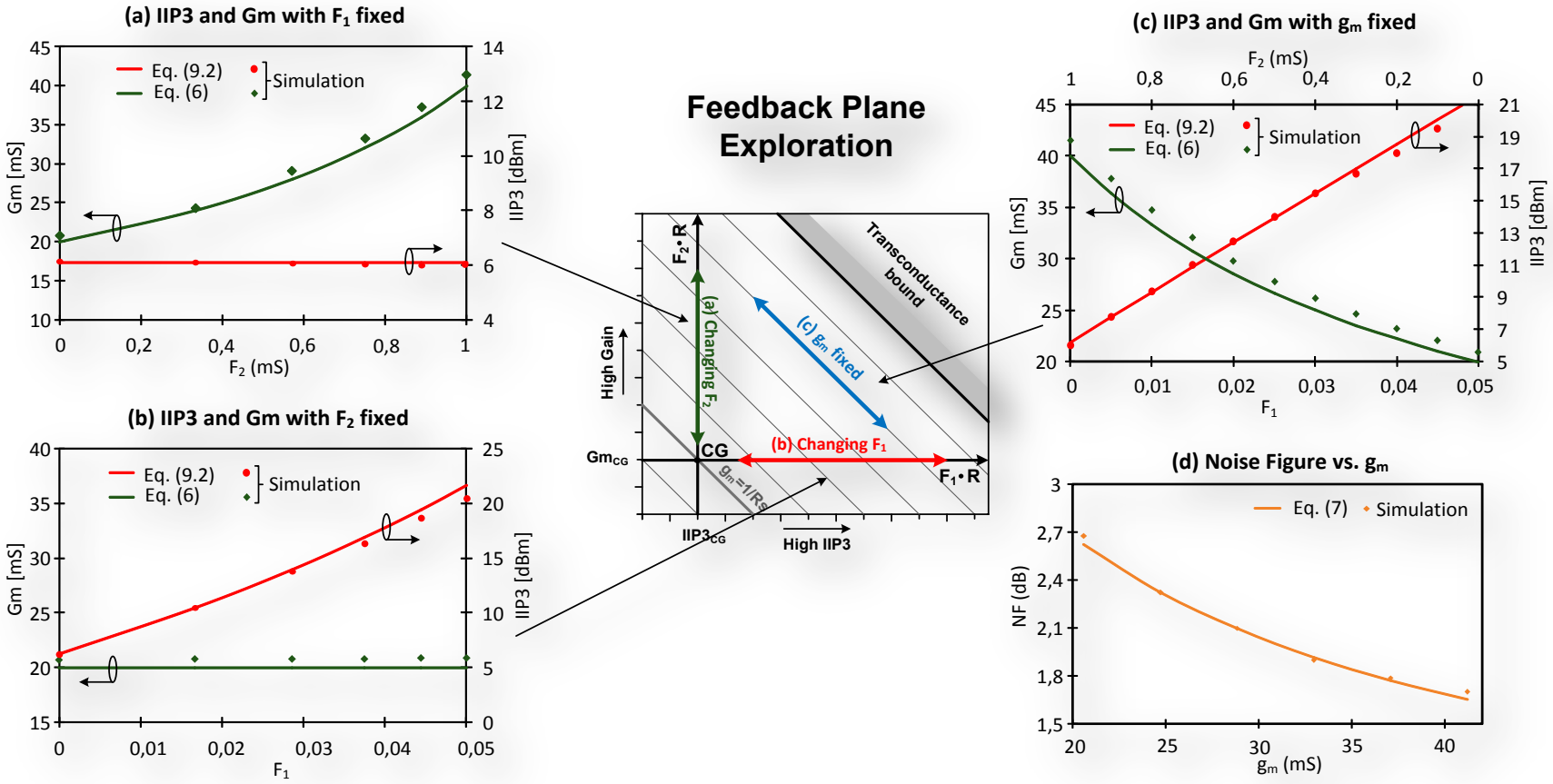
Dynamic feedback plane exploration allows an easy performance re-configurability

Adaptive Low Noise Amplifier



The combination of both feedback is realized using a capacitive divieder (series feedback) and a cross-connected gm-pair (shunt feedback)

Feedback plane Exploration



Dynamic feedback plane exploration allows an easy **performance re-configurability**

Reconfigurable LNA main features

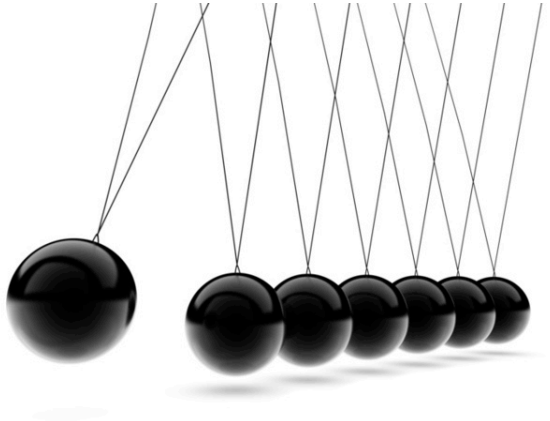
- Introduction of feedback in common gate LNA allows to reduce NF and to shape in frequency the input-matching
- Feedbacks combination is used to have efficient power scalability varying independently gain, linearity and NF

- Main References:

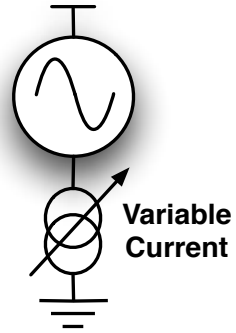
Liscidini, A., Martini, G., Mastantuono, D., Castello, R., "Analysis and Design of Configurable LNAs in Feedback Common-Gate Topologies", *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 55, no. 8, pp. 733-737, Aug

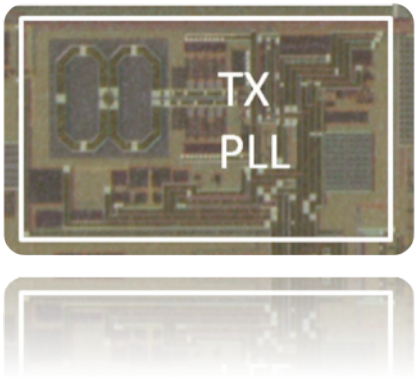
Power scalable oscillator

Scaling efficiently performances and power for multistandard and adaptive radios



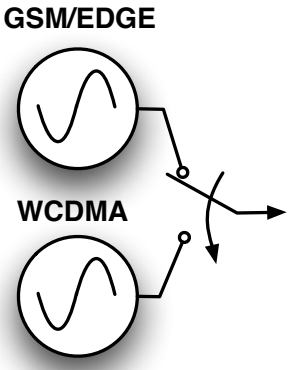
State of the Art of VCO for Cellular TX

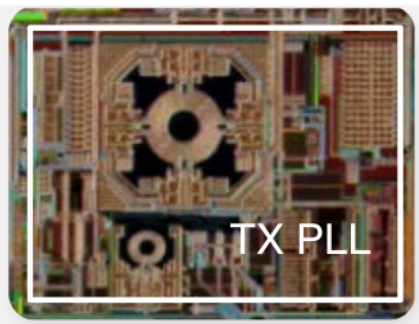




Same oscillator for GSM and WCDMA transmitters

[e.g. Nilsson et al. M., ISSCC '11]



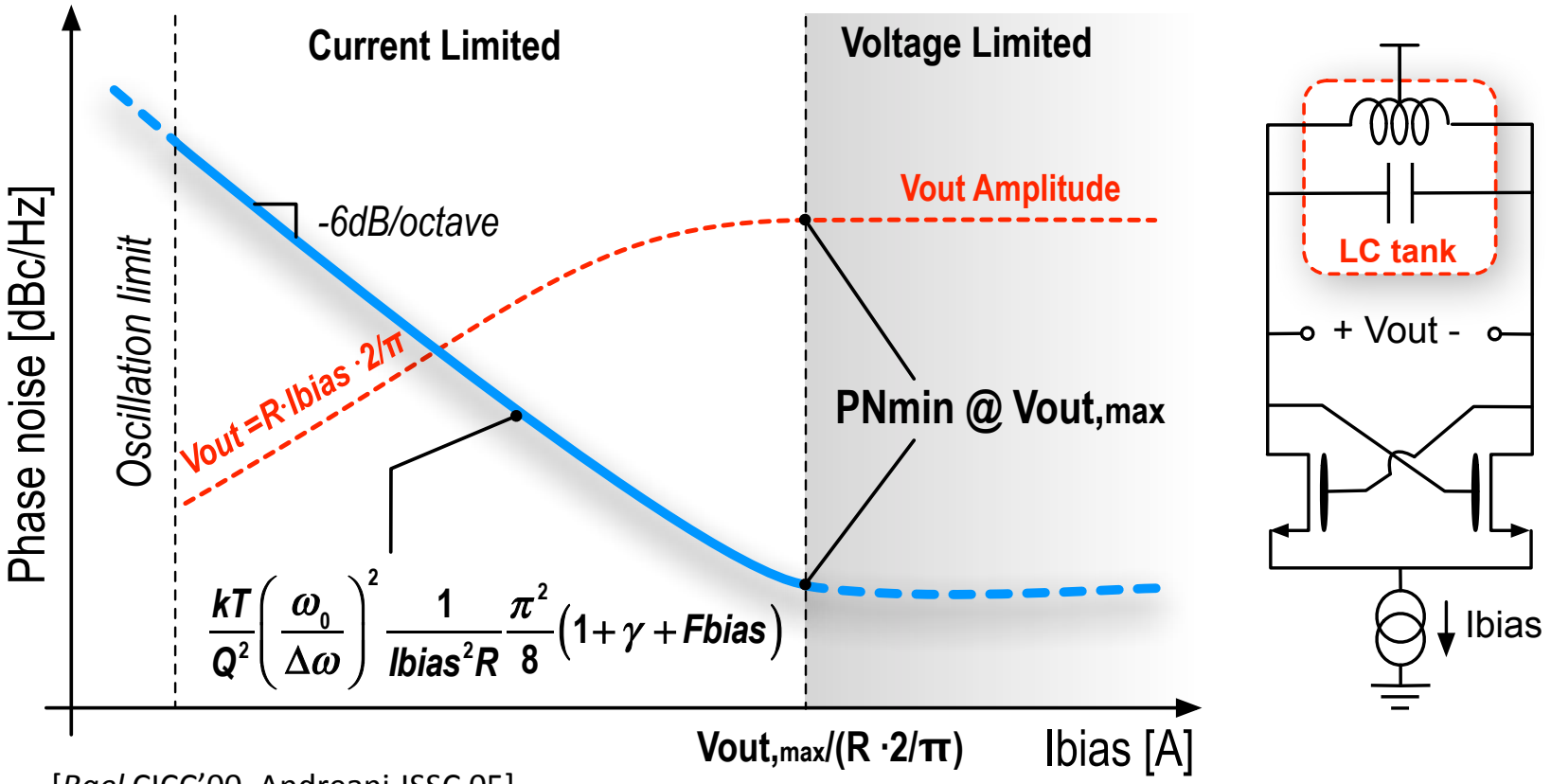


Two oscillators for GSM and WCDMA transmitters

[e.g. Hadjichristos et al. , ISSCC'09]

Why these two different strategies?

Phase noise of LC vs. Bias Current



[*Rael* CICC'00, Andreani JSSC 05]

In the current limited region, the phase noise scales as the amplitude

When current is doubled, PN decreases by 6dB

Phase noise and power efficiency (FoM)

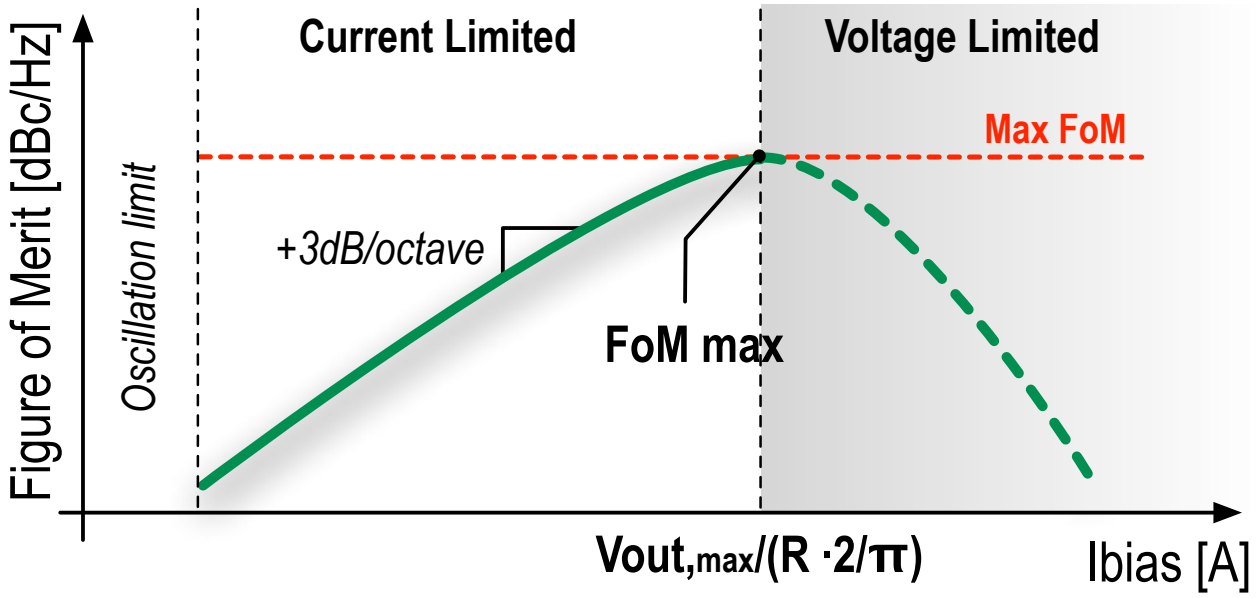
LO frequency

Power cons.($V_{DD} \cdot I_{bias}$)

$$FoM = (\omega_{LO} / \Delta\omega)^2\Big|_{dB} - PN\Big|_{dB} - (P_{diss} / 1mW)\Big|_{dB}$$

Offset from the carrier

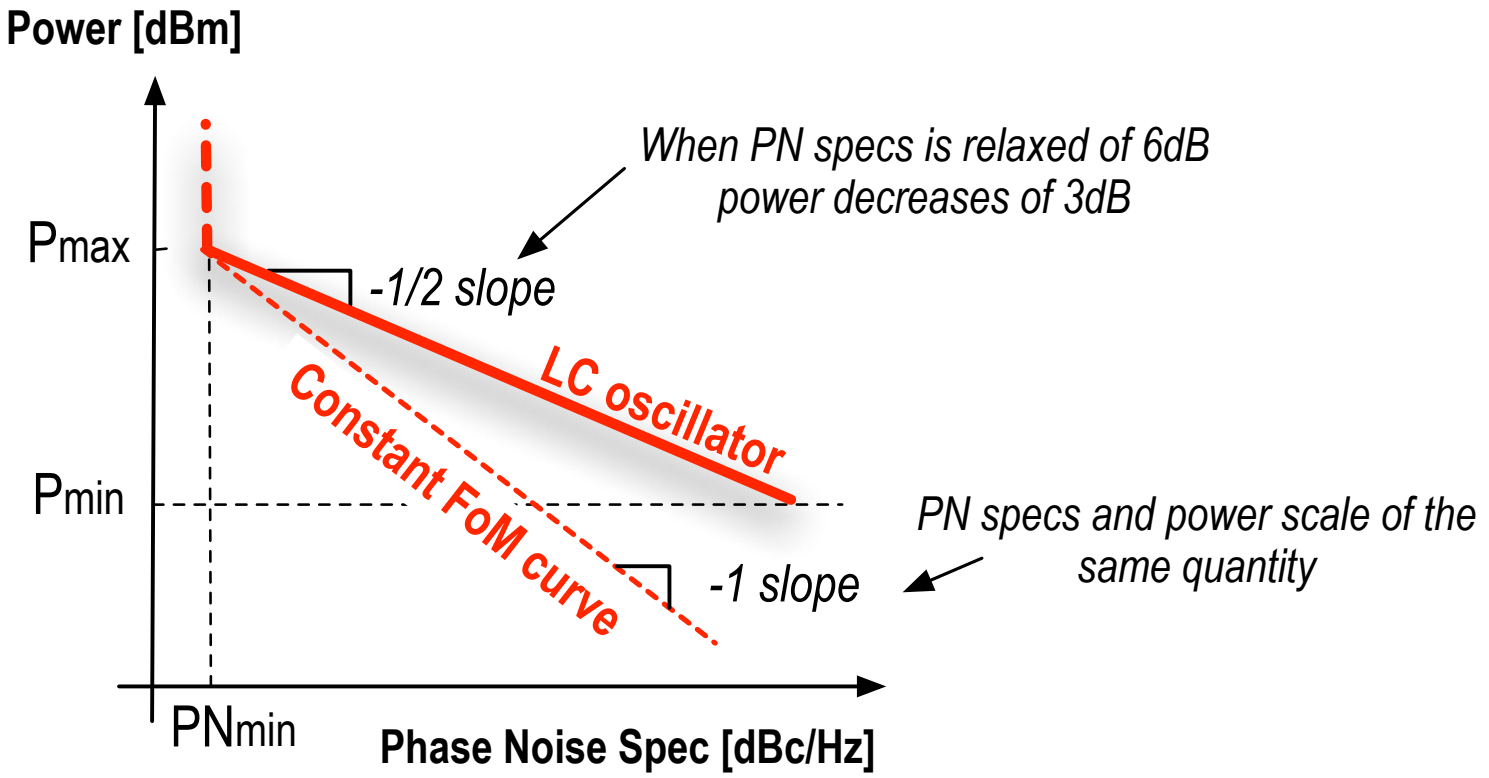
Phase Noise ($\propto 1/I_{bias}^2$)



Optimum FoM for the highest power consumption and not for the most used case

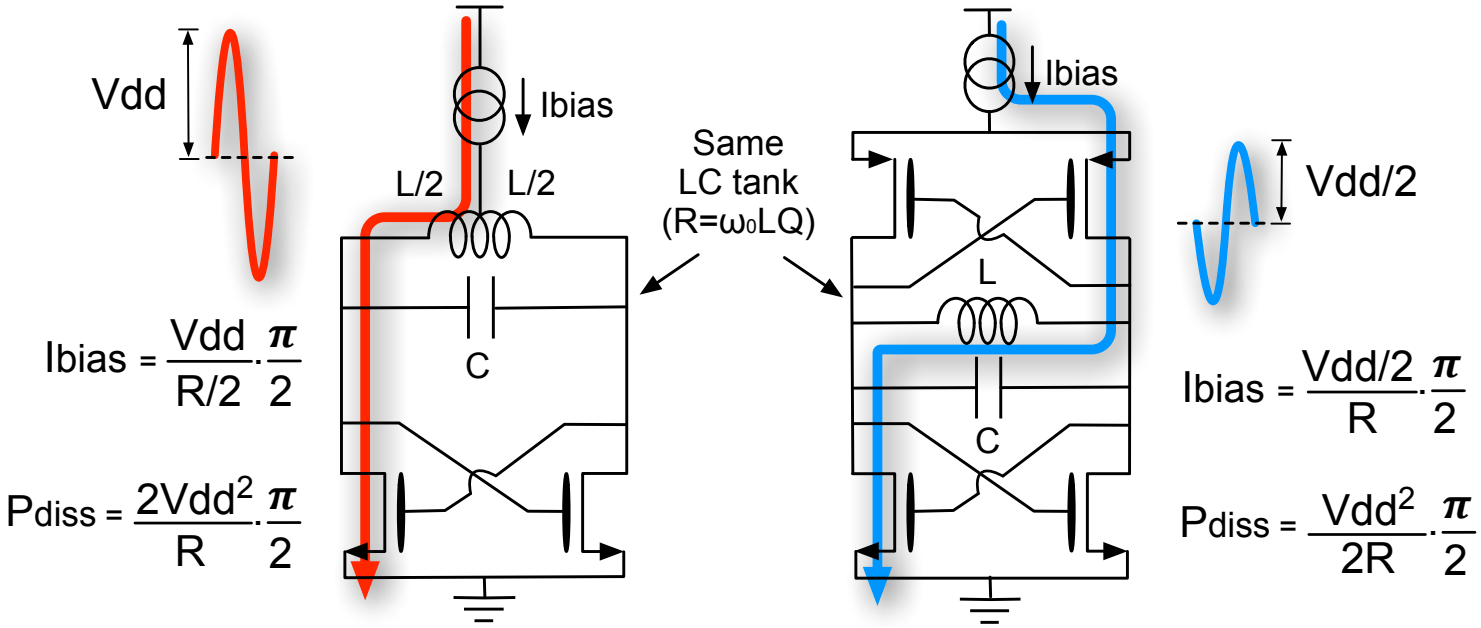
Power scalability plot

Power consumption (axis Y) vs. phase noise spec (axis X)



No power efficiency and limited configurability range

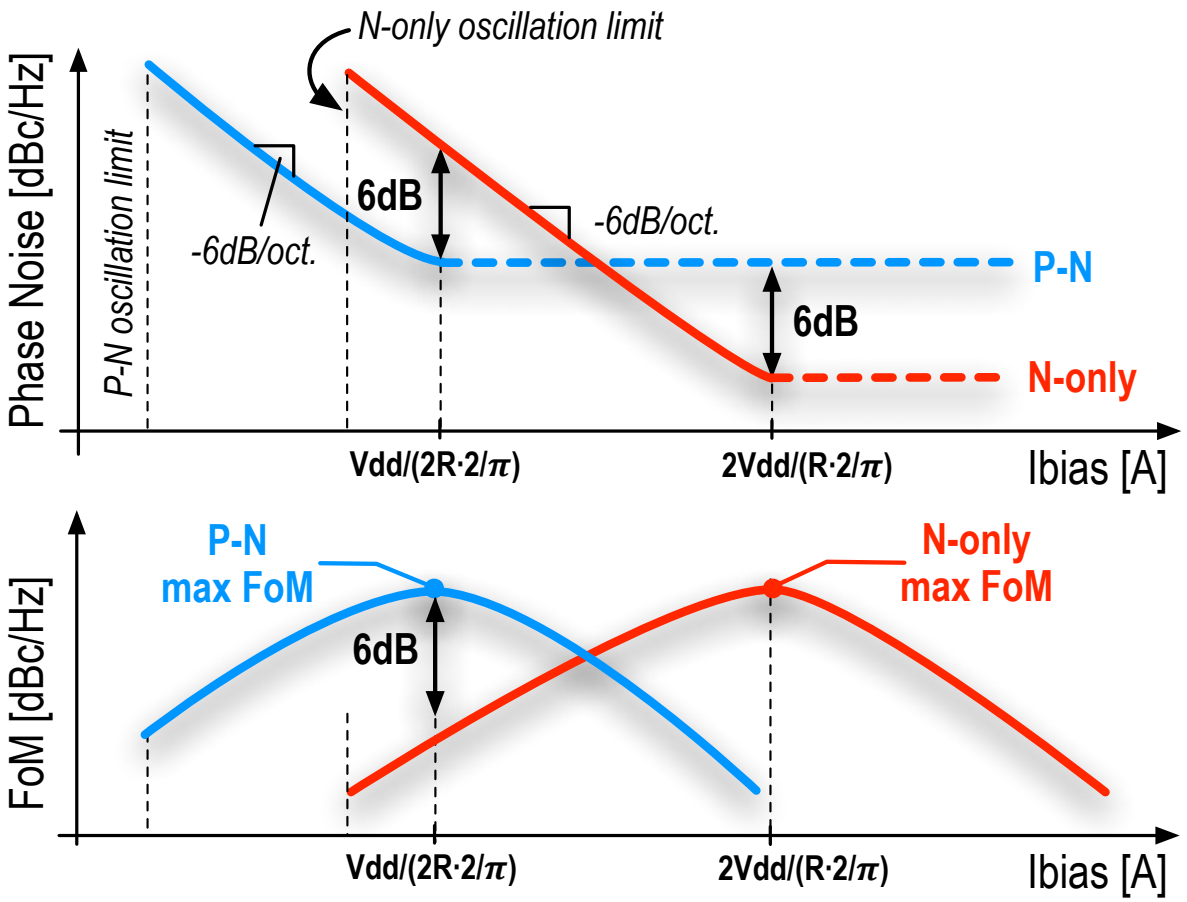
N-only vs. P-N LC tank oscillators



- Amplitude in P-N oscillator is half and phase noise 6dB more
- P-N oscillator uses the entire tank drawing ¼ of current of N-only oscillator (consuming 6dB less)

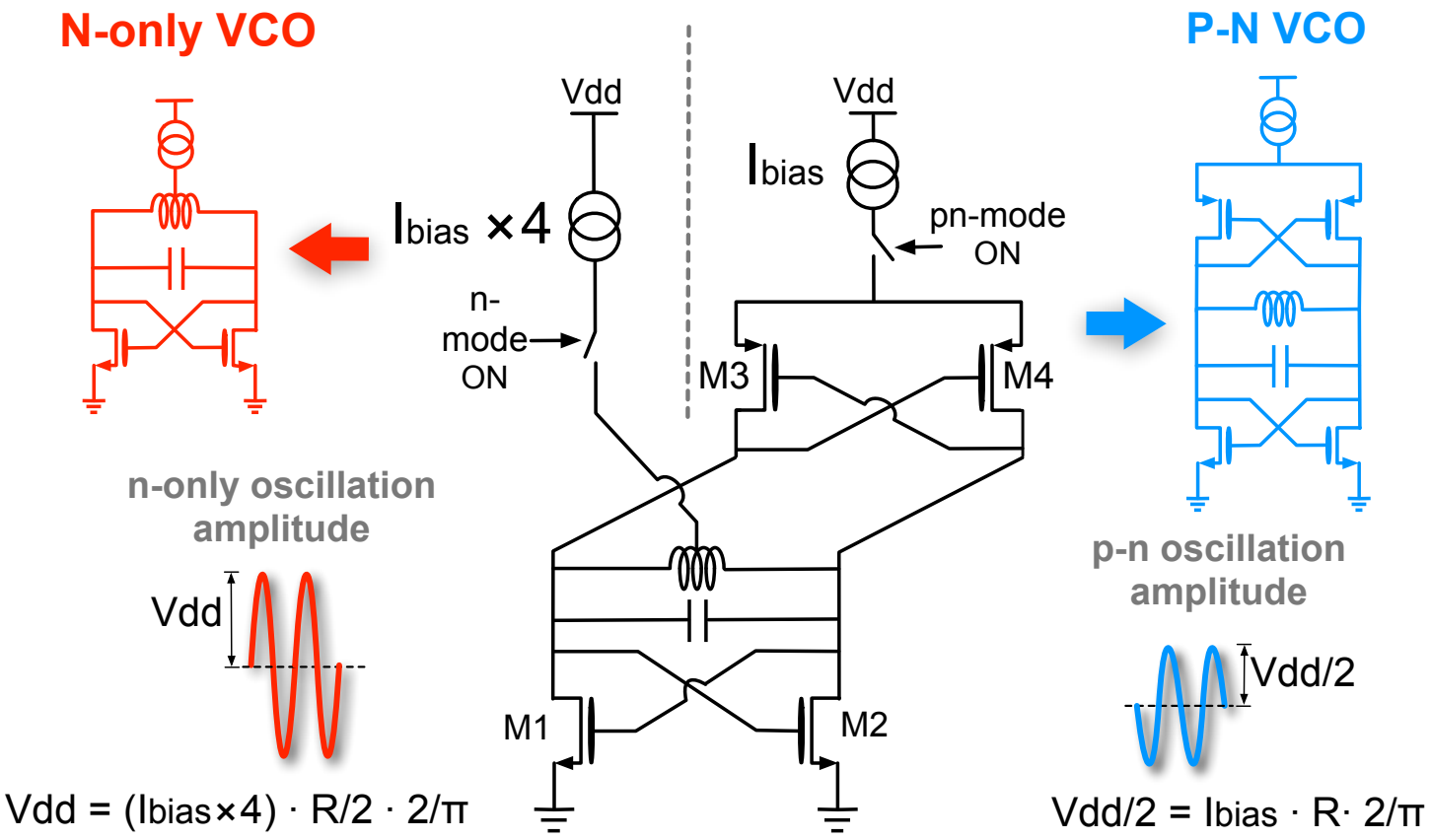
N-only and P-N topologies have the same maximum FoM (ideally)

Phase noise and FoM comparison



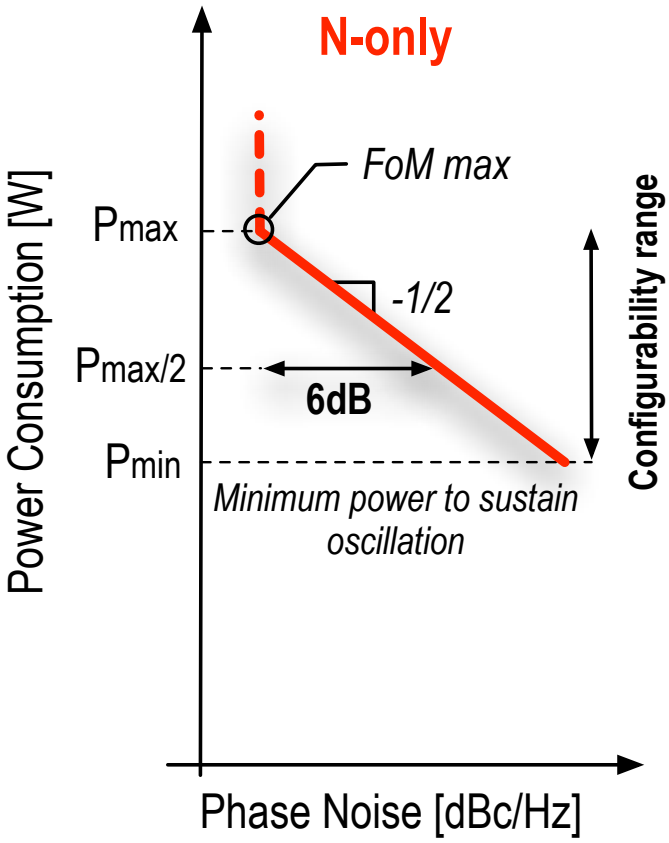
P-N performance is shifted toward a lower power consumption and a higher phase noise, keeping the same maximum FoM

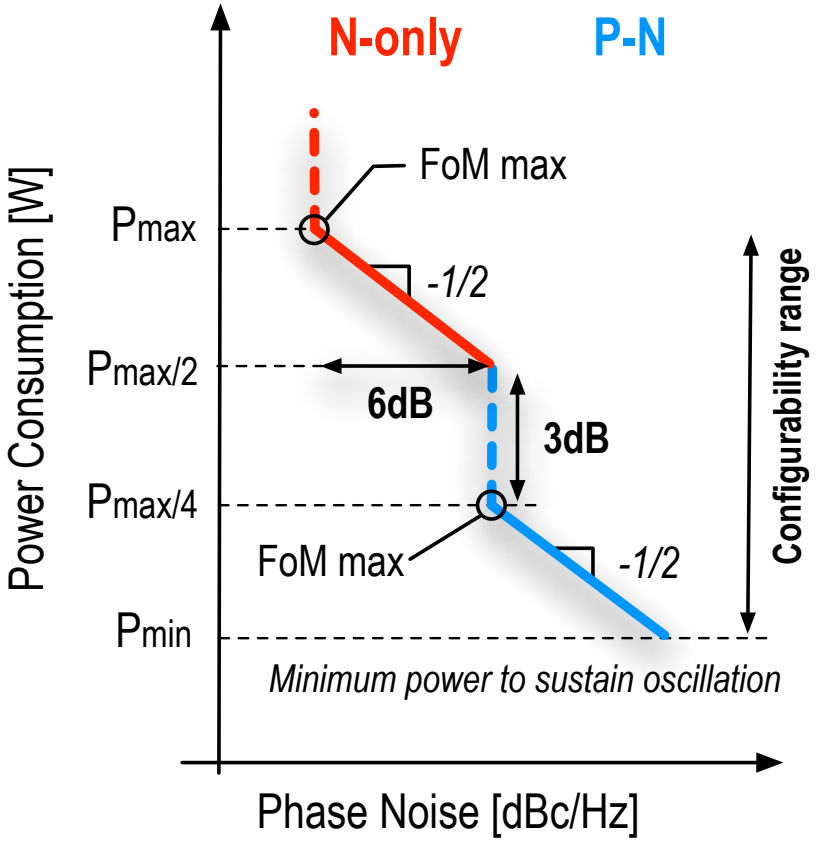
Power scalable oscillator



Higher power efficiency and power scalability beyond N-only oscillator limit

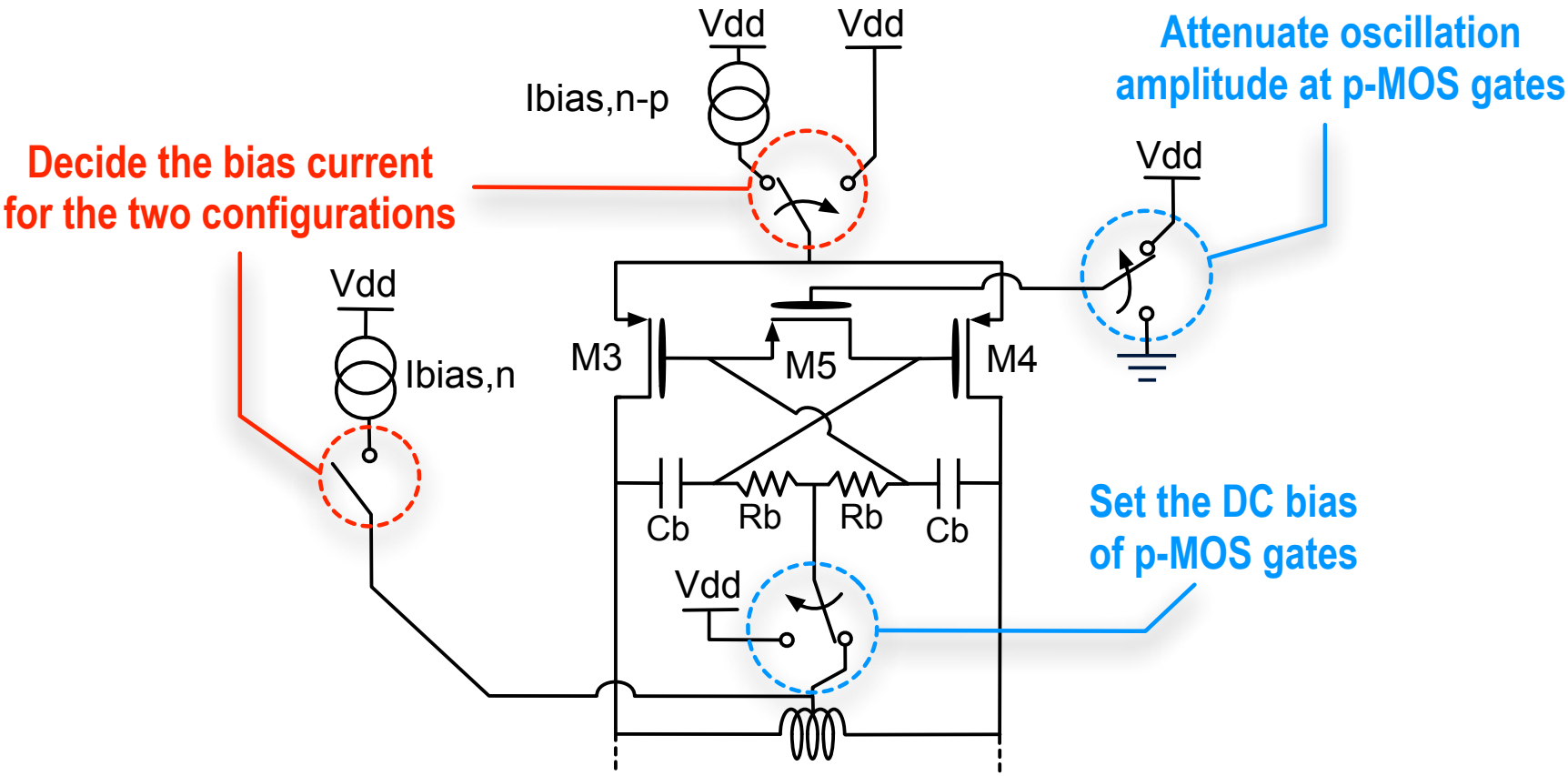
Power scalability comparison





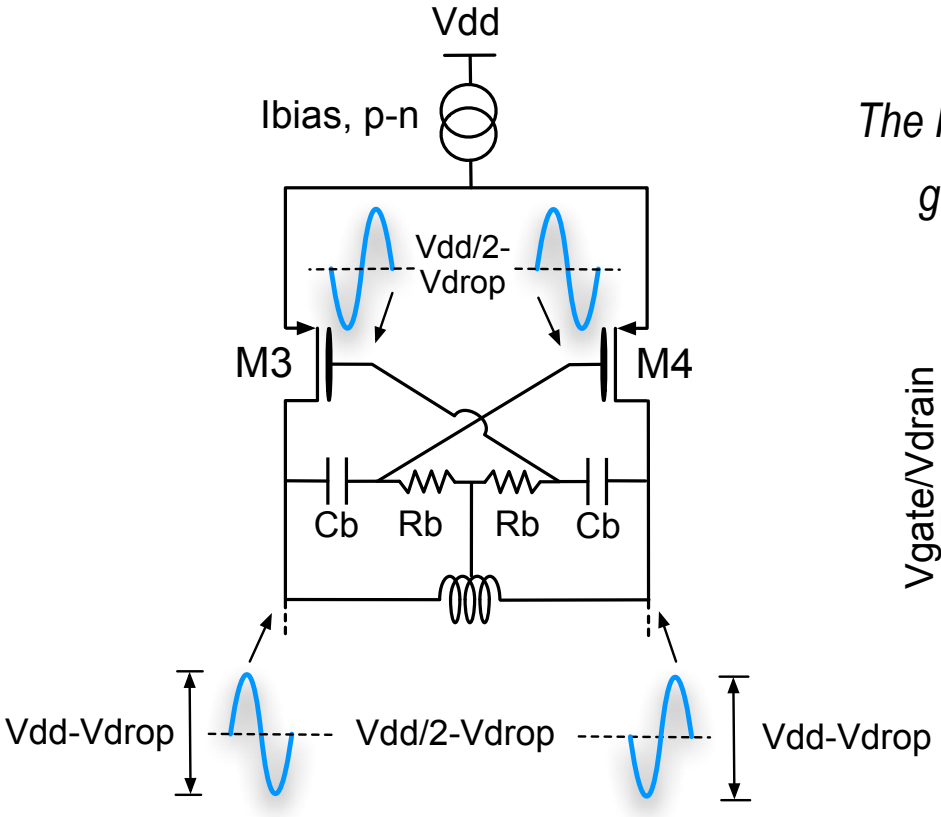
When phase noise is relaxed by 6dB, power consumption is reduced by a factor 2 compared to an N-only oscillator

VCO bias scheme

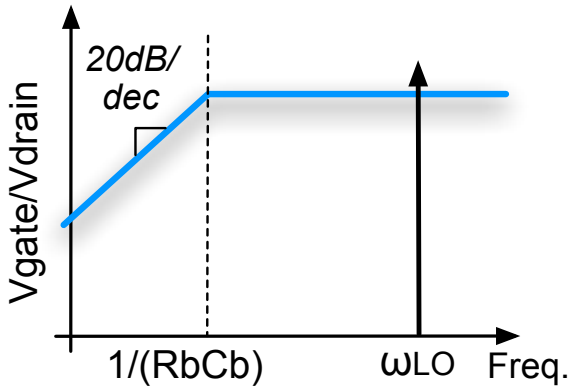


- p-MOS transistors must be completely switched-off in the N-only case to avoid Q-tank degradation
- Amplitude at p-MOS gates is set by RC network, tunable by M5

PMOS transistors in P-N mode

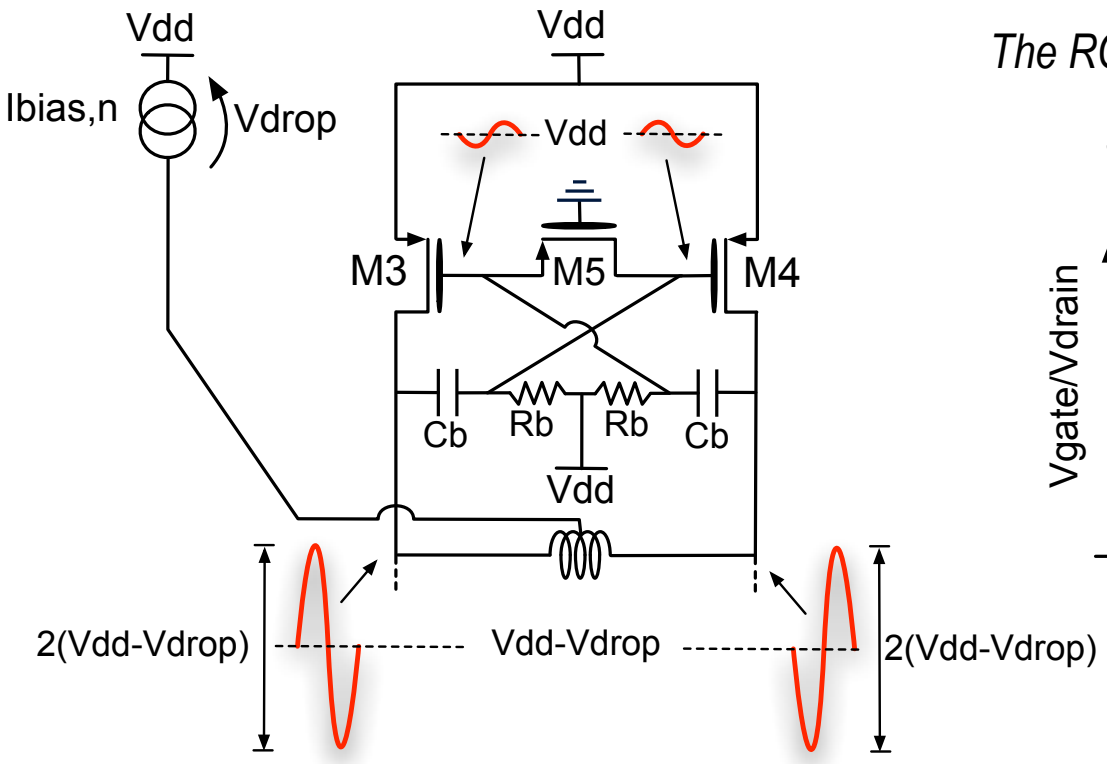


The RC network between drains and gate act as an high-pass filter

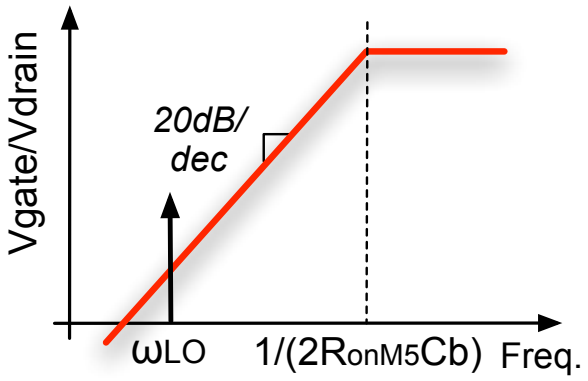


- The dc-bias is set connecting the gate to the center tap of the inductor
- When M5 is off, the cut-off frequency is 1/(CbRb)

PMOS transistors in N-only mode

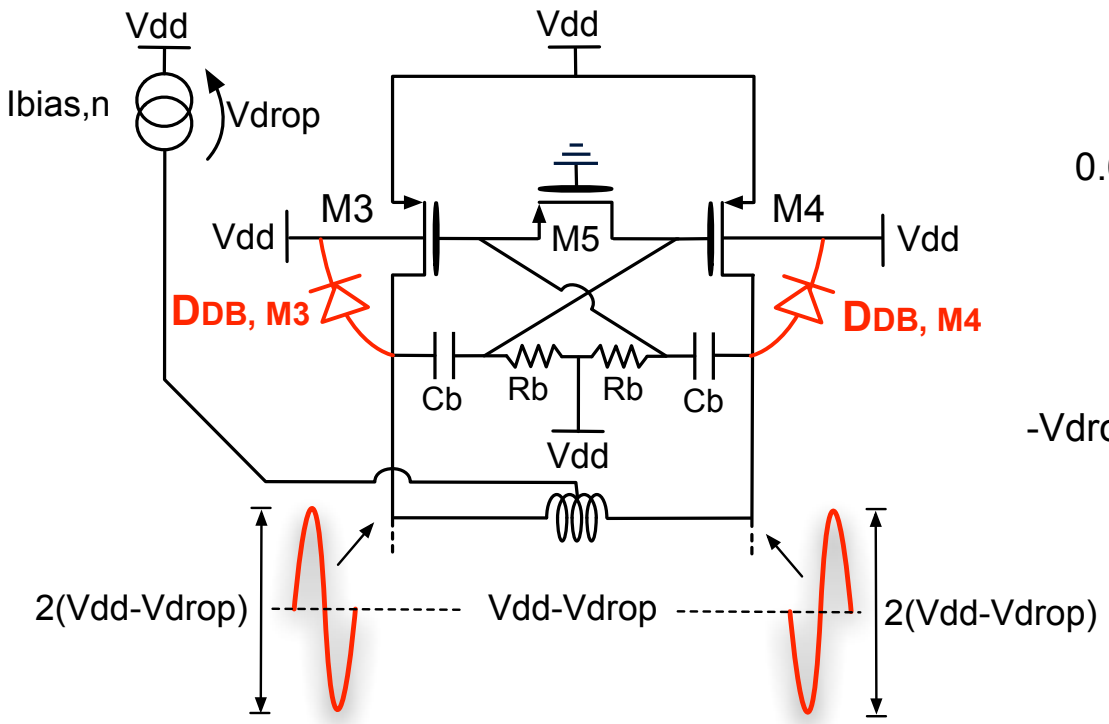


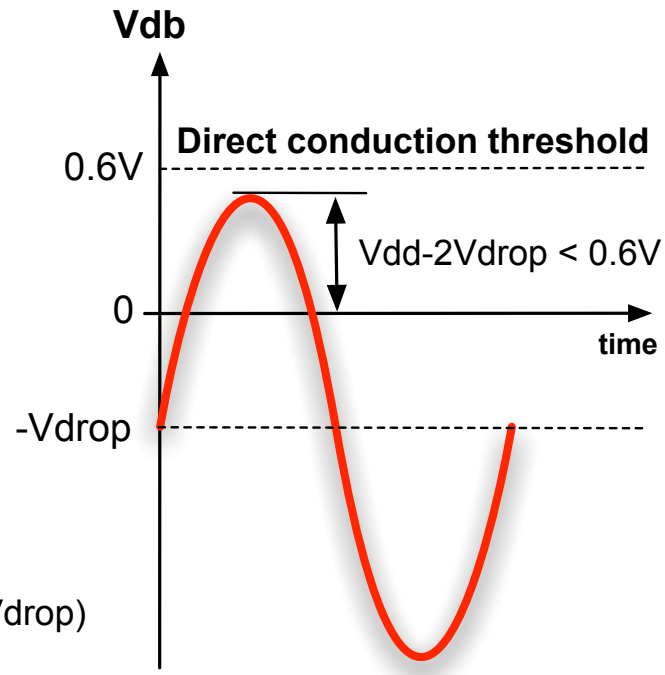
The RC network between drains and gate filter the LO signal



- The pMOS gate bias is set to Vdd to keep them off
- M5 shunts Rb and the filter cut-off frequency becomes $1/(2R_{onM5}Cb)$

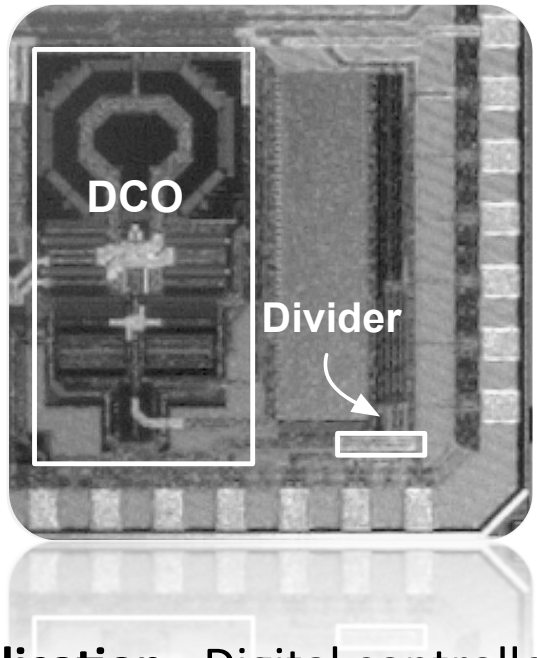
Drain-Bulk diode in N-only mode

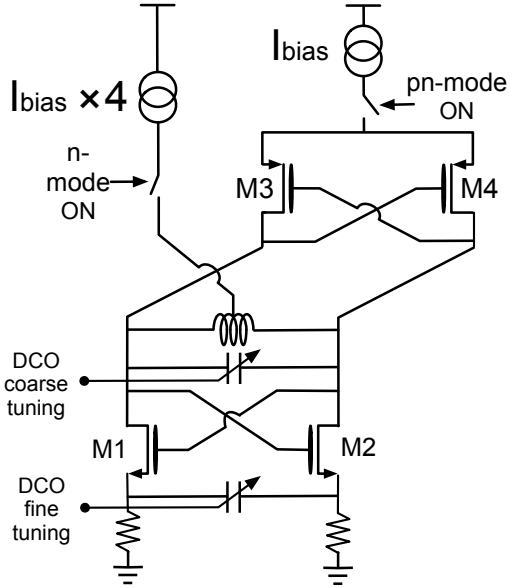




Large amplitude can lead the pMOS drain-bulk junctions in direct conduction degrading the Q of the tank

Integrated prototype





Application: Digital controlled oscillator for Multistandard 2G-3G Transceiver

Design: 55nm CMOS (Vdd = 1.5V) / Active area = 0.49mm^2

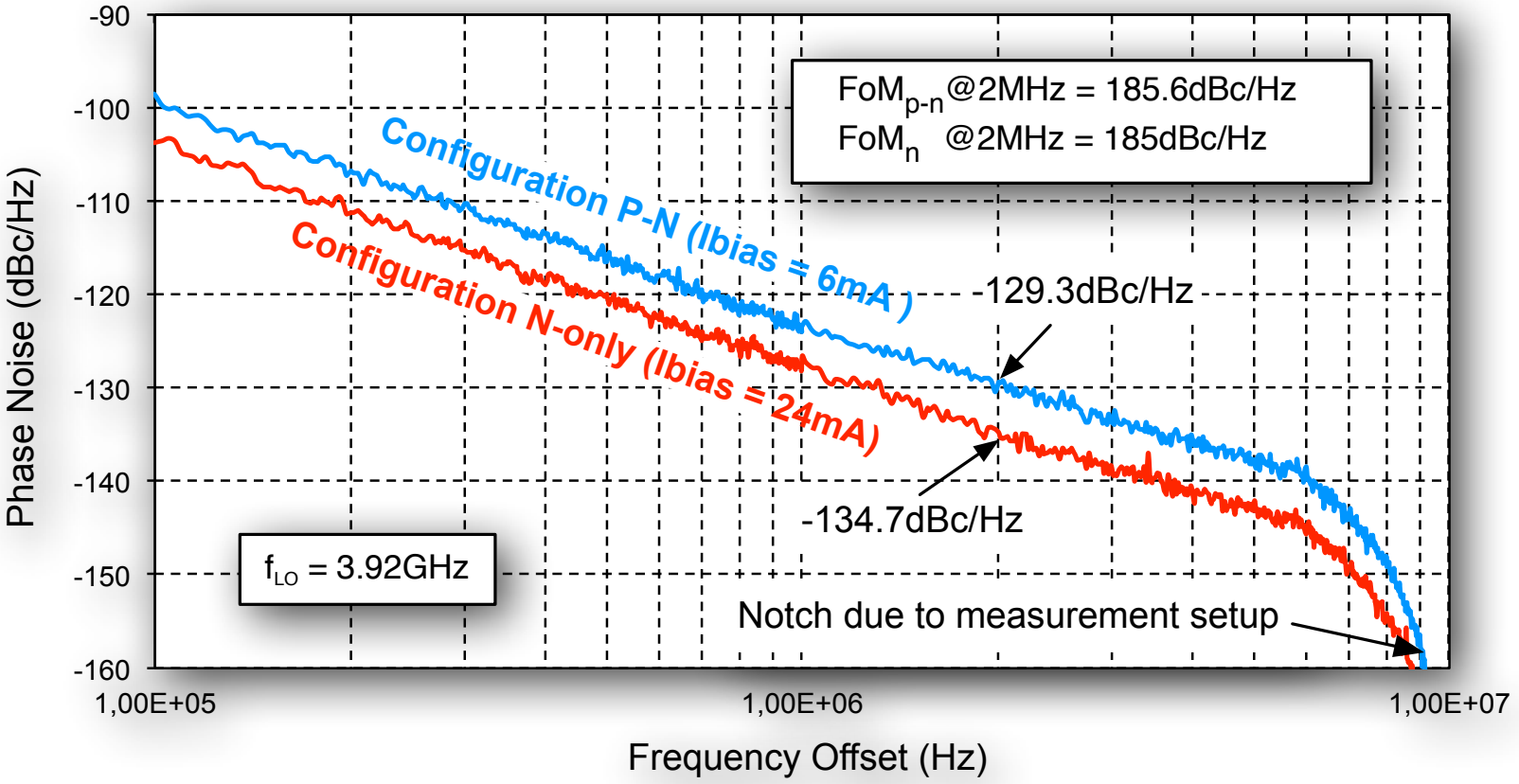
Power dissipation. : from 6.75mW to 36mW

Oscillation Frequency: 6.5GHz-9GHz

Phase Noise 4GHz @ 2MHz: -129.3dBc/Hz (9mW) ; -134.7dBc/Hz (36mW)

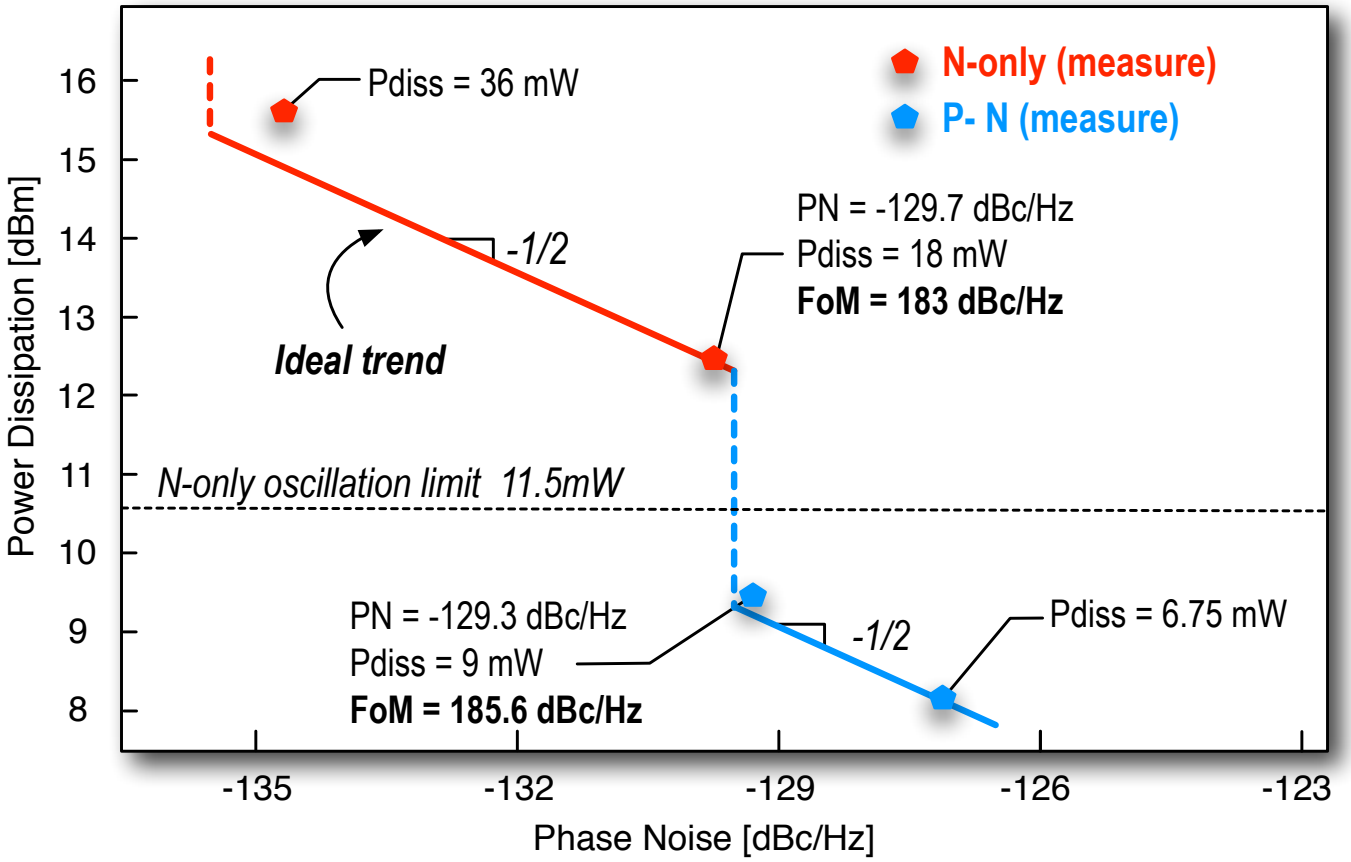
FoM 4GHz @ 2MHz: 185.6dBc/Hz (9mW); 185dBc/Hz (36mW)

Phase noise and power scalability



N-only and PN configurations have almost the same FoM, showing an efficient power scalability

Power scalability plot



Less power consumption for higher phase noise and extended re-configurability range compared to a single N-only oscillator

Power scalable oscillator main features

- Phase noise and power dissipation can be scaled keeping constant power efficiency
- Efficient power scalability suitable for multistandard transceivers and for adaptive radios

- Main References:

Liscidini, A.; Fanori, L.; Andreani P.; Castello, R.;, "A 36mW/9mW Power-Scalable DCO in 55nm CMOS for GSM/WCDMA Frequency Synthesizers," *Proceedings of the ISSCC 20112*, Feb. 2012

Conclusions

Conclusions

The reduction of power consumption in modern wireless transceivers can be achieved following two main strategies: the **power recycling** and the **power re-configurability**.

Power recycling reduces of the degrees of freedom and minimize **instant power dissipation**

Power re-configurability required an increment of the complexity and reduces **average power consumption**

Both these approaches have been discussed in the presented designs

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