Trapping in AlGaN/GaN Gate Injection Transistors: a combined electrical and optical investigation

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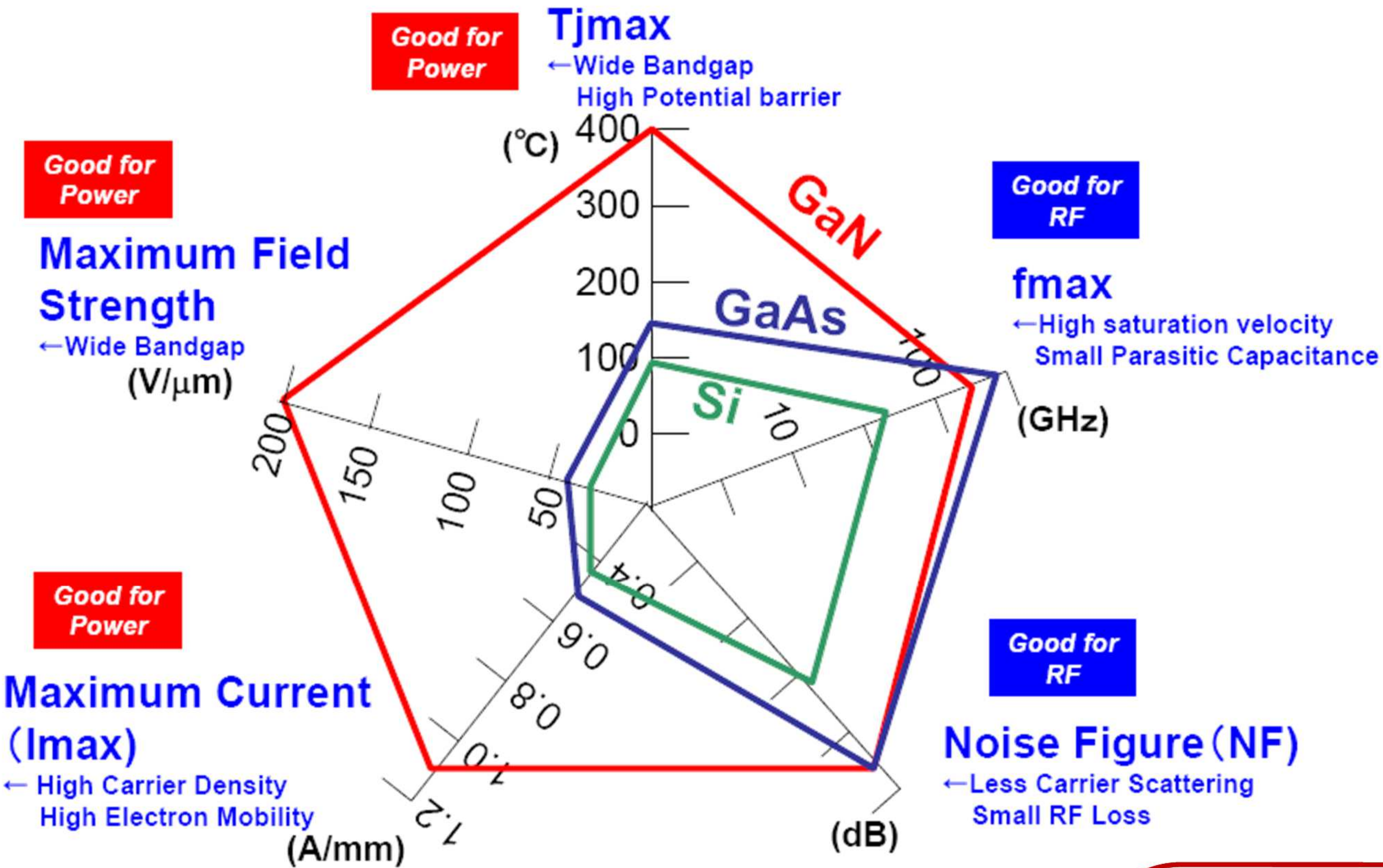
Outline

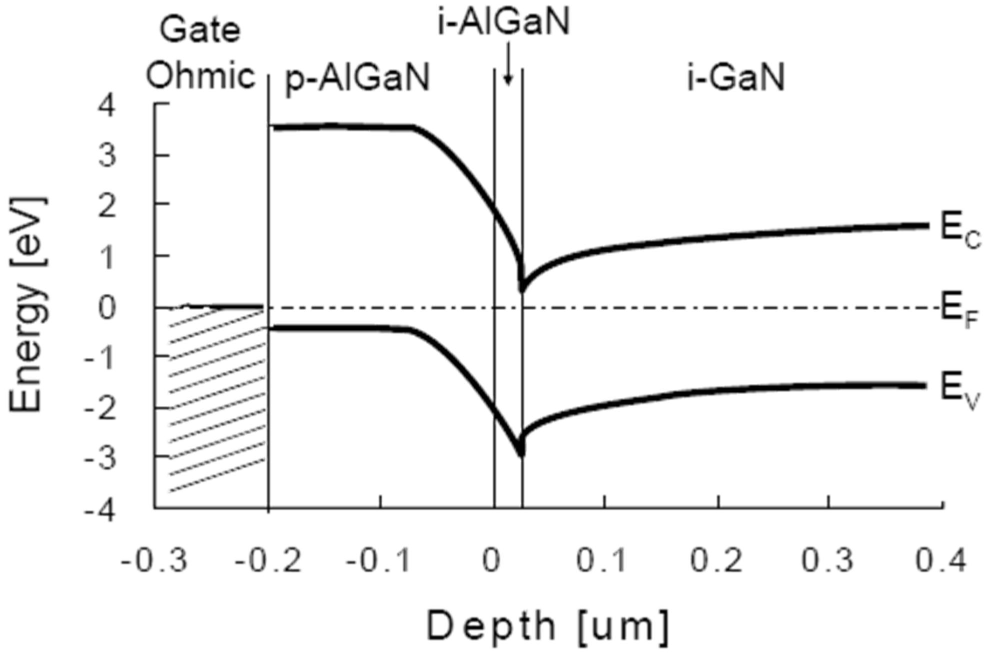
- Introduction
- Gate Injection Transistors (GITs) basics
- Trapping phenomena:
  - ON-resistance increase and recovery
  - Onset of drain electroluminescence
- Recovery process:
  - Temperature dependence
  - Hole injection dependence
- Problem resolved with improved devices

Introduction

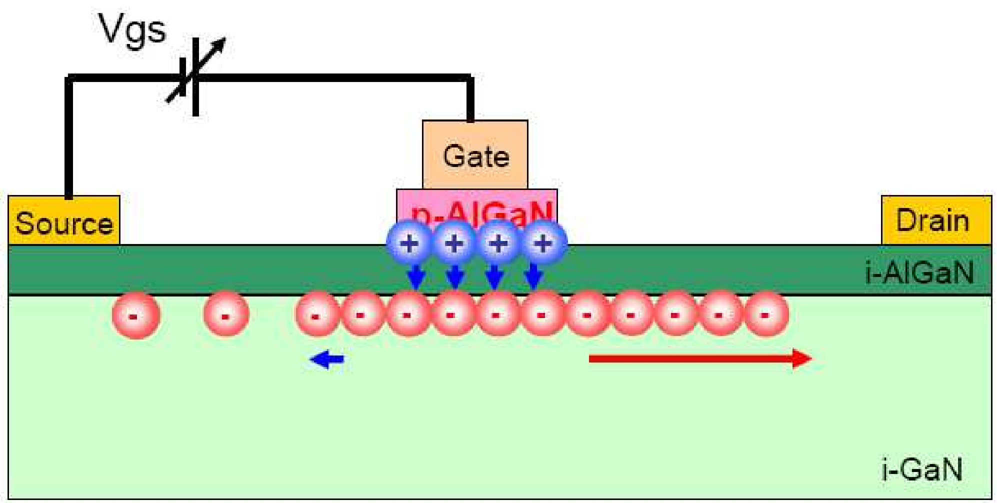


Basic Structure of a Gate Injection Transistor

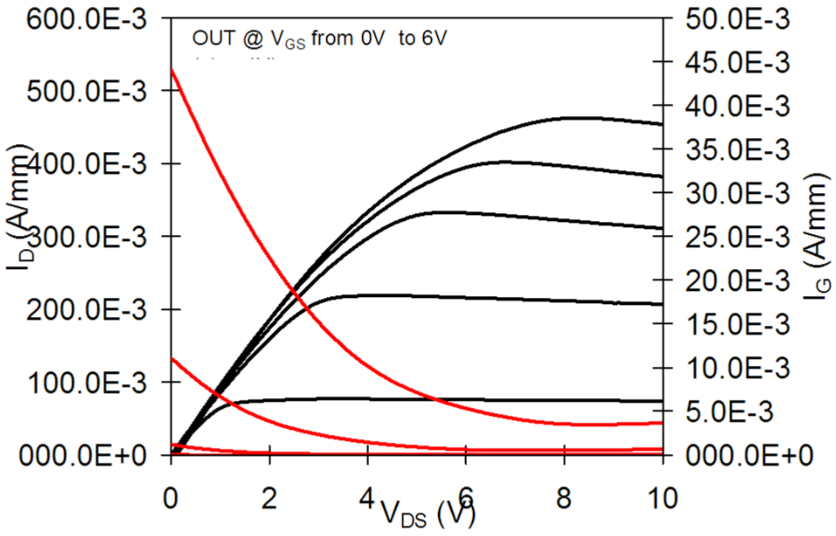
The use of a p-AlGaN layer under the gate causeses an increase of the local potential, giving a significant decrease in the e$^-$ concentration in the channel, and this allows to achieve normally-OFF operation



Furthermore, it was proposed that, for sufficiently high gate voltages, holes can be injected in the channel, and that this can result in a significant channel conductivity modulation (low hole mobility!).

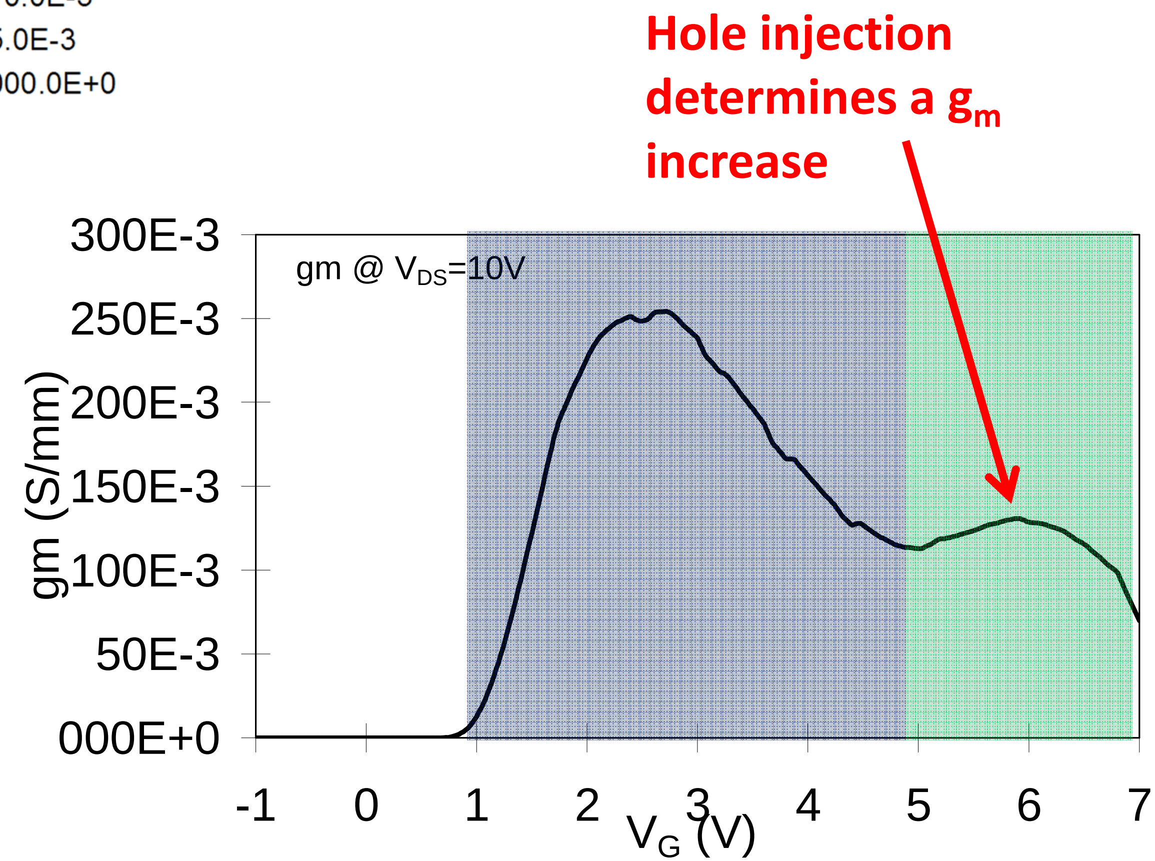


Electrical Characteristics

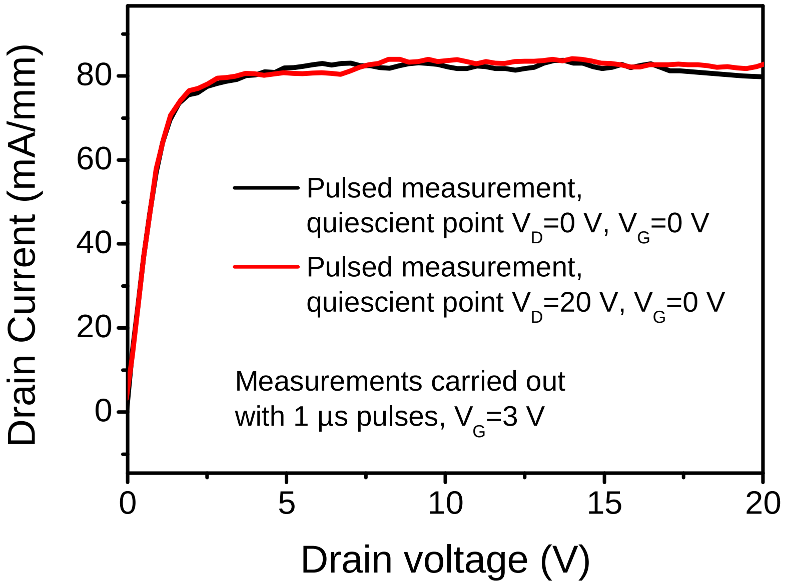


DC characteristics of one of the analyzed samples

The transconductance characteristic has two different regimes/peaks→ For VG>5 V, hole injection induces a transconductance increase

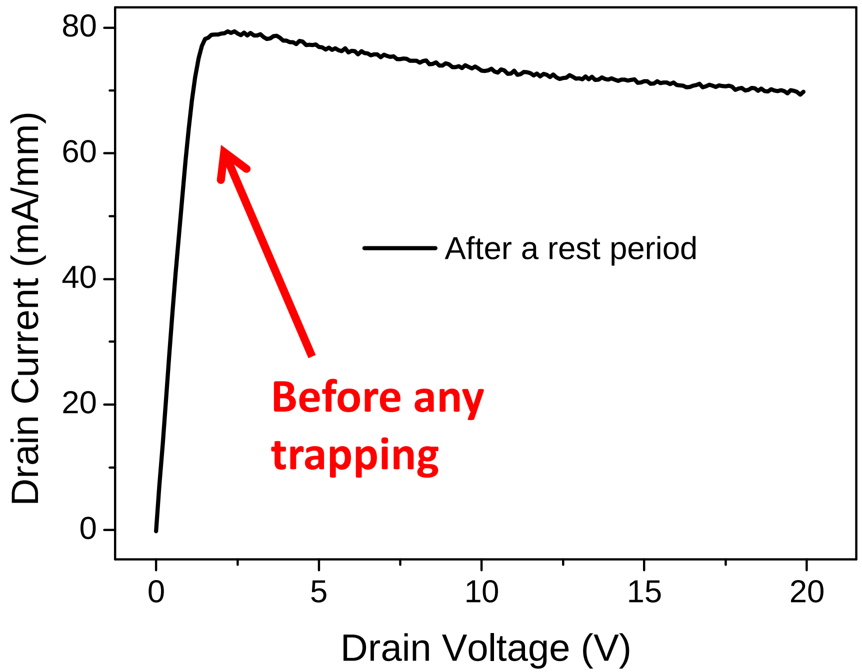


Trapping phenomena at high V_{DS} levels



Pulsed characteristics → Measurements are carried out starting from different quiescent (V_{GS}, V_{DS}) bias points, in off-state → **No significant current collapse detected by pulsed measurement at moderate V_{DS} levels**

A long-term exposure to high drain bias (between 30 and 100 V) can induce a significant charge trapping → Recoverable increase in Ron **(no variation in threshold voltage!!!)**



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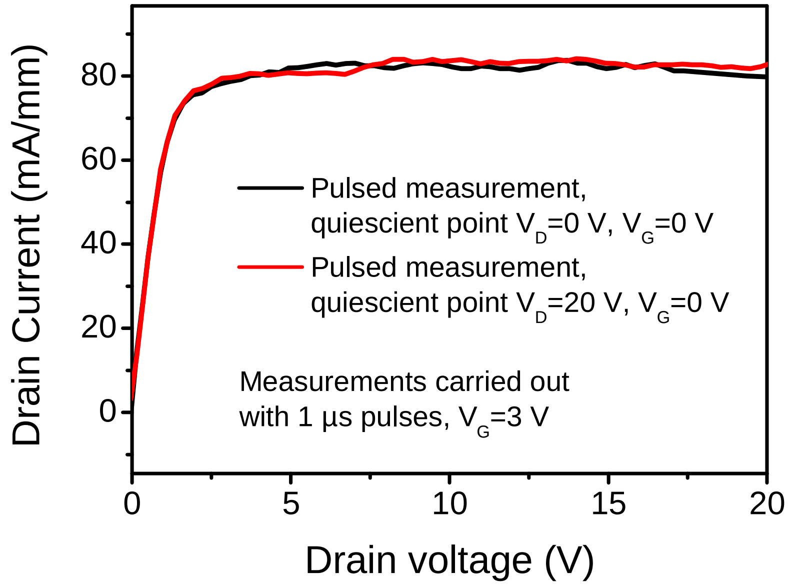

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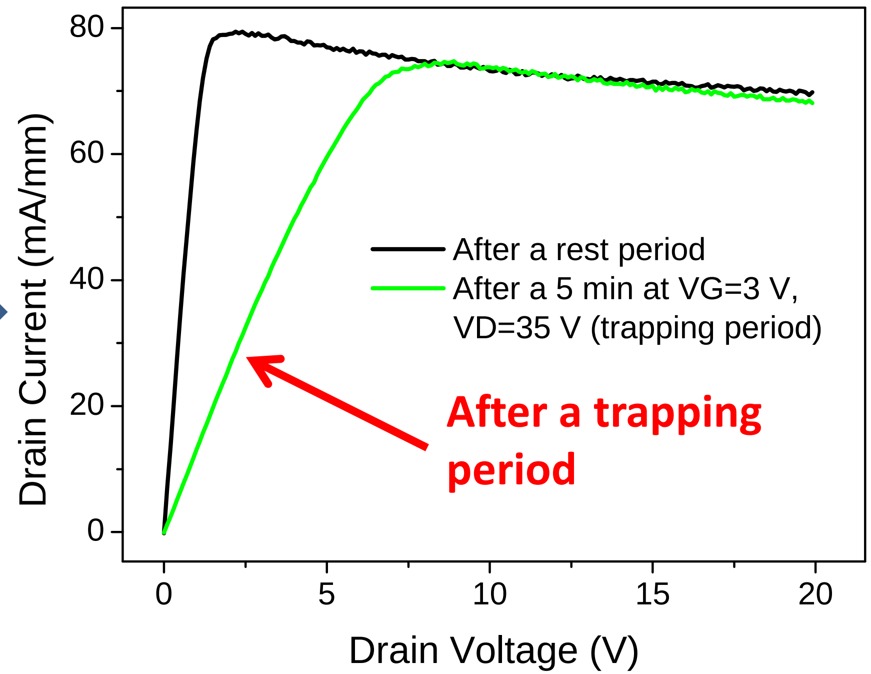
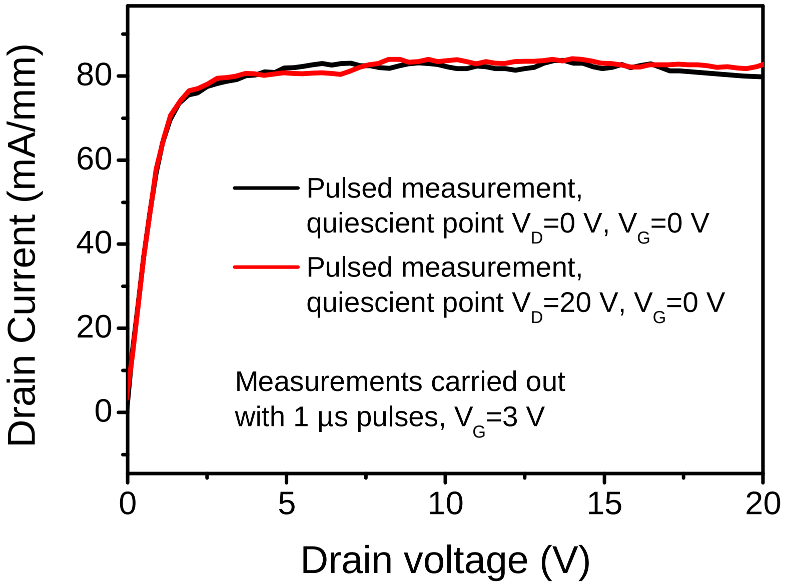


Trapping phenomena at high V_{DS} levels



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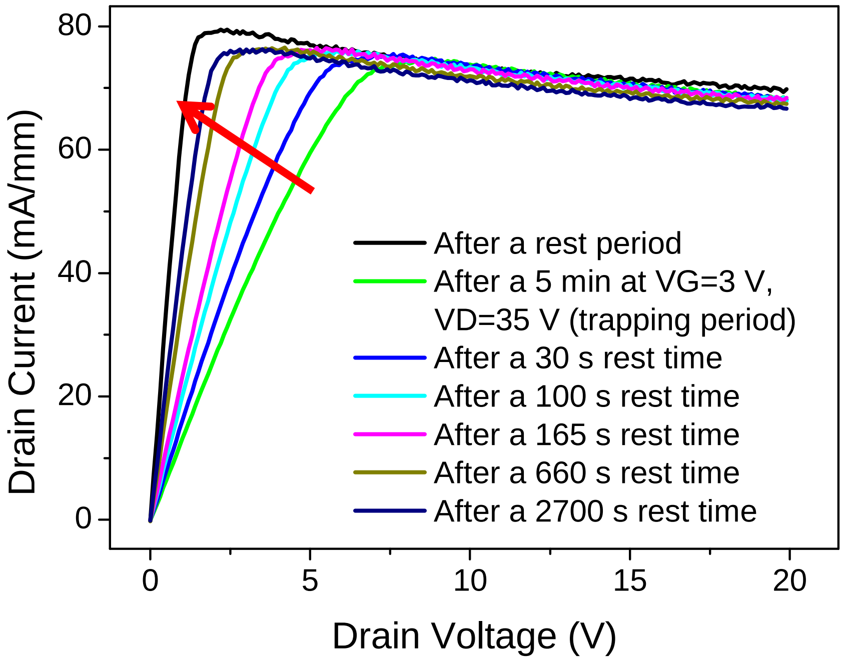
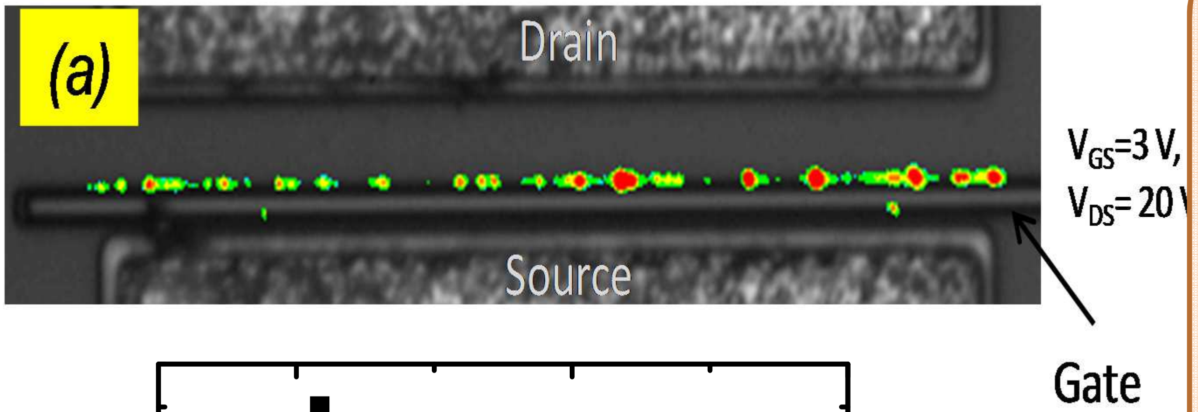
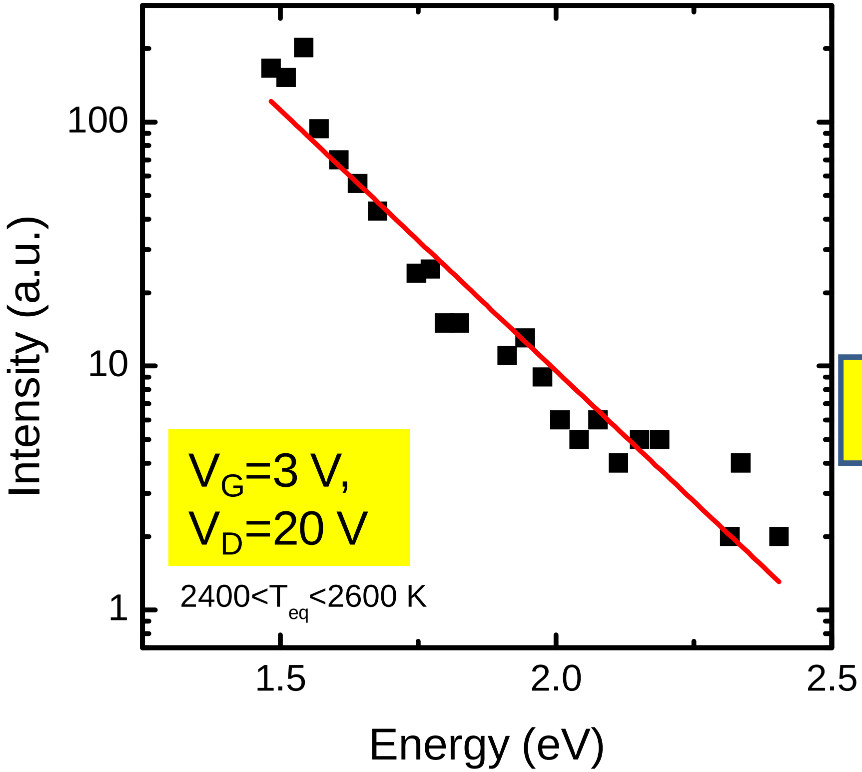
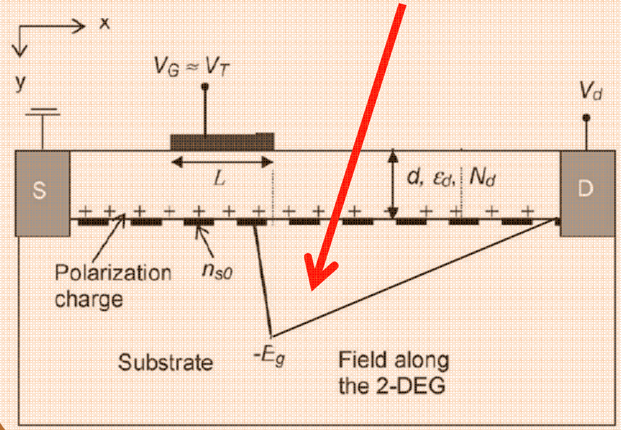


Further insight → Time-resolved EL measurements





•EL Signal is localized at the drain edge of the gate, i.e. where the electric field is maximum



EL spectra have Maxwellian shape → Hot electron emission, due to Bremsstrahlung (deceleration of carriers, accelerated by the high GD field)

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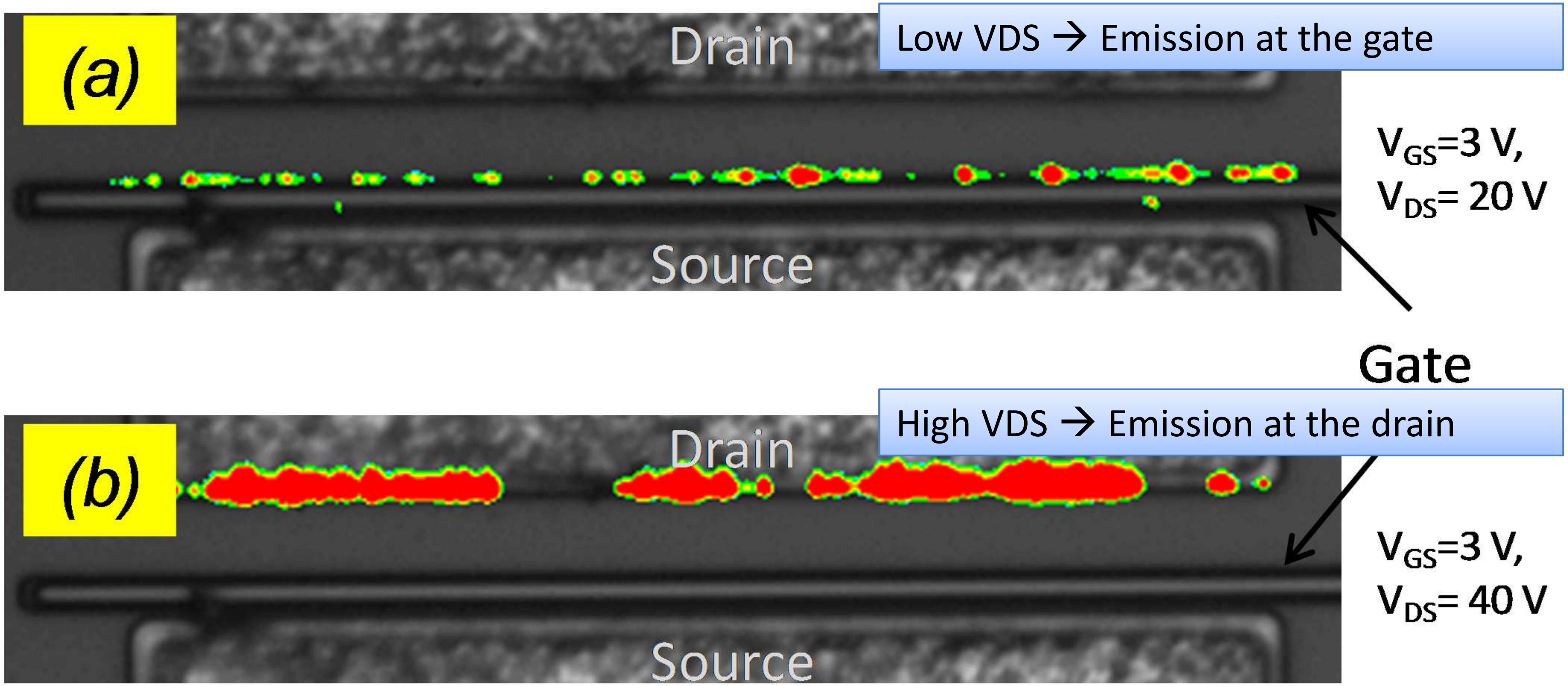
Further insight → Time-resolved EL measurements



At high drain bias → EL signal moves to the drain and significantly increases in intensity → EL peak moves from the gate to the drain → Negative charge trapped in the GD access region (virtual gate)

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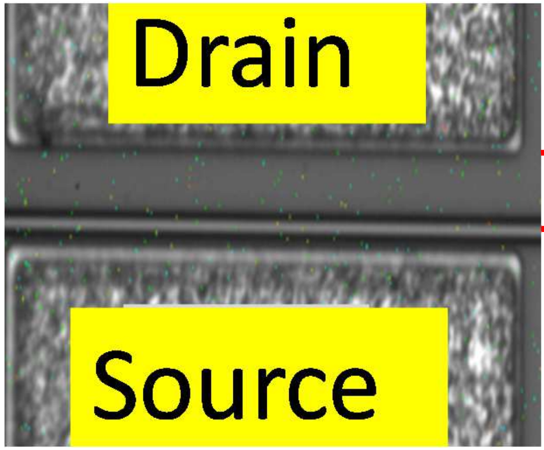
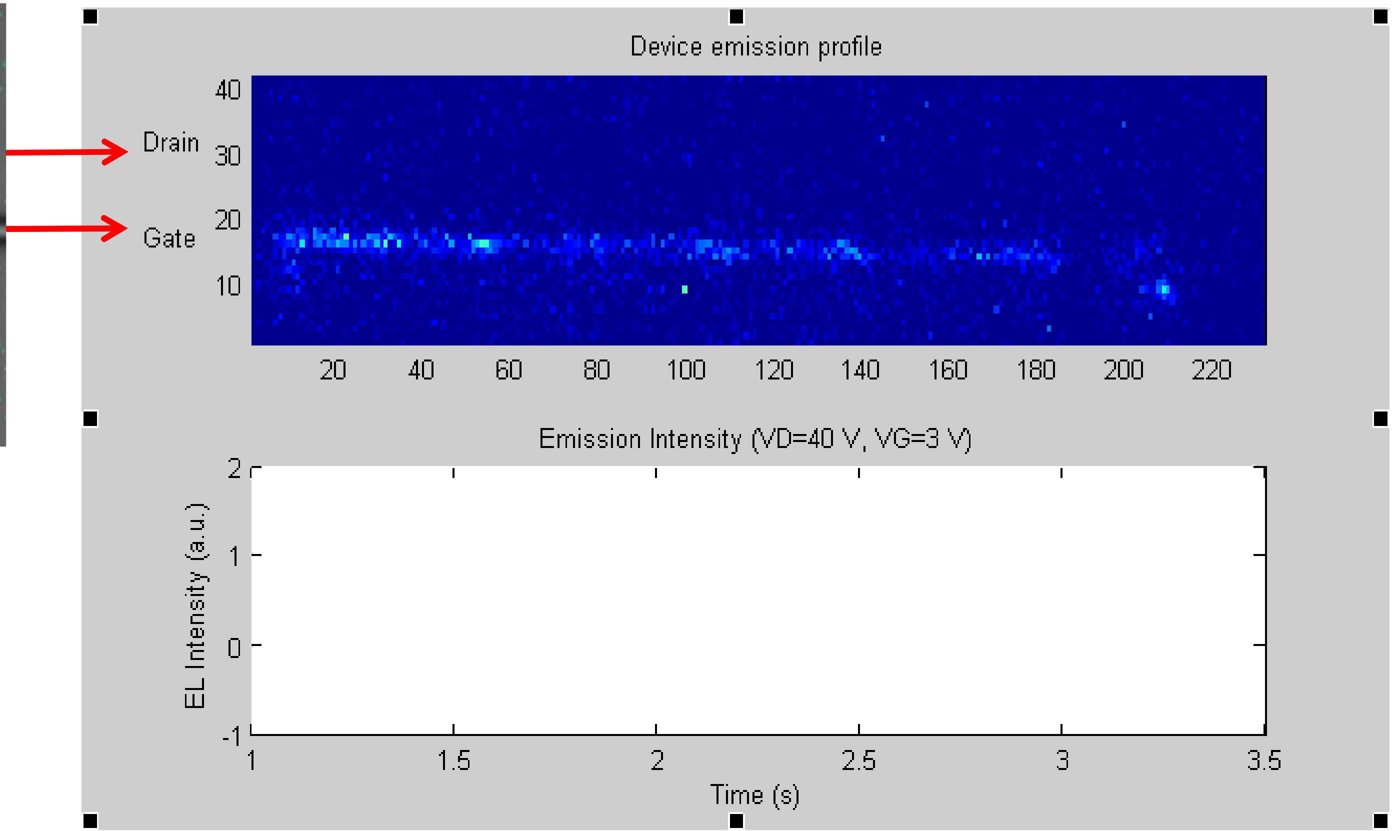
Further insight → Time-resolved EL measurements



Emission "movie" recorded during operation at VG=3 V, VD=40 V



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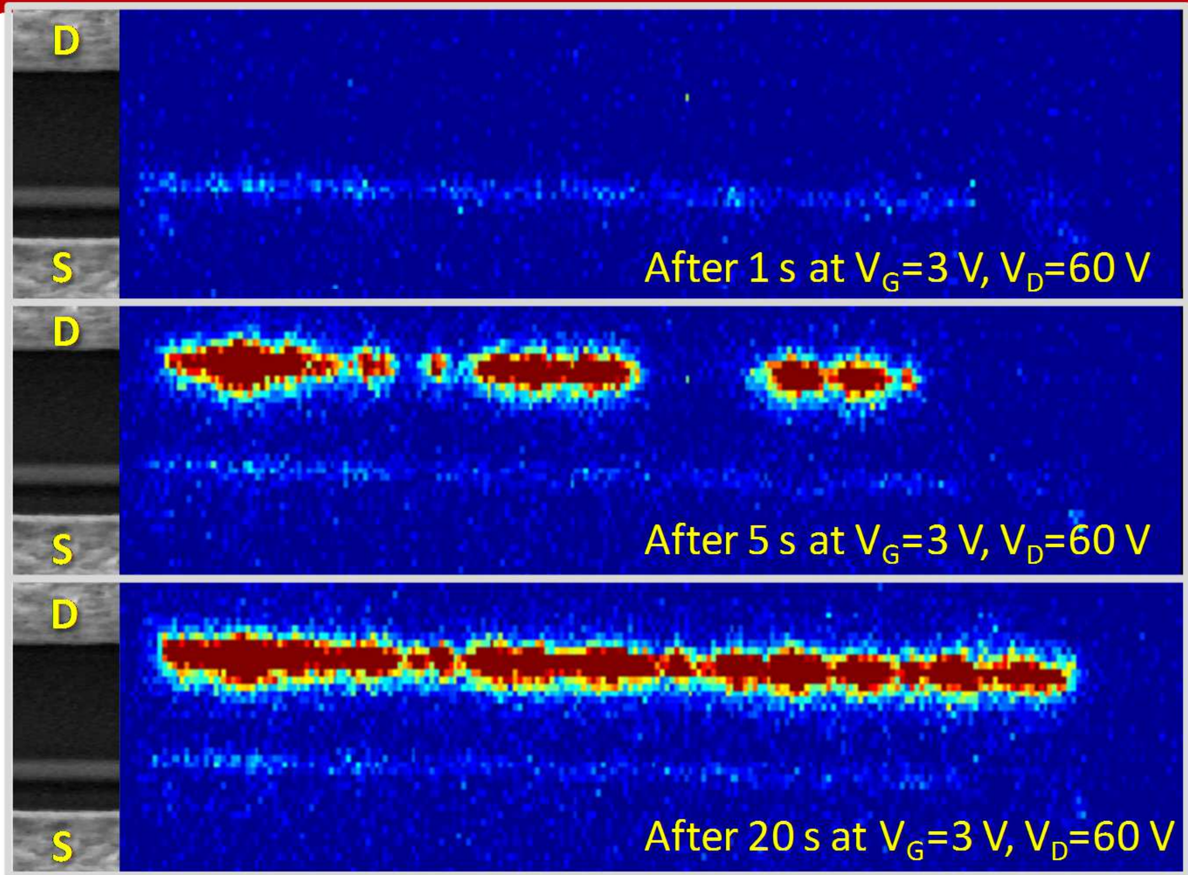
Further insight → Time-resolved EL measurements



•The onset of drain luminescence is not immediate → **After a certain delay time (t_d), EL intensity suddenly increases, and the signal moves towards the drain**

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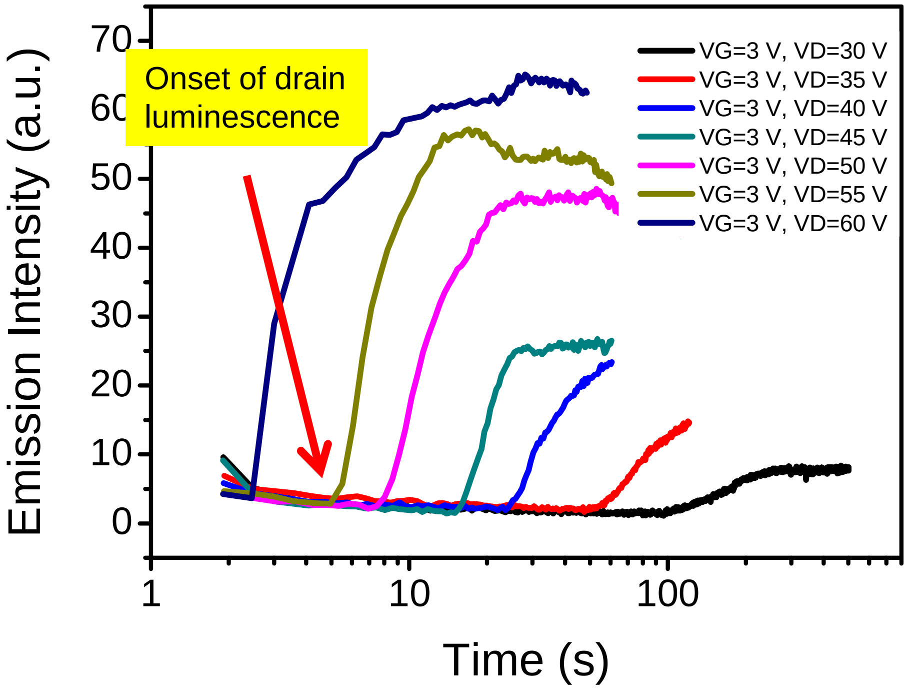
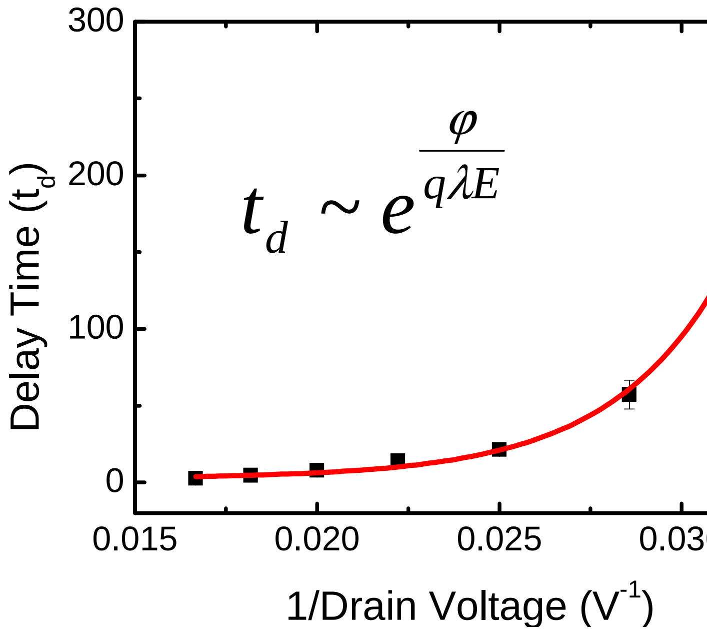
t_d strongly depends on applied drain voltage



t_d strongly depends on gate-drain field: at higher gate-drain field, t_d is shorter, indicating that the trapping rate depends on the gate-drain voltage difference



A simple model was developed to explain the experimental results: e^- are accumulated according to the lucky-electron model → When enough charge is injected into the device (after a delay time t_d), virtual gate effect takes place → Emission moves towards the drain

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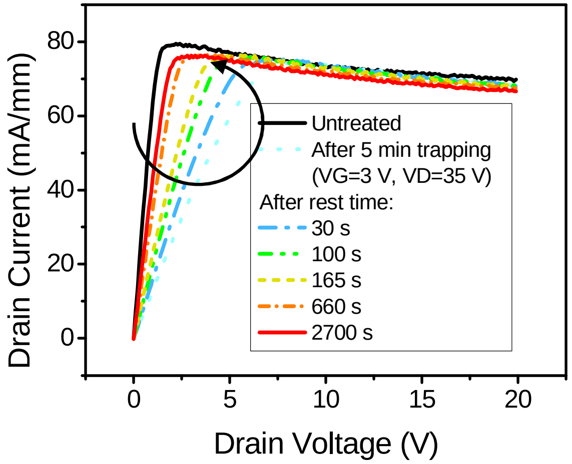
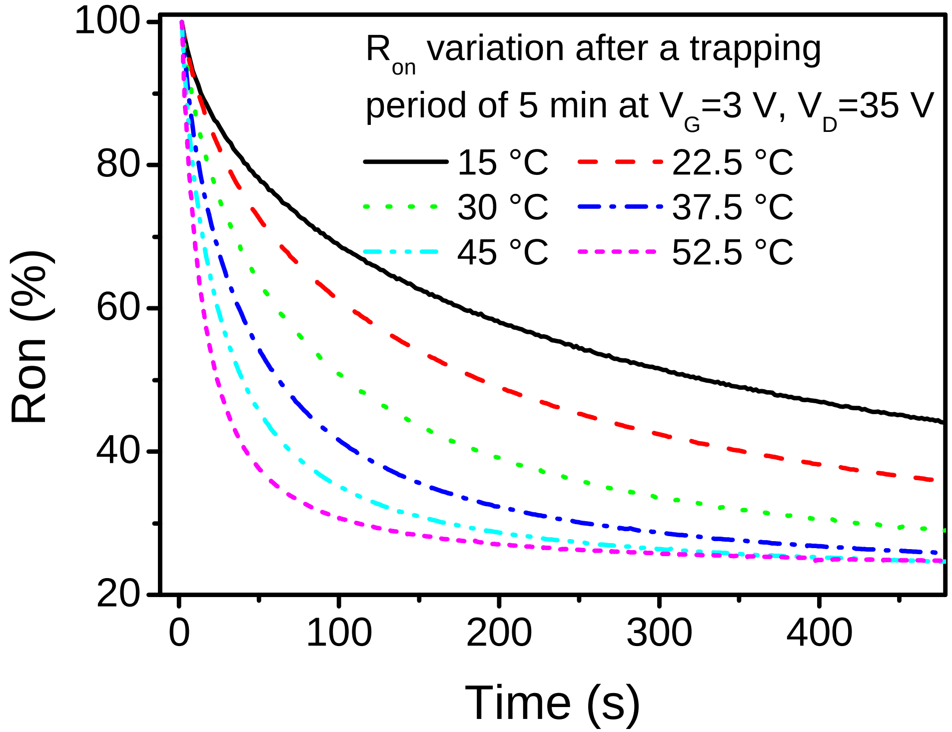
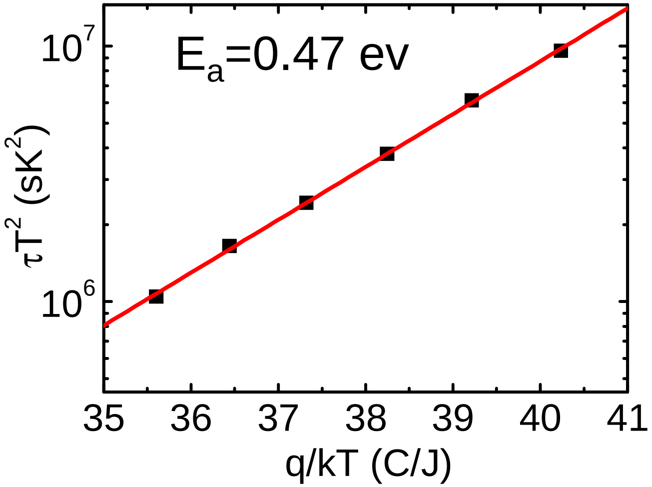
Characteristics of the recovery process





Recovery of Ron is temperature dependent → Thermally activated process



Activation energy for de-trapping process is 0.47 eV → **Mid trap level located in the gate-drain access region (since no variation of the threshold voltage is detected)**

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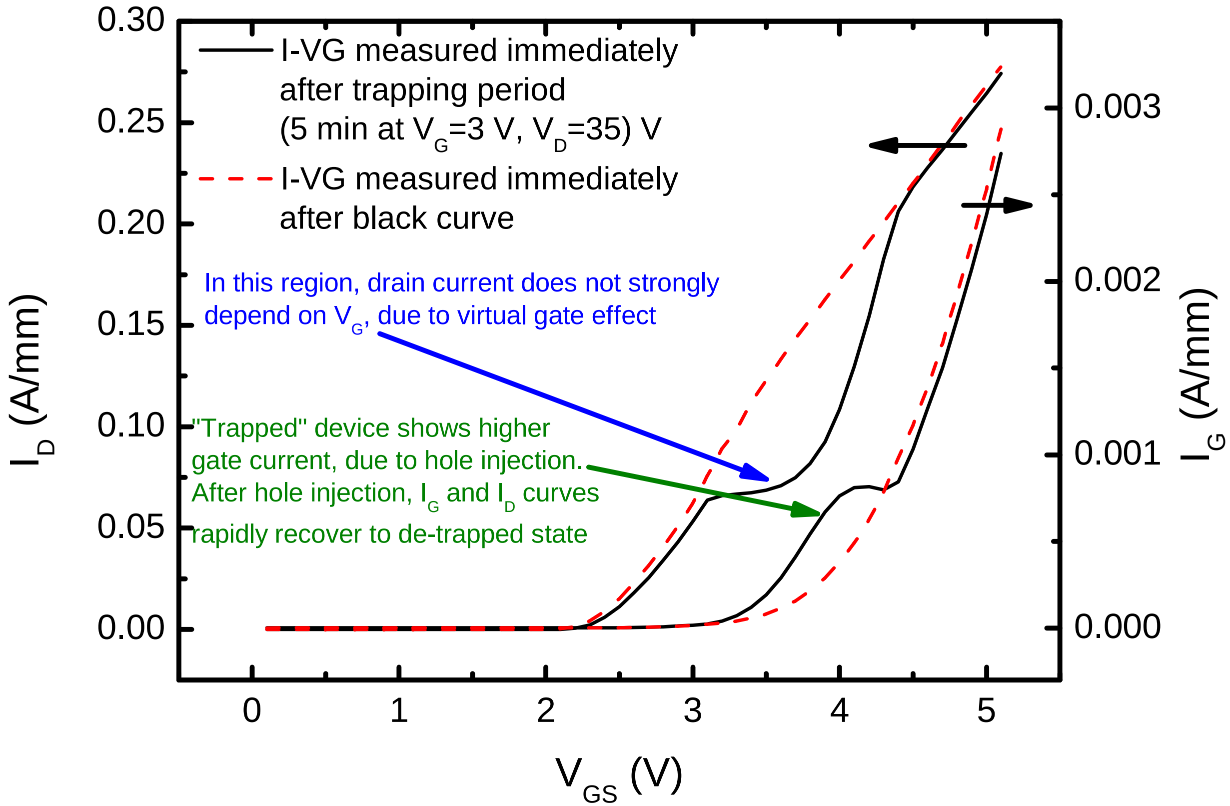
De-trapping induced by the injection of holes



- De-trapping can be significantly accelerated through the injection of holes from the gate
- The simple execution of an I_D-V_G measurement can lead to a remarkable recovery of the initial drain current levels, due to a stronger injection of holes which is recognizable from a bump in the I_G-V_G curve

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De-trapping induced by the injection of holes

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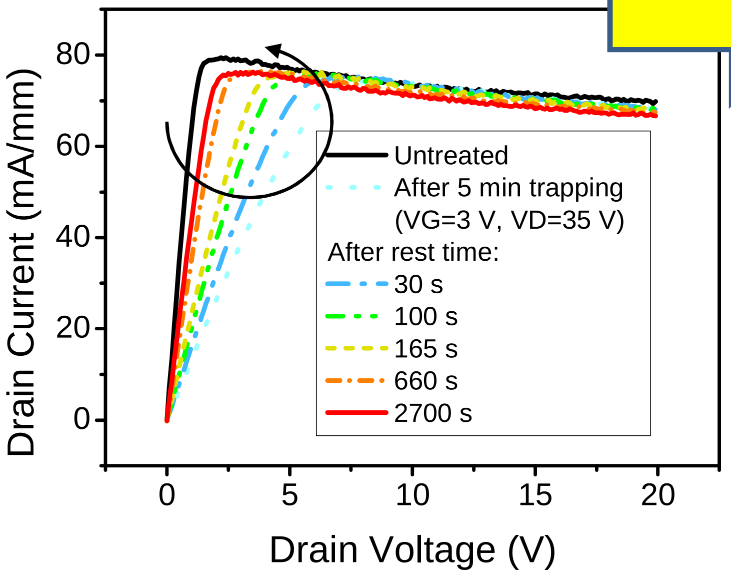
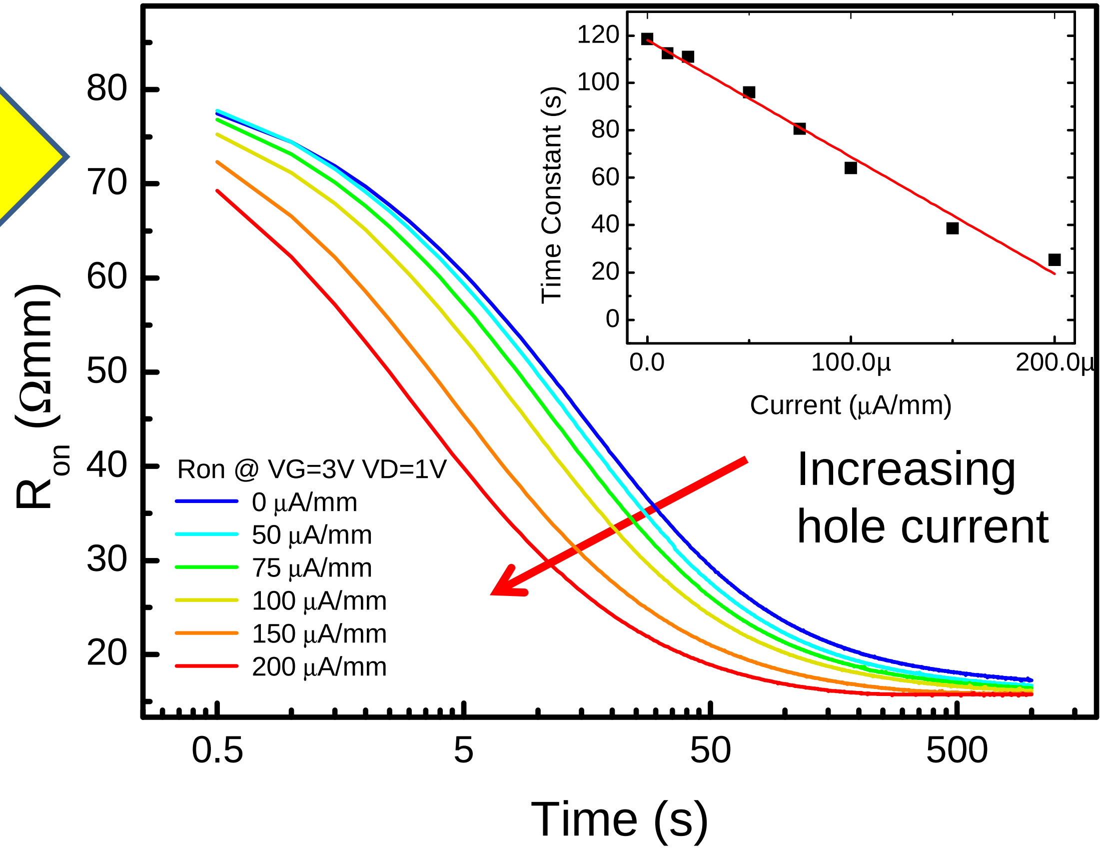
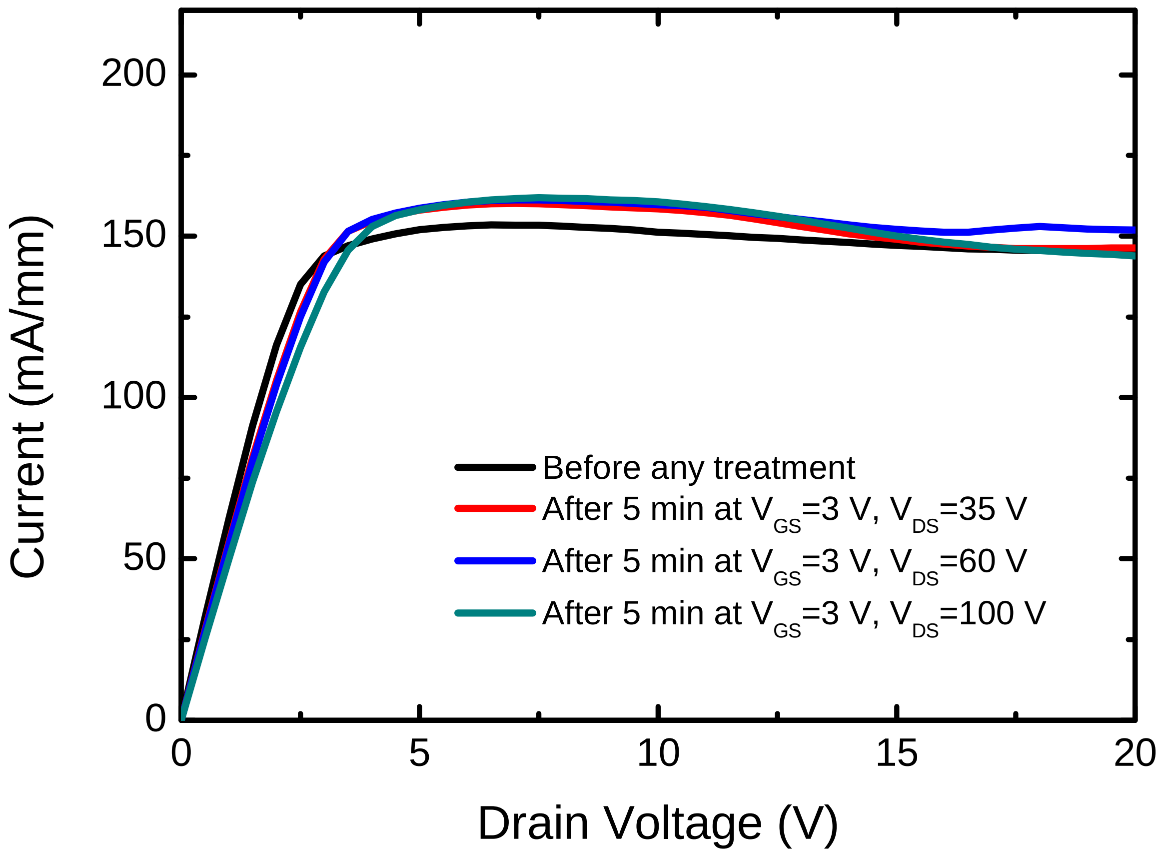




Time constant of de-trapping was found to decrease linearly with injected gate current, confirming the role of hole injection in reducing the measured virtual gate effect

Results on improved devices



DC I_D-V_D characteristics measured (with V_G=3 V)

- before any trapping
- after a 5 min trapping period at V_{GS}=3 V, V_{DS}=35 V
- after a 5 min trapping period at V_{GS}=3 V, V_{DS}=60 V
- after a 5 min trapping period at V_{GS}=3 V, V_{DS}=100 V

Within this work, trapping problems were eliminated through optimization of buffer and surface properties, and the addition of a field plate. Improved devices can withstand a V_{DS} level of 100 V in **ON-state**, without any trapping effect

Conclusions

With this paper we have demonstrated that:

(i) even if the current collapse of GITs is very low, exposure to long-term operation with high drain bias leads to a significant but recoverable increase in on-resistance. Activation energy of the detrapping process is 0.47 eV.

(ii) Several findings suggest that **R_{on} degradation should be ascribed to charge trapping in the gate-drain access region**

- **No shift in the threshold voltage** was found
- At high drain bias, **electroluminescence emission moves towards the drain contact**
- **the onset of drain luminescence, is not immediate**, but takes place at a certain delay time (t_d) after device turn-on. **t_d strongly depends on applied gate-drain field**

The observed increase in on-resistance and the onset of drain luminescence were ascribed to a field-dependent trapping process: the presence of a delay-time for trapping was modelled by assuming **that trap charging rate depends on gate-drain field**

(iii) **In GITs, charge de-trapping can be induced** by UV illumination, or **by the injection of holes** in the channel (the last solution is not possible in power HEMTs, and this makes GITs intrinsically more robust to trapping)

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