University of Padova,
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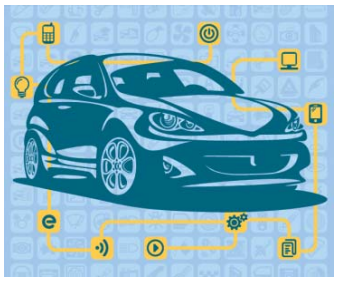
2015 Summer School of Information Engineering

ICT for Automotive Industry



Bressanone (BZ), Italy
July 5 – 11, 2013

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Automotive Smart Power IC Design

Bressanone / Brixen (BZ), Italy, July 8, 2015

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Hochschule Reutlingen
Reutlingen University

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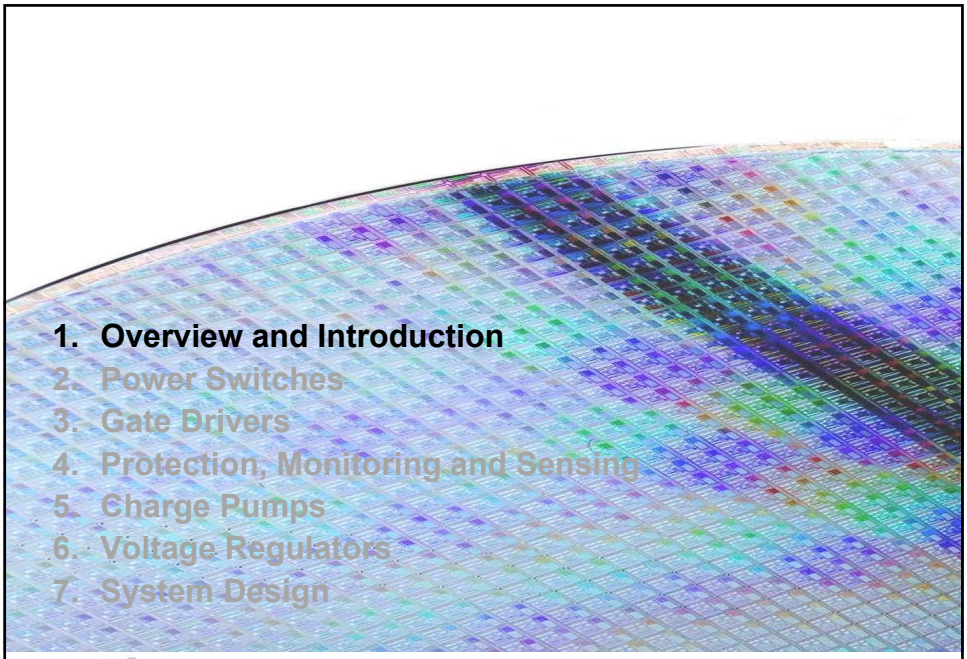
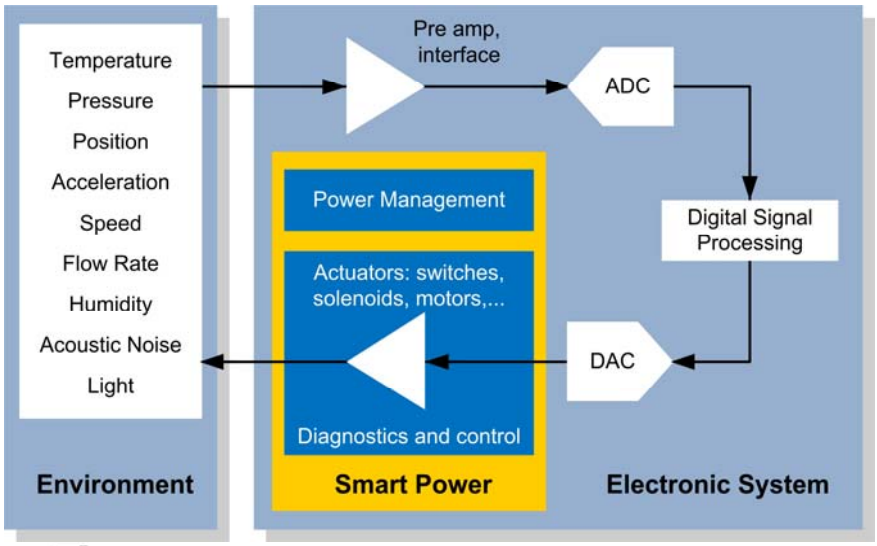
Outline

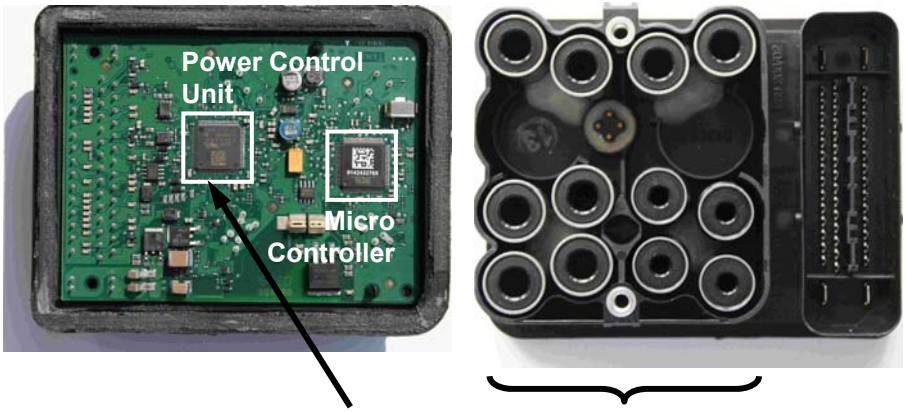


1. **Overview and Introduction**
2. Power Switches
3. Gate Drivers
4. Protection, Monitoring and Sensing
5. Charge Pumps
6. Voltage Regulators
7. System Design

Smart Power

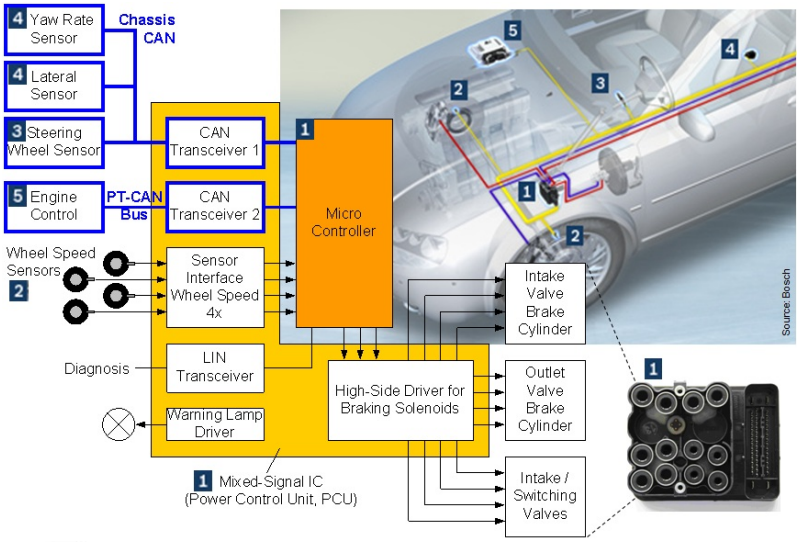


Example: Electronic Stability Program (ESP)



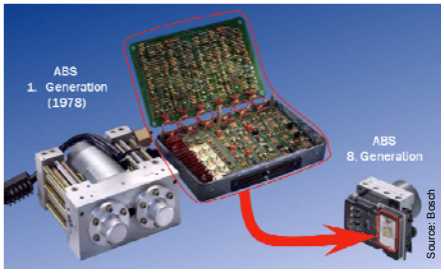
Power Control Unit contains integrated power FETs for 12 solenoids → 1-2A per solenoid (connected to car battery)

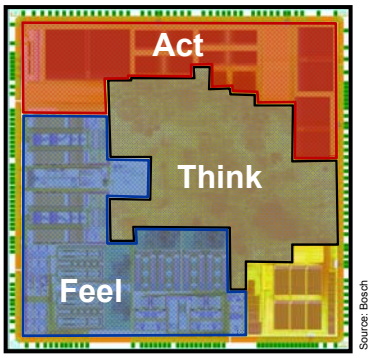
Example: Electronic Stability Program (ESP)



Smart Power

Smart Power = Integration of analog, digital und power on one single IC → Advantage: higher integration





One IC to replace multiple modules, additional monitoring and diagnosis functions → cost reduction, increased reliabilty, innovation through new functionality

Smart Power

Smart Part	Power Part
Over temperature Short circuit Open load Over voltage Under voltage Current limiting Load dump protection Control Loops (e.g. PWM)	High-voltage nmos / pmos High-side switch Low-side switch
Digital CMOS 1.8V, 3V MOS + bipolar Analog 1.8V, 3V, 5V	DMOS, Drain-extended MOS 5V, 12V,..., 80V and ~1A

Other technology features

- Buried layer or trench isolation
- Zener diodes, schottky and power diodes
- OTP memory, EEPROM, Flash memory

Mixed Signal Systems in Automotive

Power Train / Engine Control
- Sensor Signal Conditioning
- Transmission Control
- Fuel Injection Drivers
- Power Management

Dashboard
- LED Drivers
- Power Management

Body
- Window Lifter / Mirror Drivers
- Door Lock Solenoid Drivers
- Passive/Keyless Entry
- Relay Drivers
- Exterior Lightning (LED Drivers)




Safety Systems
- Airbag
- Passenger Recognition
- Adaptive Cruise Control
- Collision Avoidance

Chassis Systems
- ABS Controllers
- Vehicle Stability (ESP)
- Electronic Power Steering
- Collision Avoidance

Infotainment
- Performance Audio
- Navigation
- Power Management

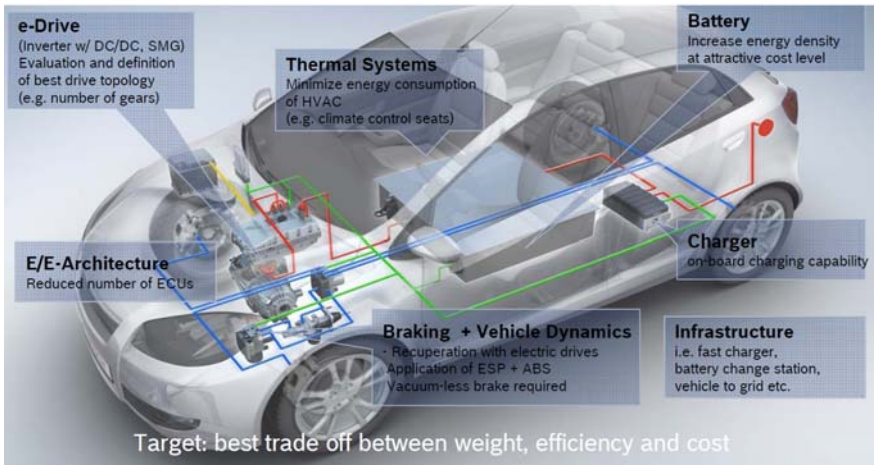
Energy Management
- Hybrid Vehicle
- Advanced Alternator System
- Motor Management

Vehicle Networking
- LIN
- CAN
- Flexray
- System Base Chips

Example: Engine Management

Source: Bosch

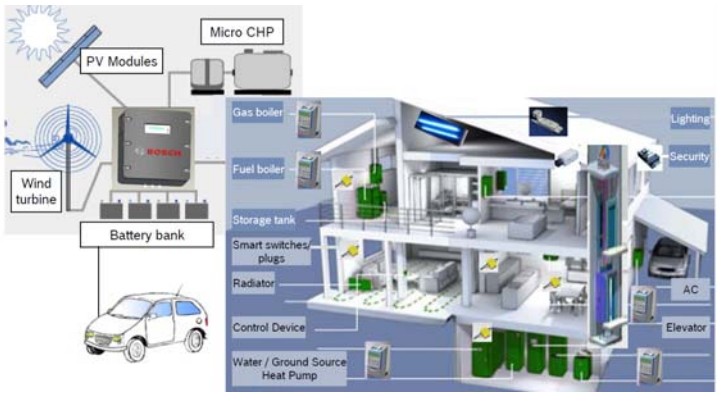
Electric Vehicle System



Source: Bosch

Smart Power – Future Markets

Smart Power ICs are enabler for growth areas like
smart home and voltage conversion from renewable energy



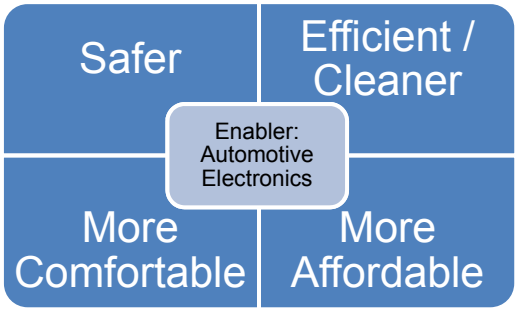
Source: Bosch

Automotive Trends and Drivers

Example: Driver Assistance
Park assist, blind spot detection, lane departure warning, night vision, adaptive cruise control, traffic sign recognition, object recognition

Example: Hybrid / Electrical vehicles
Start/Stop, battery monitoring, cell balancing, supercap management, DC/DC systems, inverter systems, charging solutions (including charging stations), fuel cells



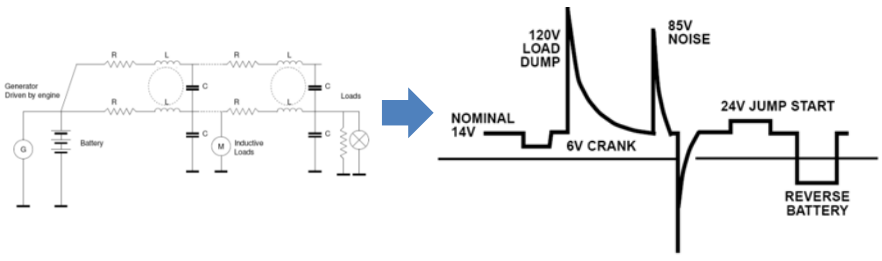


Example: Infotainment
Central entertainment unit, navigation, car audio, emergency call, WiFi, wireless USB, flash card slot, USB port, bluetooth

Example: Vehicle Safety
Emerging countries starting legislative agendas on vehicle safety → ABS, ESP

The Electrical Network in a Car

Voltage systems:
- Cars: 12V standard (battery peak power: 10kW!)
- Truck: 24V (=2x 12V in series)
- New solutions for hybrid or electrical cars: 12V, 48V + HV

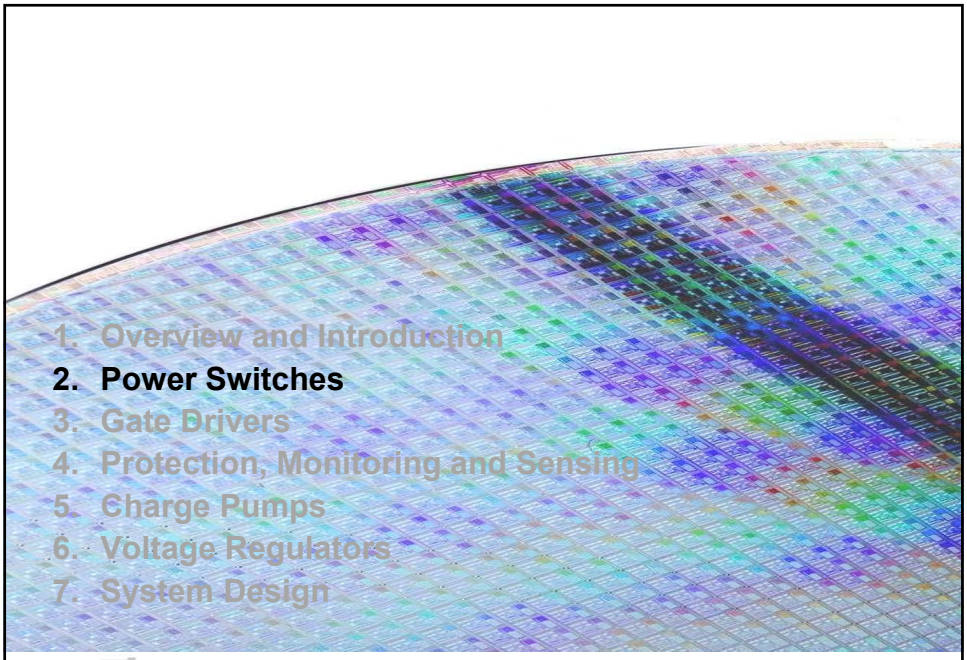


The battery line noise is modeled by ISO test pulses (also known as Schaffner pulses), defined by ISO 7637-2

Automotive IC Operating Conditions

Typical Device Ratings

	Minimum	Maximum
Supply voltage	4 - 6V	16 - 25V
Transient on supply	36V	60V
Reverse battery protection		-14V
Quiescent current		1 - 5µA
ESD strike (HBM)		2 - 6kV
Ambient temperature	−40°C	125°C
Junction temperature	−40°C	>150°C



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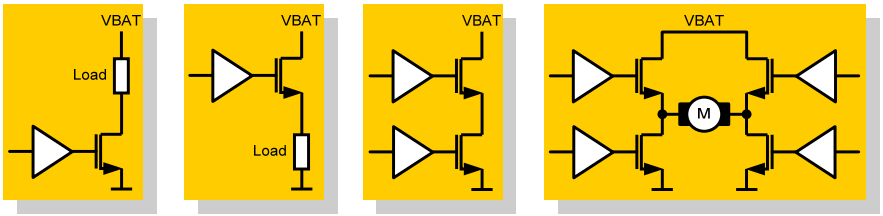
Power Transistor Switches & Drivers

Low-Side | High-Side | Half-Bridge | Full or H-Bridge



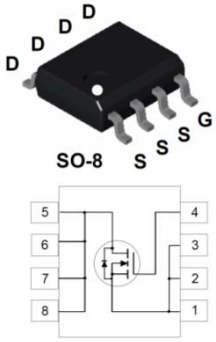
- Transistors can be on-chip (integrated) or discrete (external)
- Most applications use n-type transistors due to lower on-resistance R_{DSon}

Applications:

- Motor Control
- Switched Mode Supplies
- Valves / Solenoids
- Relais, Warning Lamps, LEDs

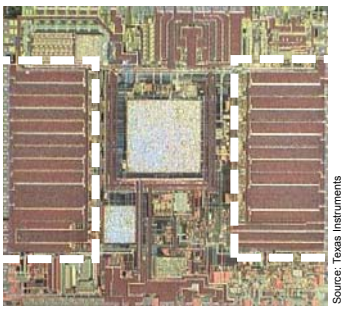
Power Transistors

Discrete Power FET (external component)



On-resistance ~ 10...100mΩ
Drain Currents > 1...10A

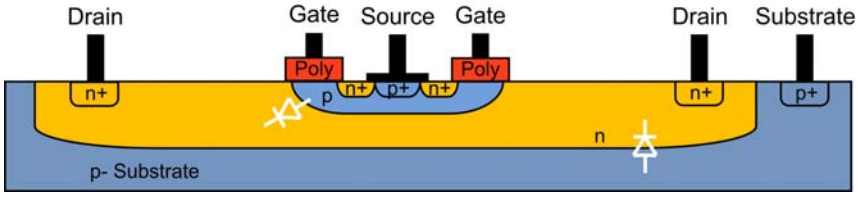
Integrated power FET in High-Voltage BiCMOS Technologies



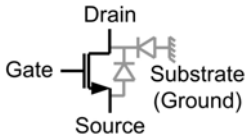
On-resistance < 1Ω
Drain Currents < 1...2A
FET types for > 60V available

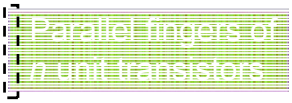
Power MOSFET = DMOS

DMOS = Double Diffused MOS (lateral oder vertical)



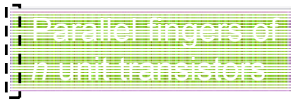
- Low on-resistance R_{DSon} (< 1Ω, 1-2A), large V_{DSmax}
- Source and Gate isolated from Substrat → negative voltages possible
- Parasitic Diodes D-S and D-SUB
  → have to be taken care of
  → can be utilized as free-wheeling or power diode





Power Transistor Sizing

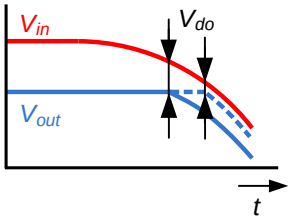
- Design *W*/*L* for targeted R_{DSon} (over all corners!)
- Switch = Triode-Region → *W*/*L* and V_{GS} determine R_{DSon}
- Trade-off between area and R_{DSon}
  e.g. R_{DSon} = 0.5Ω → *W*/*L* = 200·(450µm/1.8µm) → (0.5 x 1.5)mm²
- *W* and *L* define gate capacitance
  → to be (dis-)charged during switching → C_{gate} ~ 0.1...1nF



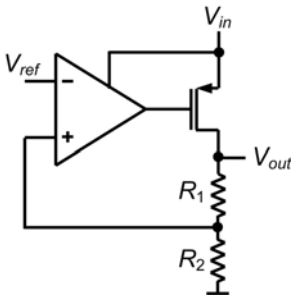
Power Transistors: Dropout

Dropout V_{do} (i.e. R_{DSon}) determines W/L and drives decision for pmos or nmos

Smaller dropout extends battery lifetime

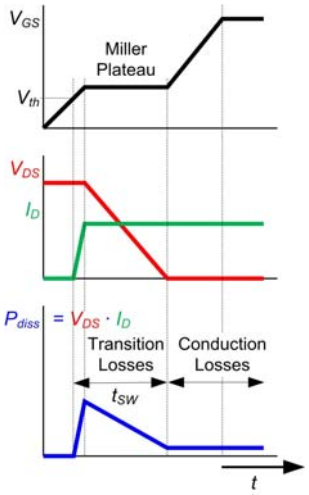


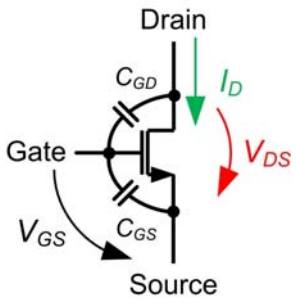
Example: Linear voltage regulator



Transistor Switching Behavior and Losses

For inductive loads:





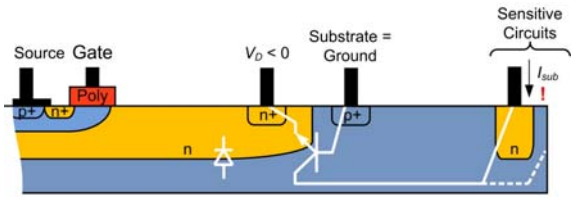
Example:
V_{GS} = 8V
V_{th} = 2V
I_D = 0.5A
R_{DSon} = 0.5Ω
V_{DS} = 12V
t_{sw} = 100ns
f_s = 500kHz

Transition Losses:
$0{,}5\ V_{DS}\ I_D\ f_s\ t_{sw}$ = 150mW

Conduction Losses:
$I_D^2\ R_{DSon}$ = 250mW

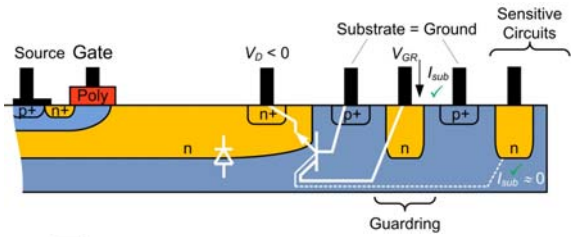
Parasitic Effects

For $V_D < 0$ substrate currents though parasitic npn:



Consequence:
- Disturbance of other circuits blocks
- Debiasing, latch-up

Countermeasure: Guardrings (GR) around the LDMOS



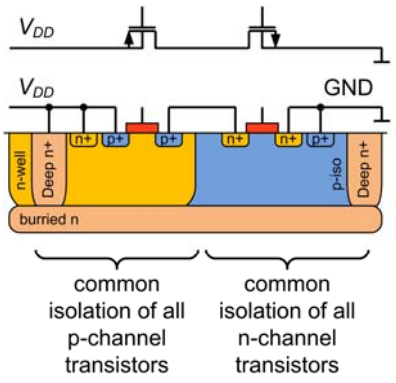
GR around every drain which goes to an IC Pin

Drawback: Layout area → cost!

Isolation of Circuit Blocks

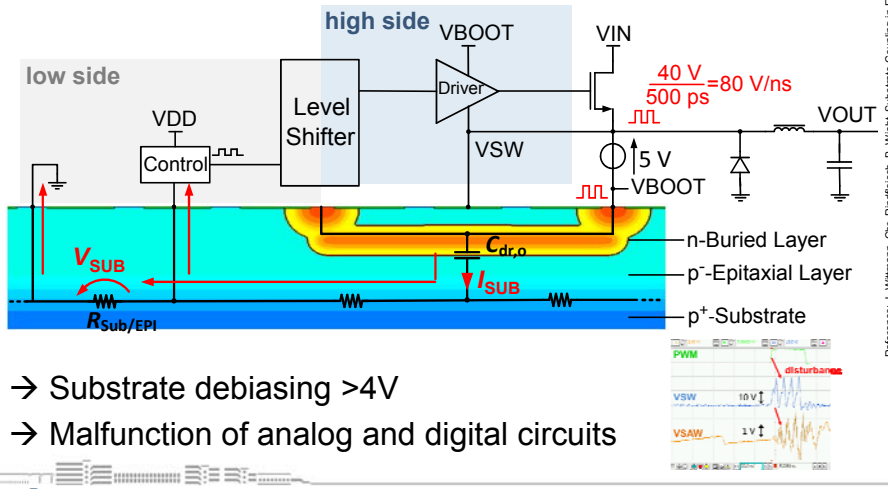
Every circuits block can be placed in isolation
→ Shielding against substrate noise coupling
→ similar to guardring with full “incapsulation” (also at bottom)

Rule for smart power designs: Isolate every circuit block if possible



Substrate Coupling

Voltage slopes > 10V/ns cause capacitive charging currents in the order of 100mA on IC-level during transition



→ Substrate debiasing >4V

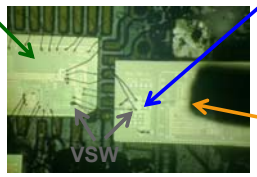
→ Malfunction of analog and digital circuits

Reference: J. Wittmann, Chr. Rindfleisch, B. Wicht, Substrate Coupling in Fast-Switching Integrated Power Stages, ISPSD 2015

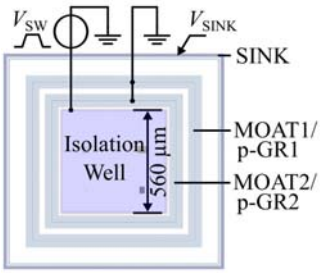
Substrate Coupling: Experimental Results

MHz-Converter

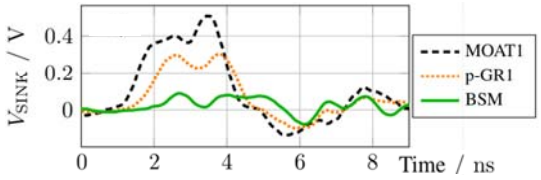
Test chips with / without BSM



Test chip layout



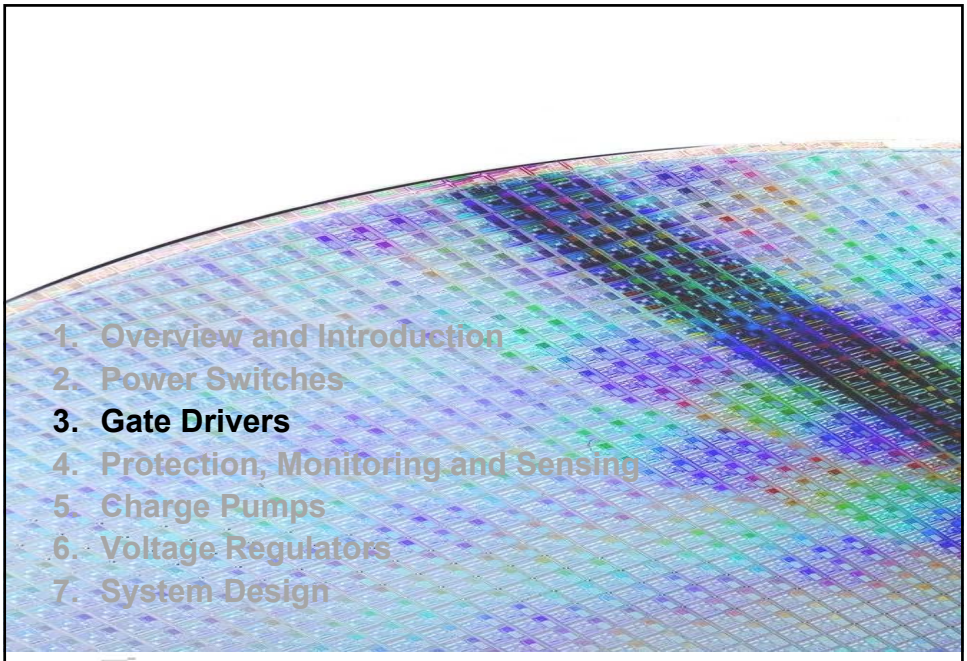
Measured disturbance at 40V/ns:



• Back-Side Metallization (BMS) reduces coupling by ~100%

• p-Guardring is less efficient but readily available

Reference: J. Wittmann, Chr. Rindfleisch, B. Wicht, Substrate Coupling in Fast-Switching Integrated Power Stages, ISPSD 2015



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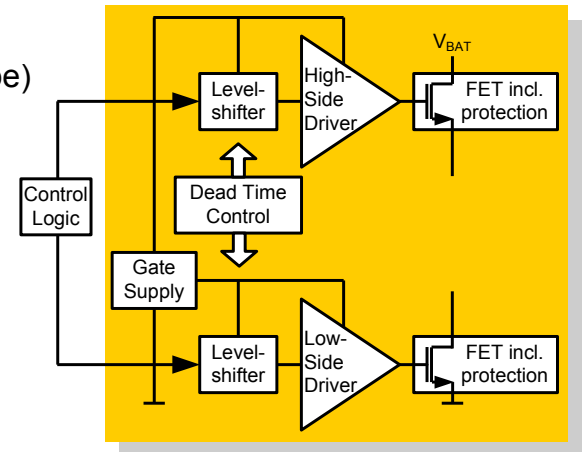
Gate Driver Block Diagram and Circuits

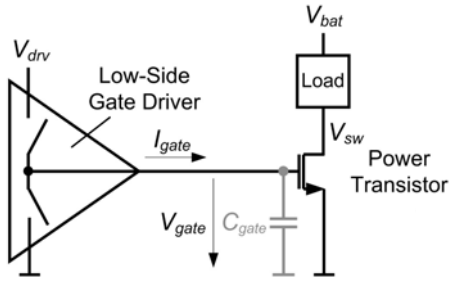
Main circuit blocks:
- Power FET (n/p-type)
- Protection
- LS / HS Driver
- Levelshifter
- Gate supply
- Dead Time Control (only for bridges)



Low-Side Driver

Function: Turn-on/off power switch with sufficient gate overdrive (voltage) and appropriate driving capability (current over time)

Principle:

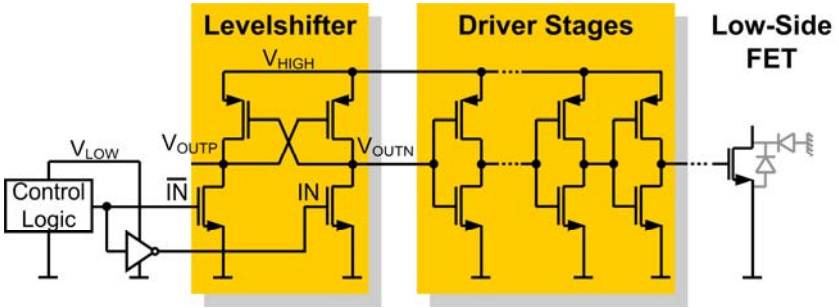


V_{drv} defines the gate-source voltage of the power transistor

Parameters:
- Gate driver sink / source resistance (at given I_{gate})
- Sink / source peak current

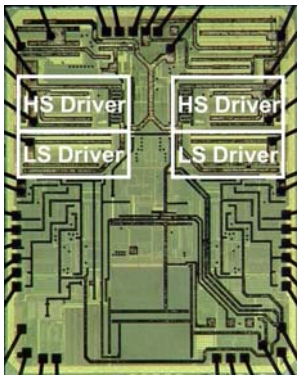
Low-Side Driver

Circuit structure:

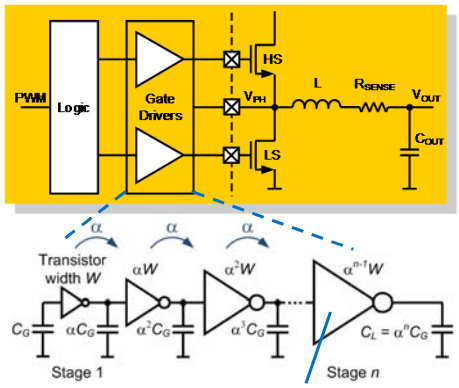


- Levelshifter followed by driver stage(s) (“CMOS inverter”)
- Single driver stage if small power FET (low C_{gate})
- Cascaded driver stages if large power FET (large C_{gate})

Practical Implementation of Gate Drivers



Reference: S. Herzer, B. Wicht et al., ESSCIRC 2009



Driver resistance: 3Ω
Driver peak current: 1.5A

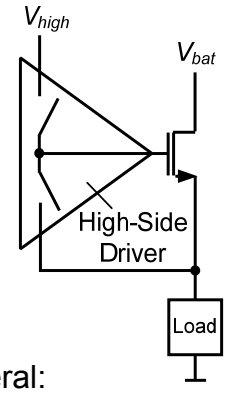
W/*L* = 32000µm / 2.5µm

15ns delay at C_{gate} = 10nF

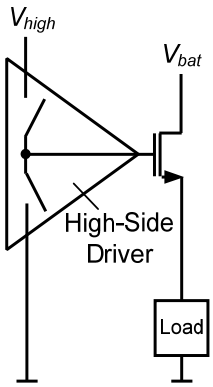
Optimization for speed, power, area: *n* stages, each increasing in driver strength (*W*/*L*) by Faktor α

High-Side Driver

Type 1 Floating Driver



Type 2 Referred to GND

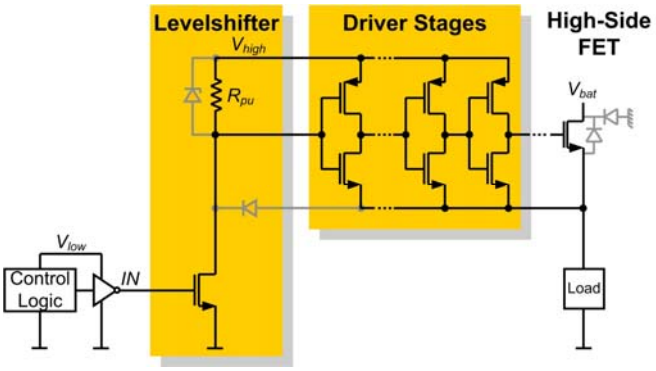


General:

- Overdrive needed → $V_{high} = V_{bat} + V_{GS}$
- V_{high} from charge pump, boost converter, bootstrapping

High-Side Driver

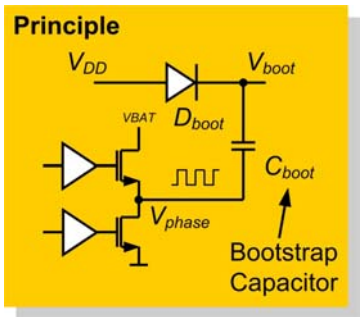
Example for floating driver (Type 1)

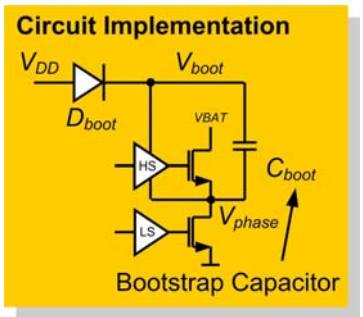


- Driver stage: Low voltage transistors even for 60V V_{BAT}
- R_{pu}: Tradeoff between speed and DC current (typ. 100kΩ)
- Diode(s) to clamp voltage across R_{pu} and limit V_{GS} for driver

High-Side Gate Supply: Bootstrapping

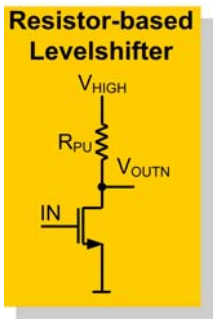
Similar to charge pump with oscillator replaced by bridge

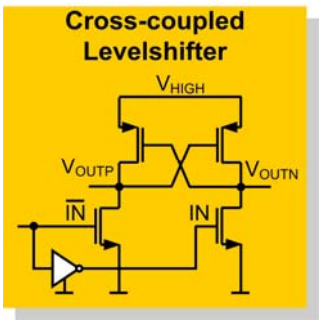


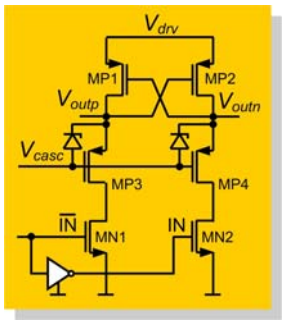


- C_{boot} supplies high-side driver → $V_{boot} = V_{BAT} + V_{DD} - V_F$
- C_{boot} gets recharged if high-side is off (low-side on, V_{phase} = 0V) from V_{DD} through bootstrapping diode D_{boot}
- Sizing: $C_{boot} \geq \left(Q_{gate} + Q_{rr} + I_{boot}/f_{sw}\right)/\Delta V_{boot}$

Levelshifters







Reference: Moghe et al., Nanosecond Delay Floating High Voltage Level Shifters ..., JSSC Feb. 2011

- DC current
+ Simple, small
+ Default state

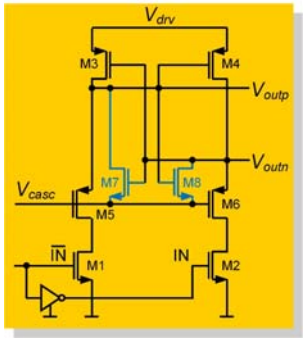
+ No DC current from V_{HIGH}
- Slow and large area
- No default state

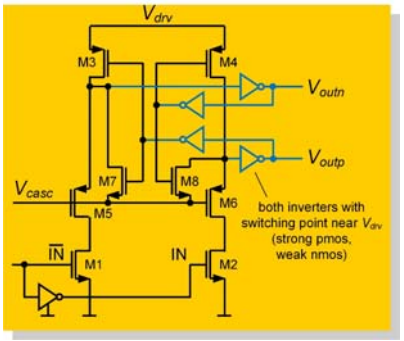
High-voltage version with cascodes

Advanced levelshifters combine advantages of both (often with capacitive coupling), bus protocol to save # of levelshifters

Cross-coupled Levelshifter with Full HS Swing

V_{SG} of cascodes M5, M6 prevents logic '0' level at driver input → full high-side swing achieved by active clamping → M7, M8

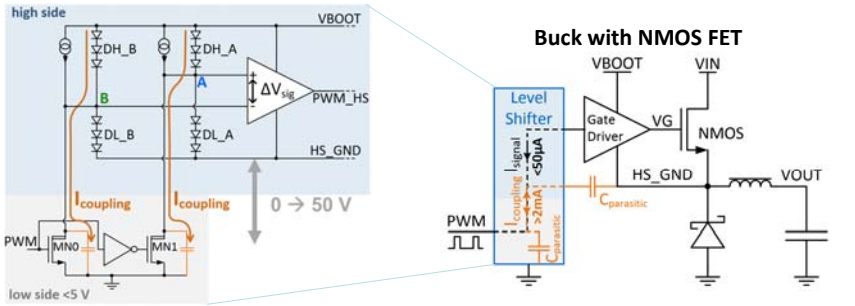


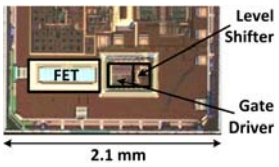


Reference: Moghe et al., Nanosecond Delay Floating High Voltage Level Shifters ..., JSSC Feb. 2011

Insertion of inverters in cross-coupling (right) → increased loop gain → faster switching and reduced power consumption → M7, M8 can become minimum size

50V High-Speed dv/dt Robust Levelshifter



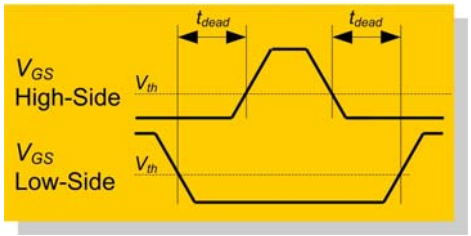


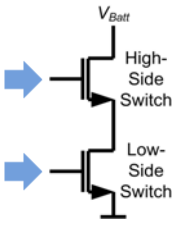
- Minimum pulse width < 3 ns
- 5 ns propagation delay
- Robust against transitions >20 V/ns:
  No incorrect switching at >2 mA coupling currents

Reference: J. Wittmann, Th. Rosahl, B. Wicht, "A 50V High-Speed Level Shifter with High dv/dt Immunity for Multi-MHz DCDC Converters", ESSCIRC 2014

Dead Time Control of HS / LS Drivers

To avoid cross-conduction of HS and LS FET (damage!):
Turn off FET → then turn on FET with dead time in between





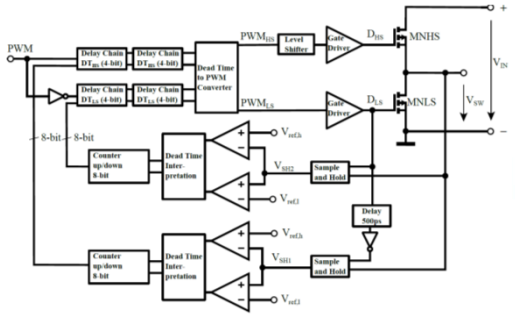
Typical t_{dead}:
10ns for SMPS (f_{sw} = 500kHz)
>1µs for Motor Control (f_{sw} = 20kHz)

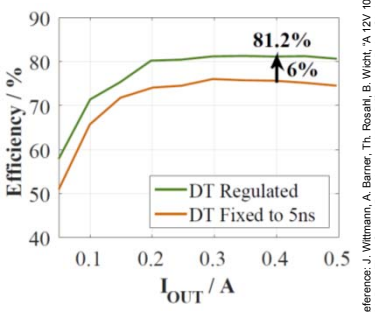
Methods:

- Constant delay: Simple, but worst case margin → large t_{dead}
- Adaptive delay: Sensing of off-state → then turn on other FET
- Predictive delay: Cycle-by-cycle control by sensing LS body diode or switching node → good performance, but complex

Synchronous Buck with Dead Time Control

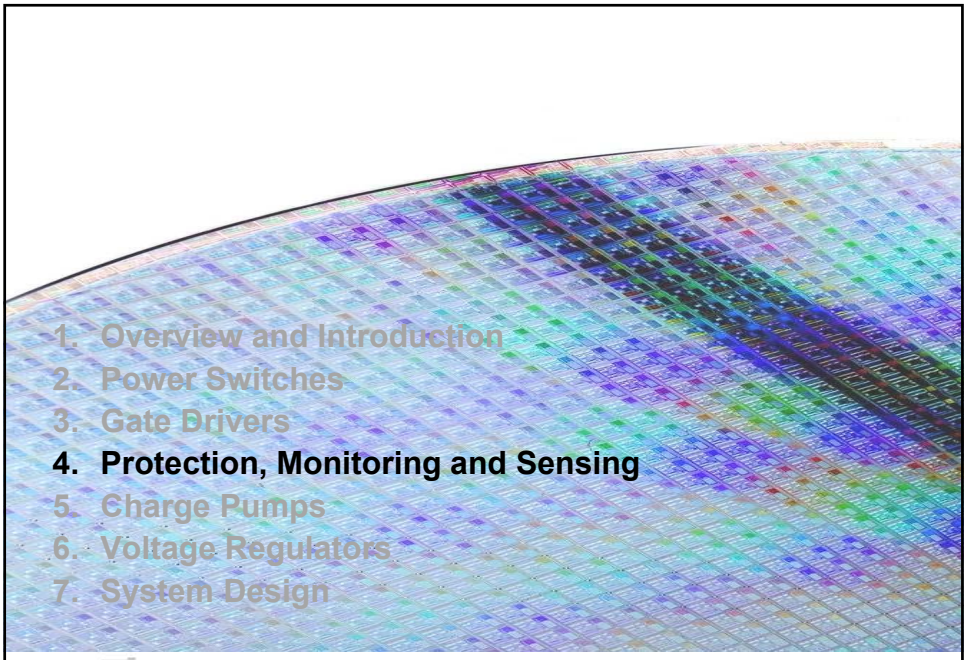
Vin = 12-18V, 10 MHz buck converter with predictive mixed-signal dead time control based on a 125 ps 8-bit differential delay chain





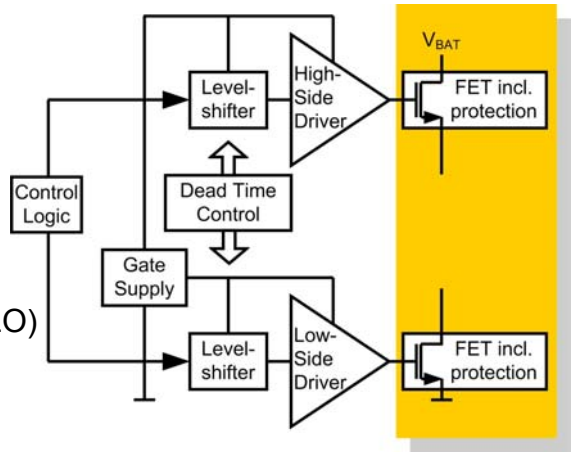
Reference: J. Wittmann, A. Barner, Th. Rosahl, B. Wicht, "A 12V 10MHz Buck Converter with Dead Time Control Based on a 125 ps Differential Delay Chain", ESSCIRC 2015

- No low-side body diode conduction
- Loss reduction of up to 30% → 6% higher efficiency at 10 MHz



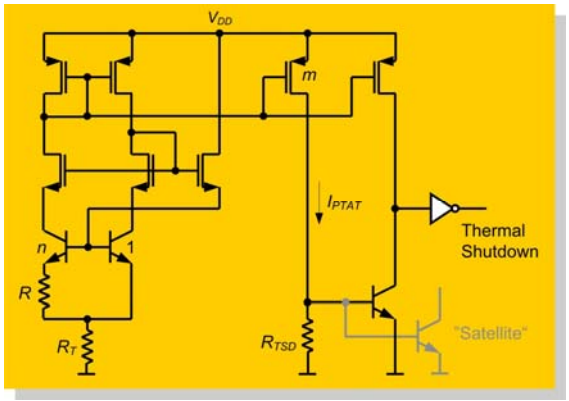
Protection and Diagnostics in Smart Power

- Thermal protection
- Over-voltage (VDS)
- Over-current
- Short-to-ground
- Short-to-battery
- Open load
- Under-voltage (UVLO)



Thermal Shutdown

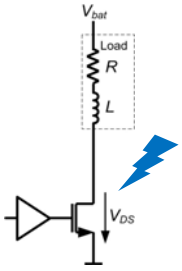
Protects the IC from damage at high temperature

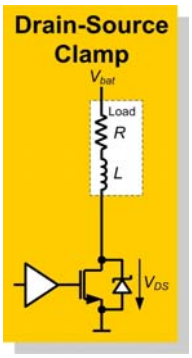


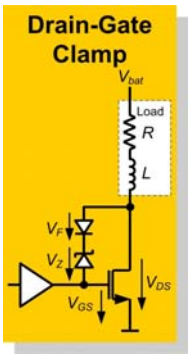
Usually installed as a secondary protection:
Indirect limitation of load current in regulators, drivers

Protection Schemes - Inductive Loads

Low-side and high-side switches: Zener diode based voltage clamps ensure $V_{DS} < V_{DSmax}$ when power switch is turned off







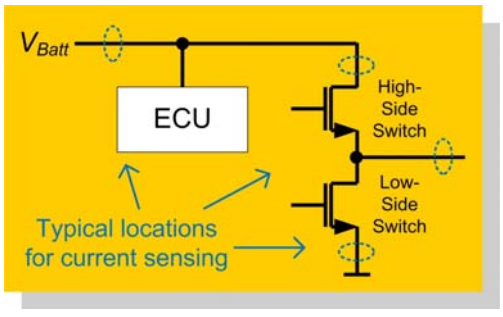
Similar schemes for high-side protection

Example:
$V_{DS} < 45...50V$
$V_{DSmax} = 55V$

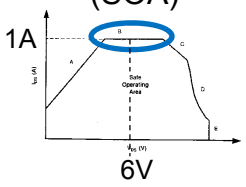
Zener diode dissipates all the energy from *L*

Preferred: FET dissipates energy from inductor

Over-Current Protection – Current Sensing



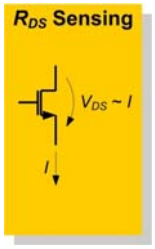
Safe Operating Area (SOA)



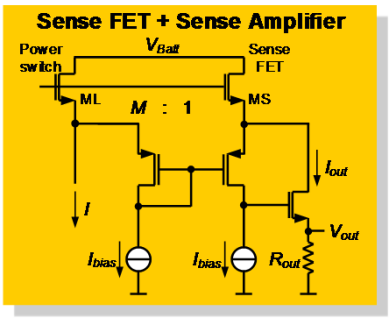
Open loop:
- Over-current detection → turn-off power FET
- Continuous current measurement

Closed loop:
- Current limit (example: LDO)
- Current controlled DCDC conversion

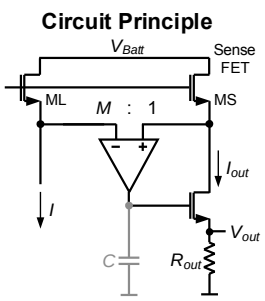
Current Sensing



+ Lossless
− Accuracy



+ Lossless
+ Good accuracy
− Complexity



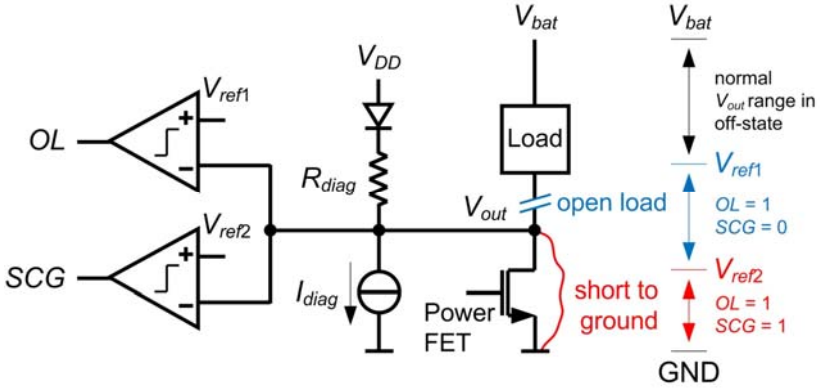
Accuracy depends on (1) mismatch in sense transistor ratio M, (2) amplifier offset and on variation of (3) R_{out} (use trimming), (4) total loop gain

References:
• W.H. Ki, Current sensing technique..., U.S. Patent 5,757,174, May 26, 1998.
• D. Ma et al., A 1.8V singleinductor dual-output..., IEEE VLSI Symp. Circ., June 2001
• H. Y. H. Lam et al., Loop gain analysis and ..., ISCAS 2004.

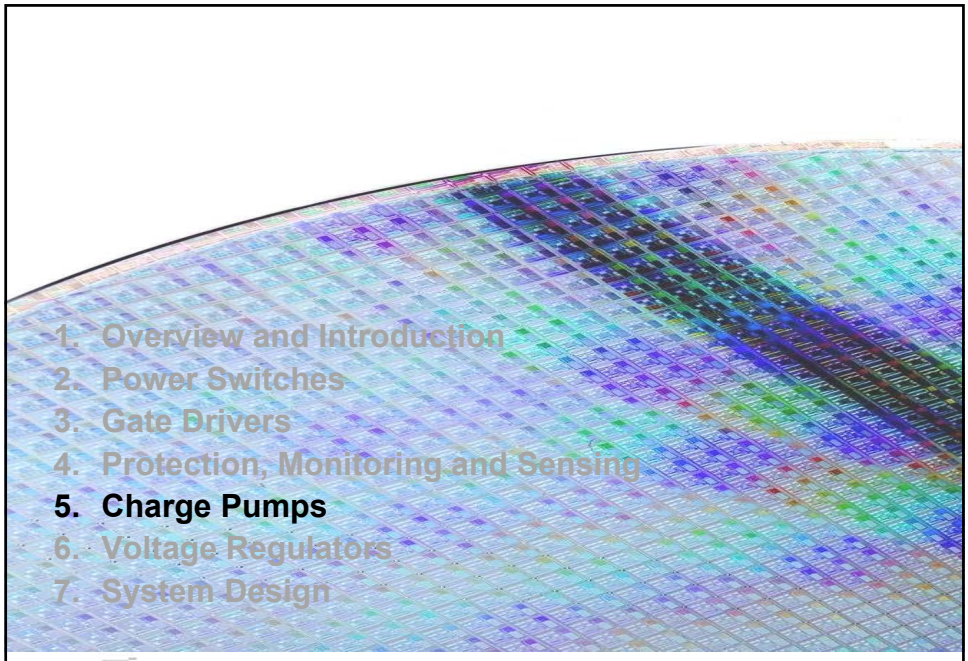
Monitoring: Short to GND / BAT, Open Load

Short to battery usually detected by current limit

Short to ground, open load are detected in off-state (FET off):



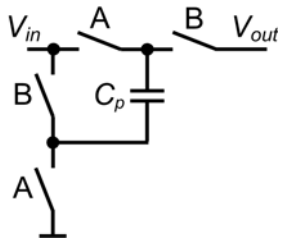
Voltage levels: $V_{ref2} < V_{DD} - V_F - I_{diag} \cdot R_{diag} < V_{ref1}$



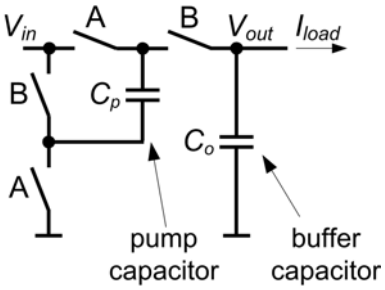
1. Overview and Introduction
2. Power Switches
3. Gate Drivers
4. Protection, Monitoring and Sensing
5. **Charge Pumps**
6. Voltage Regulators
7. System Design

Charge Pump Principle

Idea (Dickson Charge Pump):



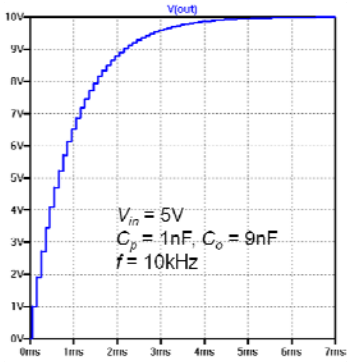
With buffer *C* at output:



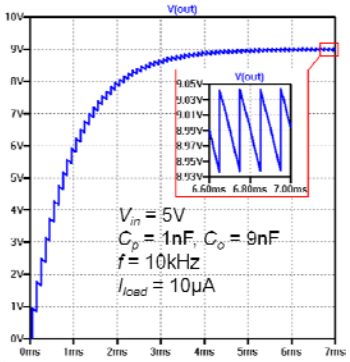
Voltage doubler: $V_{out} = 2V_{in}$ (ideally with I_{load} = 0)

Transient and DC Behavior

Without load current:

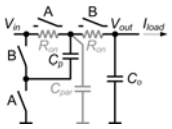


With load → ripple and drop of V_{out}



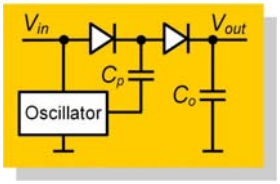
With I_{load}, C_{par} and finite switch on-resistance R_{on}

$$V_{out} = V_{in} + V_{in}\frac{C_p}{C_p + C_{par}} - \frac{I_{load}}{f_{sw}(C_p + C_{par})} - 2R_{on}I_{load}$$



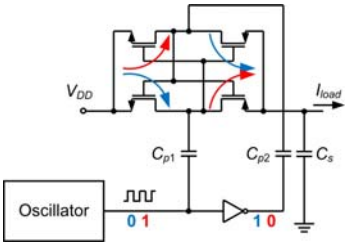
Typical Charge Pump Implementations

With diodes:



$$V_{out}\big|_{t\to\infty} = 2\left(V_{DD} - V_F\right)$$

With transistors:



Reference: Pelliconi, ESSCIRC 2001 und JSSC 2003

$$V_{out}\big|_{t\to\infty} = 2\left(V_{DD} - V_{DS,on}\right)$$

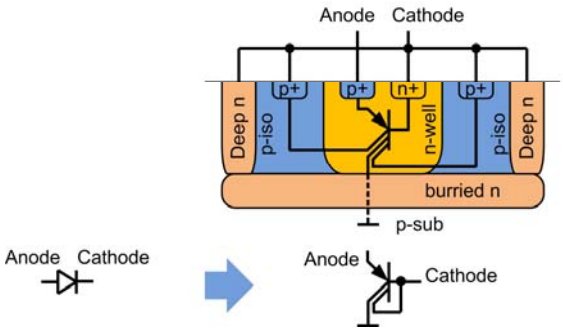
Advantage: Dual phase operation
→ 2x driving capability
→ 50% ripple or reduction of C, f

Cascading of N stages possible: V_{out} = (N+1) V_{in}

Realization of Diodes

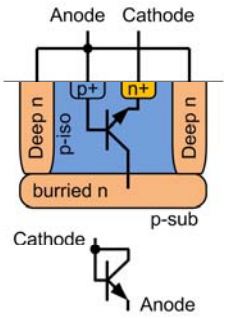
Every diode is associated with parasitic bipolar transistor:

Parasistic pnp



Isolation keeps β as low as 0.1

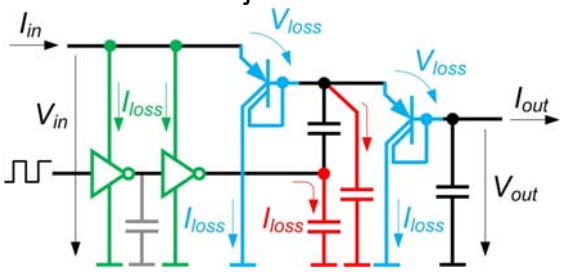
Parasistic npn



Minimum losses → preferred

Charge Pump Power Efficiency

Equivalent circuit with major losses:



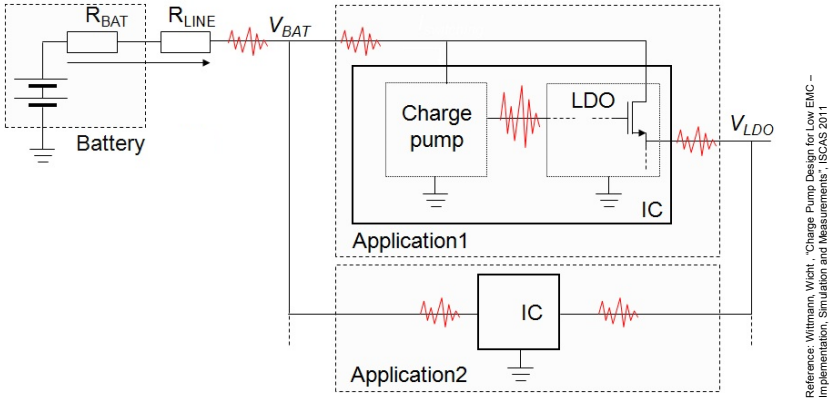
Charge pump efficiency

$$\eta = \frac{P_{out}}{P_{in}} = \frac{V_{out} I_{out}}{V_{in} I_{in}} = \frac{\overline{V_{out}} I_{out}}{V_{in} \overline{I_{in}}}$$

} Mean values per periode to account for ripple, current peaks, etc.

$$\eta = \frac{P_{out}}{P_{in}} = \frac{(2V_{in} - V_{loss1} - V_{loss2} - \cdots) I_{out}}{V_{in}(2I_{out} + I_{loss1} + I_{loss2} + I_{loss3} + \cdots)}$$

EMC: Conducted Emissions



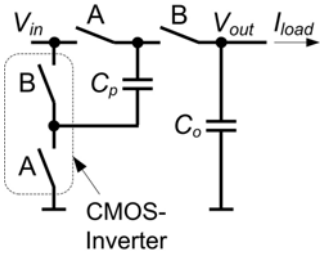
Reference: Wittmann, Wicht, "Charge Pump Design for Low EMC – Implementation, Simulation and Measurements", ISCAS 2011

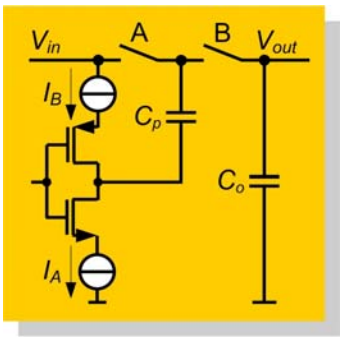
Current spikes from switching circuits like oscillator, charge pump → noise on global connection lines

Current-mode Charge Pumps

Switches replaced by current sources at bottom of C_p → reduced current spikes → EMC advantage

Conventional hard switching charge pump:

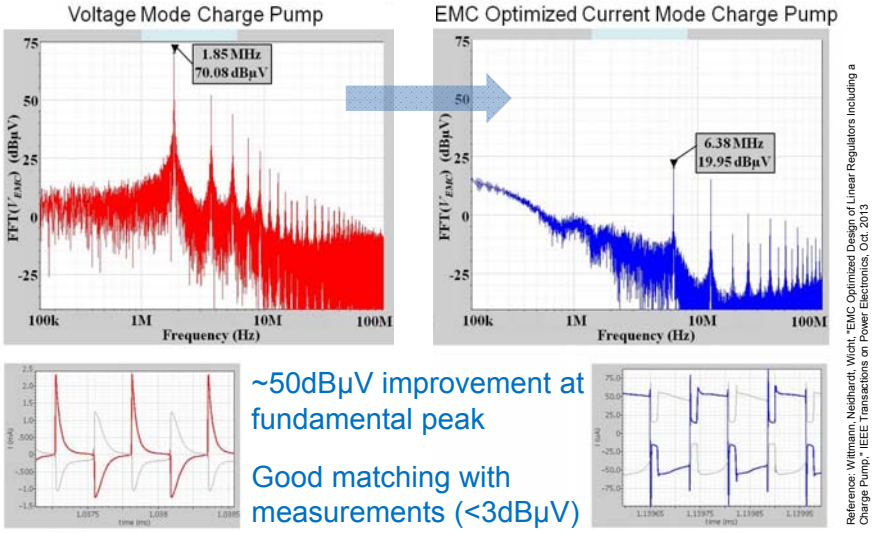




Periodic current spikes at every recharge of C_p

„Slow“ recharge of C_p over one half periode

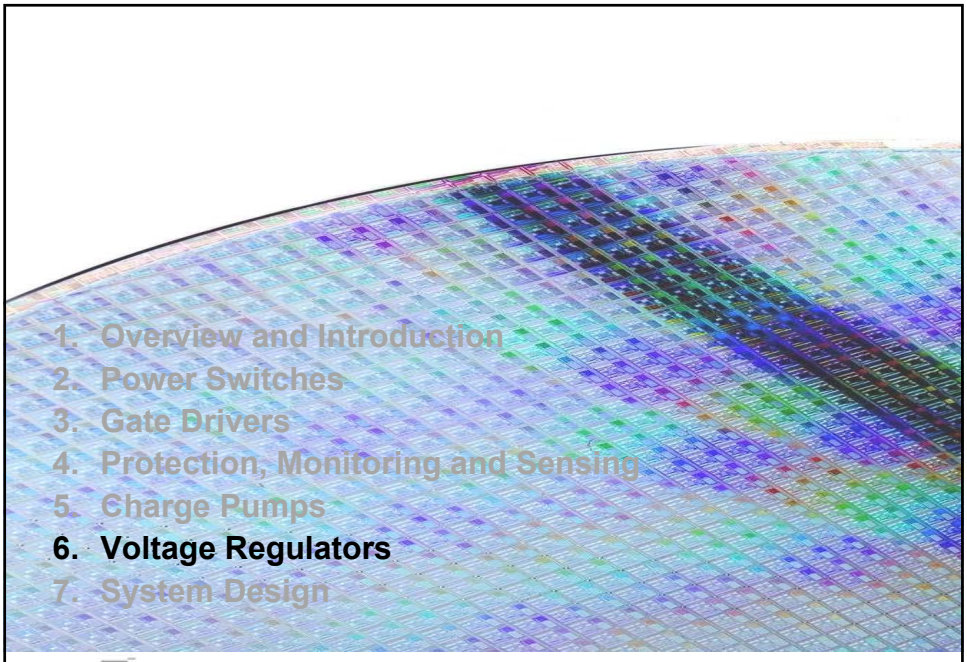
EMC Optimized Charge Pump



~50dBµV improvement at fundamental peak

Good matching with measurements (<3dBµV)

Reference: Wittmann, Neidhardt, Wicht, "EMC Optimized Design of Linear Regulators Including a Charge Pump," IEEE Transactions on Power Electronics, Oct. 2013



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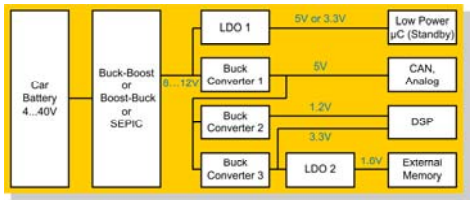
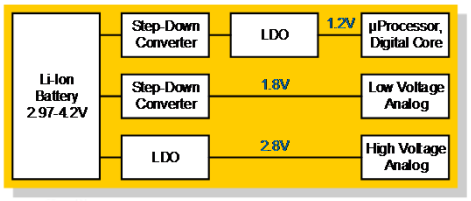
Automotive Power Management

Multiple regulators to supply µCs, MPUs, DSPs, analog & mixed-signal circuits → at „point of load“
→ Part of smart power ICs or separate power management ICs



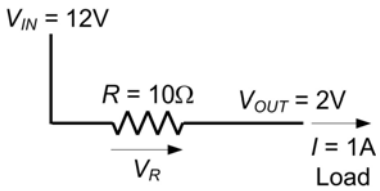
Automotive:
V_{in} > 10 - 60V,
larger conversion ratios



In Comparison → Handheld devices, consumer products:
V_{in} ~ 4V, moderate conversion ratios

How to Convert 12V into 2V?

Using a simple resistor…



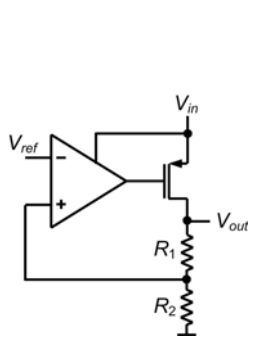
It works, but…

Large power loss at the resistor:

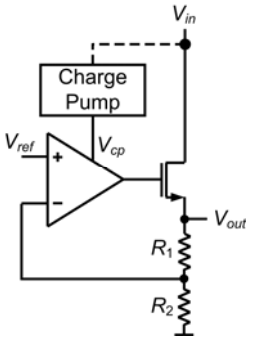
$P_R = V_R \cdot I$ = 10V · 1A = 10W
(even larger than P_{out}!)

Linear Low Dropout Regulator (LDO)

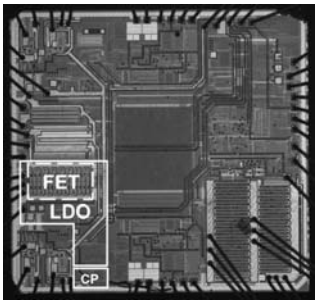
Key characteristics:
+ Fast load transient response (load steps)
− Poor power efficiency (losses in power FET)



pmos



nmos



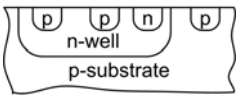
Reference: Wittmann, Wicht ISCAS 2011

Area comparison:
„nmos + CP < pmos“

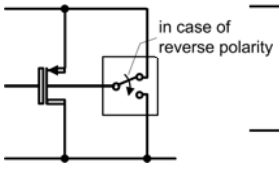
→ Dropout drives decision for pmos or nmos

Reverse Polarity Protection

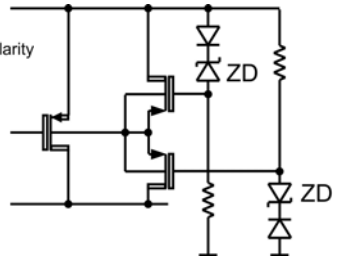
Rule: n-well at highest potential
→ pn-junction to substrate reverse biased



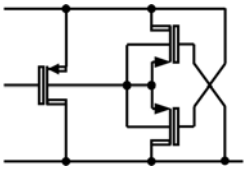
Concept:



Option 1:



Option 2:

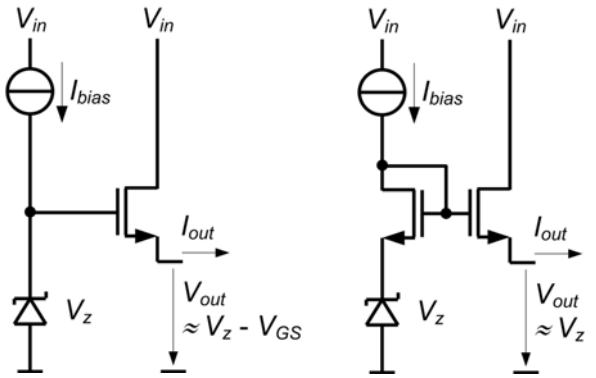


(observe max. V_{SG}!)

Most simple solution: Diode in battery line
→ drawback: dropout reduced by V_F → often not acceptable

Shunt Regulator

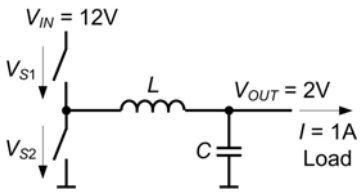
Alternative to LDO, often as a crude supply for e.g. noncritical digital block or as pre-regulator for LDO



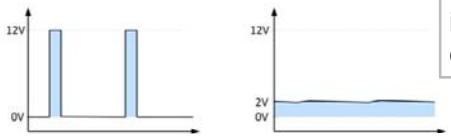
Comparision to LDO: Open loop → fast, but not as precise

How to Convert 12V into 2V?

Switched mode conversion…



Pulse-Width Modulation:



Pulse signal Output voltage

It works and has small losses…

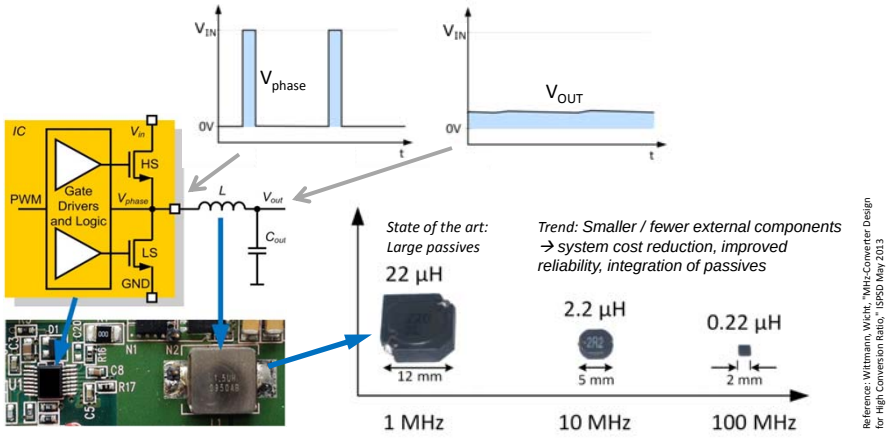
Power loss at the switches: $P_S = V_S \cdot I_S$

ideally:
off: $I_S = 0$ → $P_S = 0$
on: $V_S = 0$ → $P_S = 0$

in reality >95% power efficiency possible

Switched Mode Power Supplies

Key advantage: Much higher efficiency (>95%) and much less heat than linear regulators because *L* stores the energy

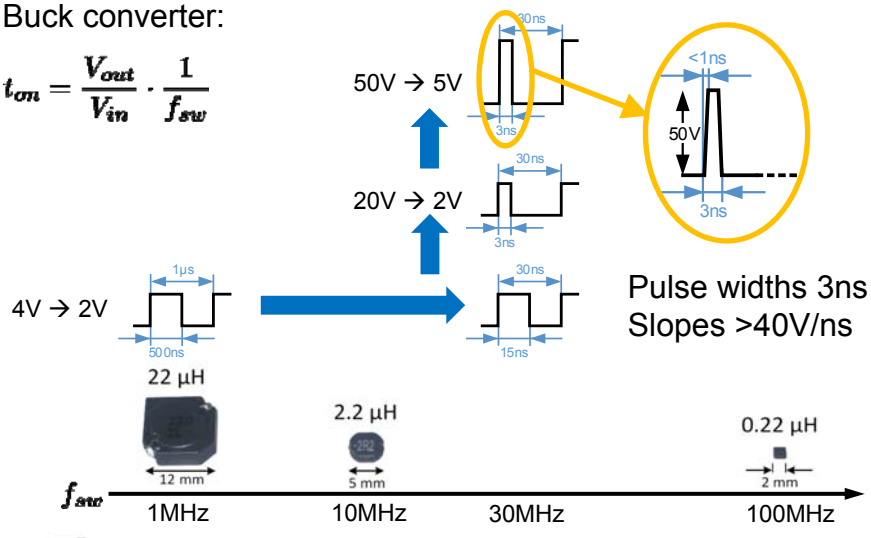


Reference: Wittmann, Wicht, "MHz-Converter Design for High Conversion Ratio," ISPSD May 2013

Impact of Fast Switching and High Vin

Buck converter:

$$t_{on} = \frac{V_{out}}{V_{in}} \cdot \frac{1}{f_{sw}}$$



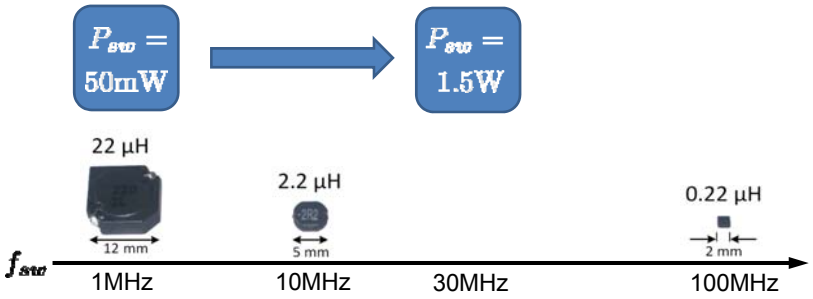
Losses

Power loss scales with switching frequency: $P_{loss} = E_{loss} f_{sw}$

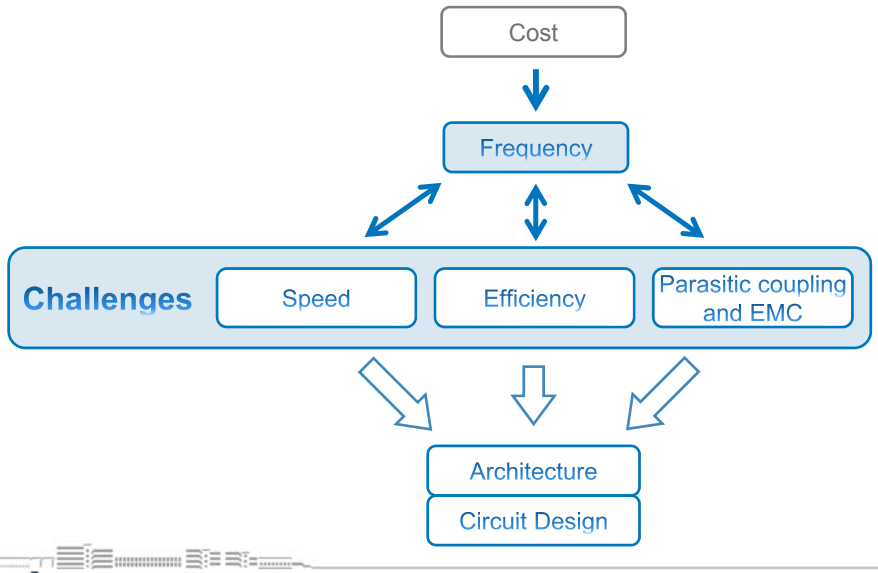
Capacitive energy loss scales proportional to Vin²

Switching energy loss scales proportional to Vin:

$E_{sw} = I_{out} V_{in} \Delta t_{sw} = 1\text{A} \cdot 50\text{V} \cdot 1\text{ns} = 50\text{nJ}$ (per period)

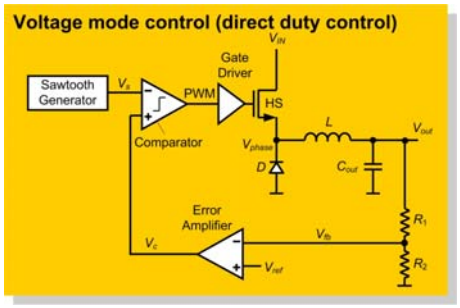


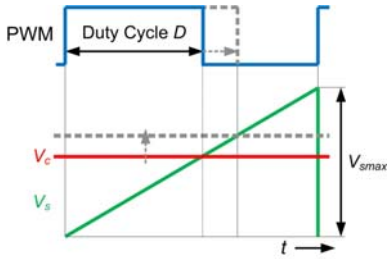
Challenges for Fast Switching Converters



Regulation Schemes: Voltage Mode Control

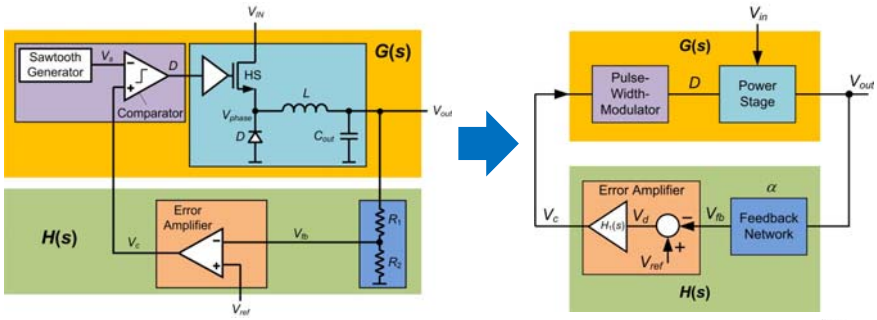
Control voltage V_c is compared to sawtooth reference:
$D = t_{on} / T = V_c / V_{smax}$ → D ↑ if V_c ↑





Drawback:
- Poor transient response to changes of V_{in} → Change in D has L-C_{out} time constant
- Acceptable line regulation requires voltage feedforward

Control Loop Analysis and Stability



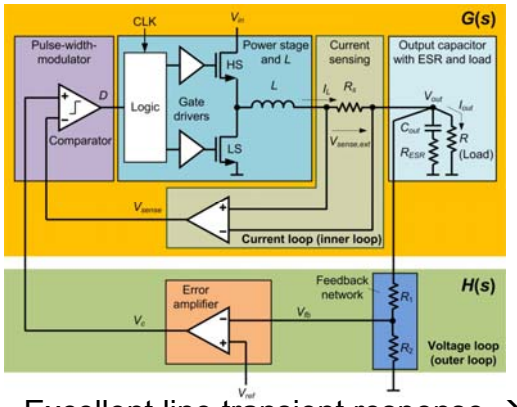
Closed loop transfer function: $\frac{V_{out}}{V_{ref}} = \frac{1}{\alpha}\frac{G(s)H(s)}{1+G(s)H(s)} \approx \frac{1}{\alpha}$ $\alpha = \frac{R_2}{R_1+R_2}$

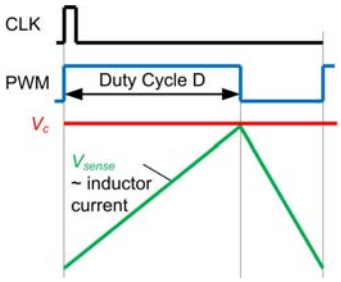
Loop gain: $\frac{V_{fb}}{V_{ref}} = G(s)H(s)$

Modulator transfer function: $G(s) = \frac{1}{V_{smax}} V_{in} \frac{1}{1 + s\frac{L}{R} + s^2 LC_{out}}$

Regulation Schemes: Current Mode Control

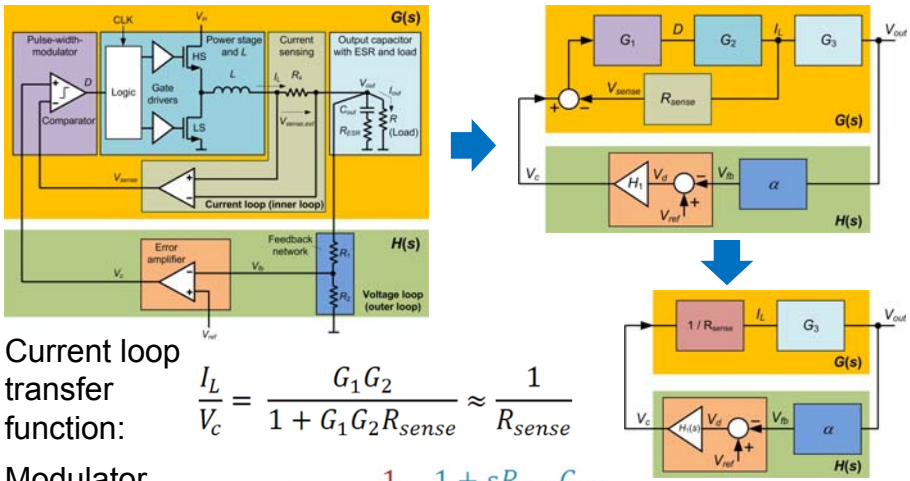
V_c is compared to a ramp voltage V_{sense} derived from the inductor current I_L, forming a second, inner control loop





- Excellent line transient response → V_{out} independent of V_{in}
- Inherent I_L current limit (by limiting V_c)

Control Loop Analysis Current Mode Control



Current loop transfer function:

$$\frac{I_L}{V_c} = \frac{G_1 G_2}{1 + G_1 G_2 R_{sense}} \approx \frac{1}{R_{sense}}$$

Modulator transfer function:

$$G(s) \approx \frac{1}{R_{sense}} \frac{1 + sR_{ESR}C_{out}}{1 + sRC_{out}}$$

→ 1st order system

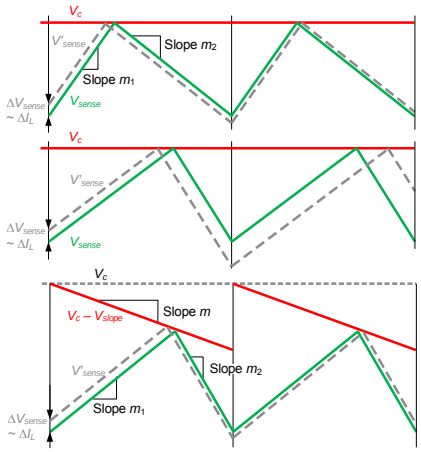
Current Mode: Subharmonic Oscillations

Unconditional instability above 50% duty cycle → pertubation ΔI_L of inductor current leads to subharmonic oscillations

$D < 0.5$ (stable)

$D > 0.5$ (unstable)

$D > 0.5$ (with slope compensation)

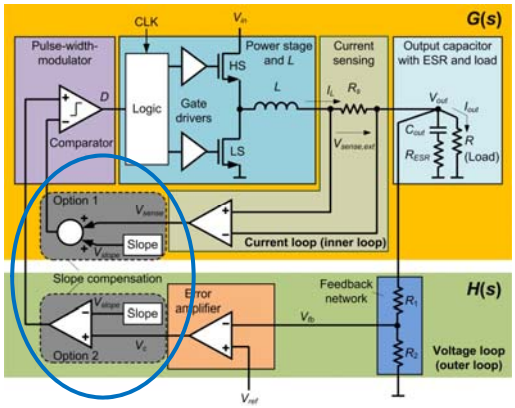


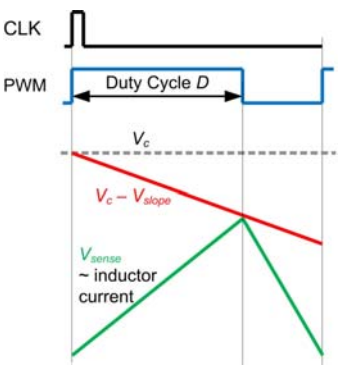
→ stable if

$$m > \frac{m_2}{2}$$

Regulation Schemes: Current Mode Control

With slope compensation: (V_c-V_{slope}) is compared to a ramp voltage V_{sense} derived from the inductor current

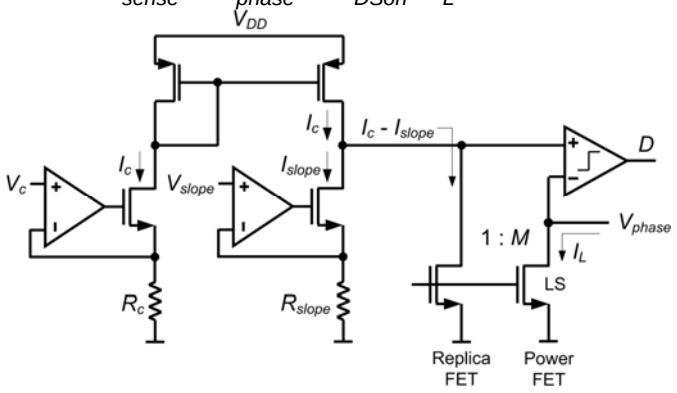




Two options to implement slope compensation

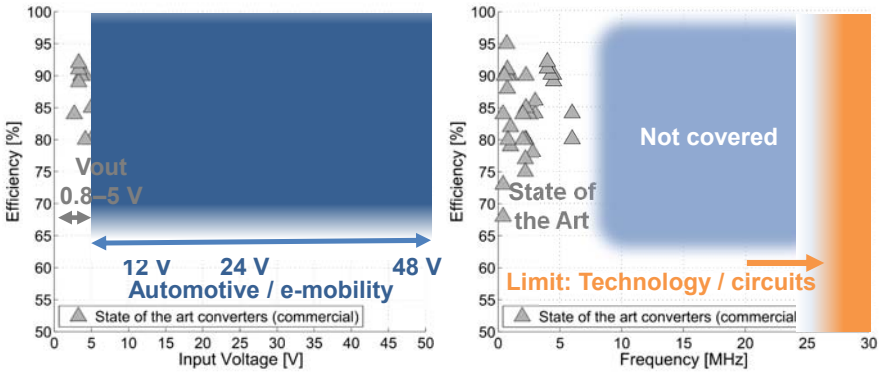
Slope Compensation: Example for Option 2

Difference (V_c – V_{slope}) is generated in current domain, fed into replica FET and compared to voltage across power FET = V_{sense} = V_{phase} = $R_{DSon} \cdot I_L$

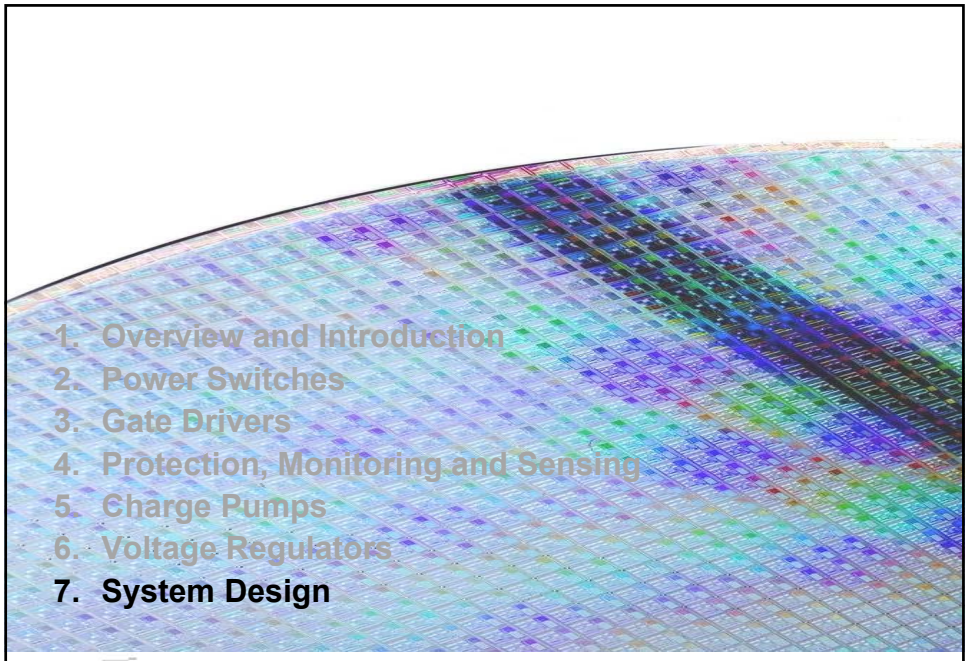


Concept can also be implemented on high-side FET

State-of-the-Art: Efficiency vs. fsw and Vin



- Existing high Vin converters are operating at < 5MHz
- Technology / circuits set limit at ~30 MHz (conversion ratio)
- Gap within 5-30 MHz not covered yet

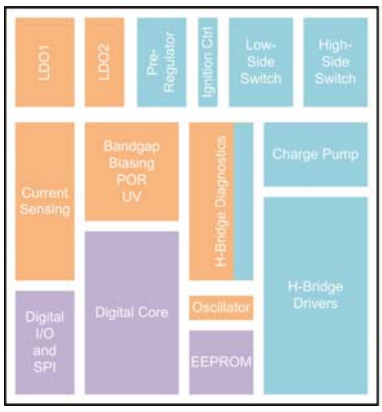


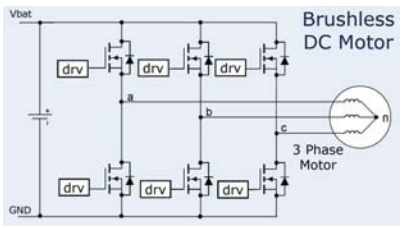
1. Overview and Introduction
2. Power Switches
3. Gate Drivers
4. Protection, Monitoring and Sensing
5. Charge Pumps
6. Voltage Regulators
7. **System Design**

Floorplan

Rule: Separate high-voltage and low-voltage domains

Motivation: HV-Isolation = Spacing = Chip Area = Cost



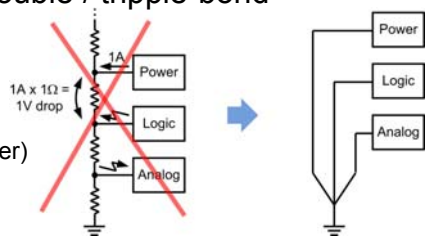


Source: ATMEL, Automotive Compilation, 2010

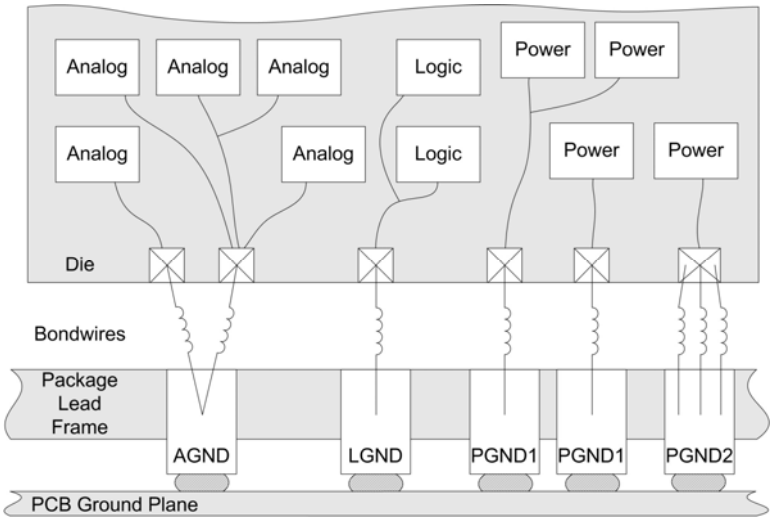
Mechanical stress: avoid corners / edges for critical blocks

Pinout, Grounding and Supply Guidelines

- Supply and ground pin next to each other, bypass-C placed here close to pins → reduces inductive effect and reduces EMI radiation level, also valid for on-chip wiring
- Keep short bond wires for power pins and fast signals (R↓, L↓) → close to the middle of one side of the die, vice versa: corner pins for quite signals
- Use separate bond pads for each domain or at least apply star connections, consider double / tripple-bond
- IC-Level wiring in groups:
  - Supply lines (high current)
  - Sensitive lines (analog)
  - Noisy lines (digital, switching power)



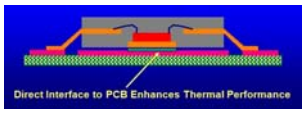
Pinout, Grounding and Supply Guidelines

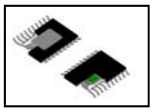


Packaging, Metallization and Thermal Design

Selecting the proper package

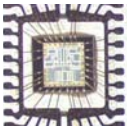
- Die Size estimation
- Power Dissipation





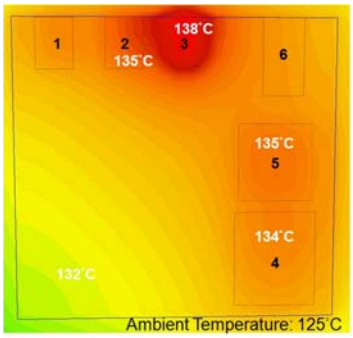
IC Level Copper Technology

- Power bussing
- Reduces power device area
- Bond Over Active Circuitry



Thermal Analysis

- Simple hand calculations
- Detailed thermal simulations



Source: Texas Instruments

Thanks for Your Attention!

Reutlingen and Surroundings