Instability of the Breakdown Voltage and Leakage Current in GaAs Pseudomorphic HEMTs

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Outline

- Introduction
  - Aim and summary of the presentation
  - III-V devices
- GaAs, HEMTs, PHEMTs
- Transistor
  - Degradation modes and mechanisms
  - Analysis of trapping effects
- Diode
  - Degradation modes and mechanisms
  - Analysis of the barrier height decrease and gate sinking
- Capacitors
  - Degradation modes and mechanisms

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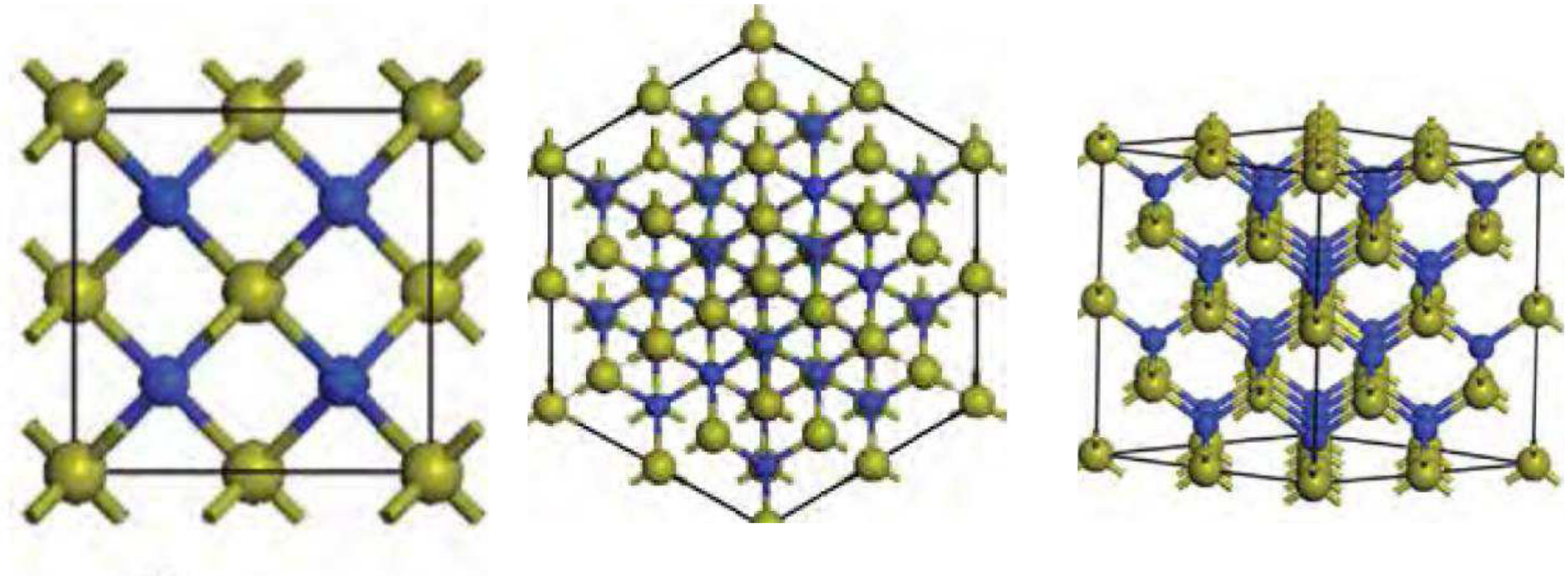
perspective view of GaAs crystal



Gallium arsenide has a zincblend crystal structure with a lattice constant of 5.6536Å

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Properties

	Si	GaAs	InP	SiC	GaN
BandGap (eV)	1.1	1.42	1.35	3.26	3.49
Electron Mobility at T=300°C $(cm^2/V \cdot s)$	5500	8500	5400	700	1000÷2000
v_{sat} $(10^7 cm/s)$	1	1.3	1	2	1.3
Breakdown field (MV/cm^2)	0.3	0.4	0.5	3	3
Thermal conductivity $(W/cm \cdot K)$	1.5	0.5	0.7	4.5	>1.5
Dielectric constant (ε_r)	11.8	12.8	12.5	10	9

electron mobility is four times higher than GaN and Si

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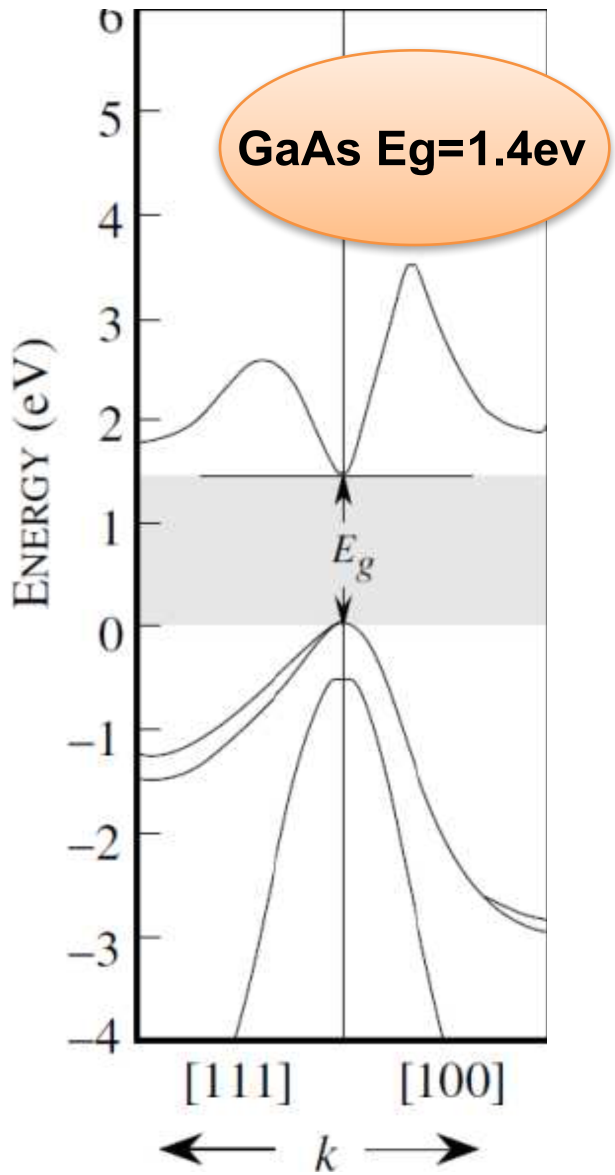
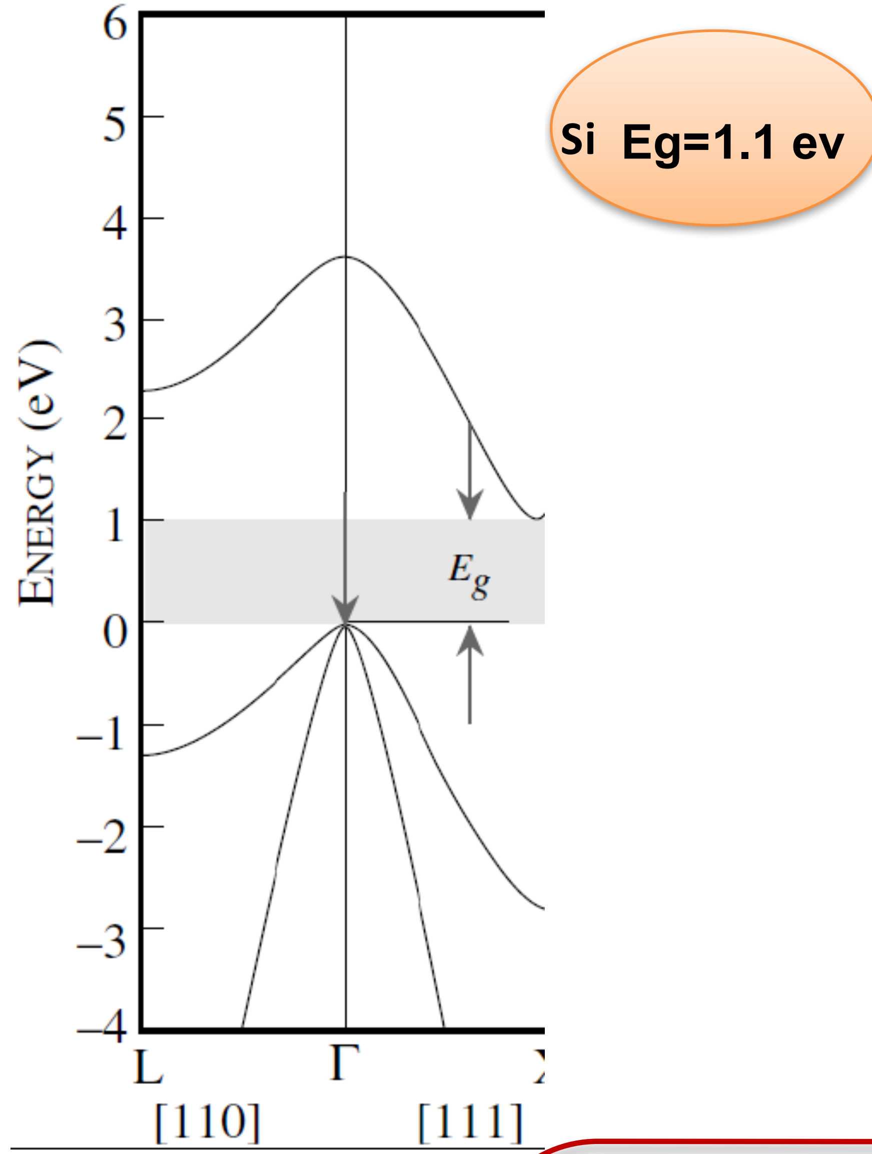

GaAs Eg=1.4ev
ENERGY (eV)
6
5
4
3
2
1
0
−1
−2
−3
−4
E_g
[111]
[100]
k


Si Eg=1.1 ev
ENERGY (eV)
6
5
4
3
2
1
0
−1
−2
−3
−4
E_g
L
Γ
[110]
[111]

HEMT

High Electron Mobility Transistors

- Field effect transistors composed by a hetero-junction
- The channel is produced by the creation of a bidimensional electron gas (**2DEG**) through the confinement of the electrons in a triangular quantum well
- Can reach high voltage and current levels, thus allowing the use of HEMT for applications which require **high power**.
- consequently to their **high mobility** and carrier velocity can reach significant performances in **high frequency applications.**

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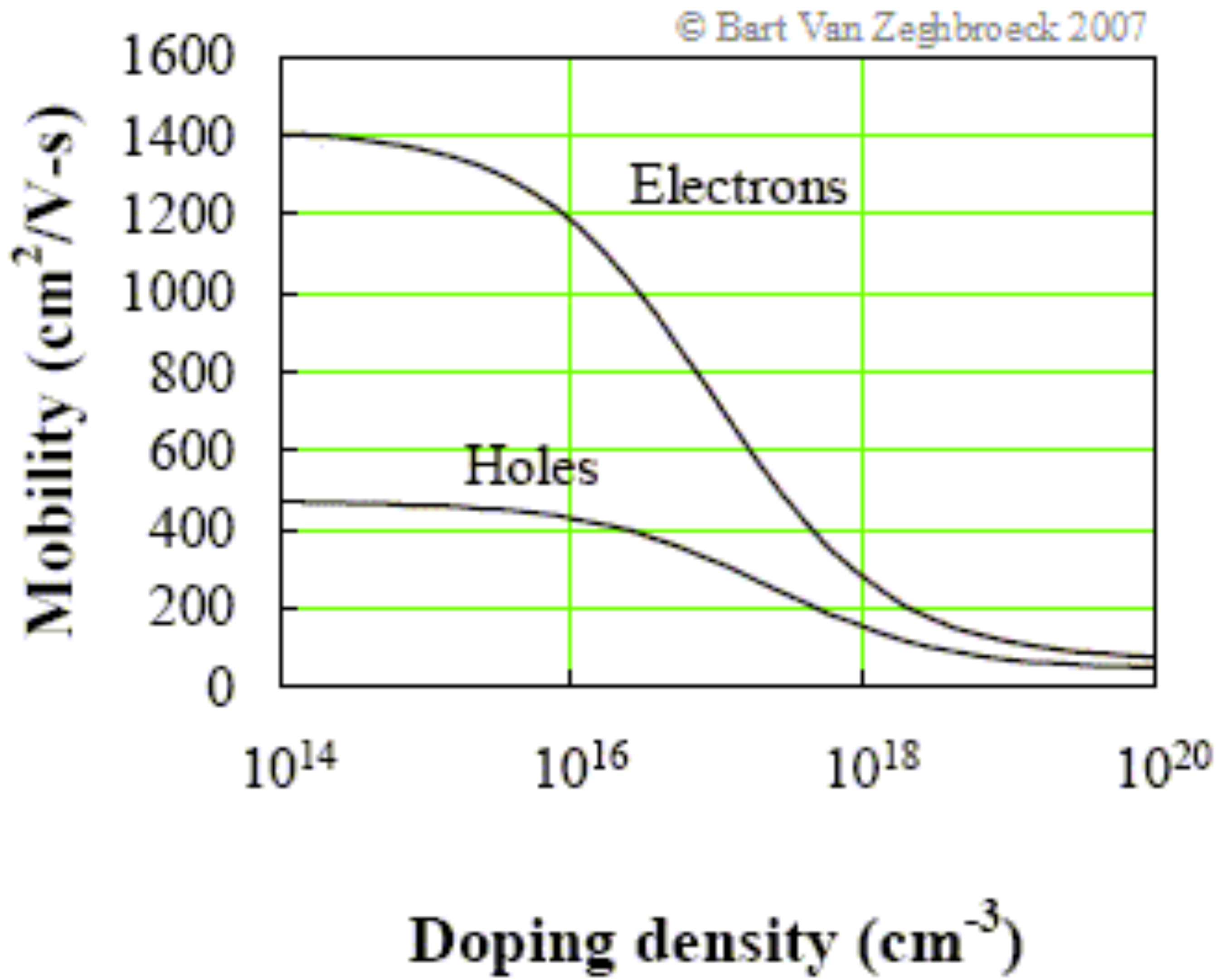
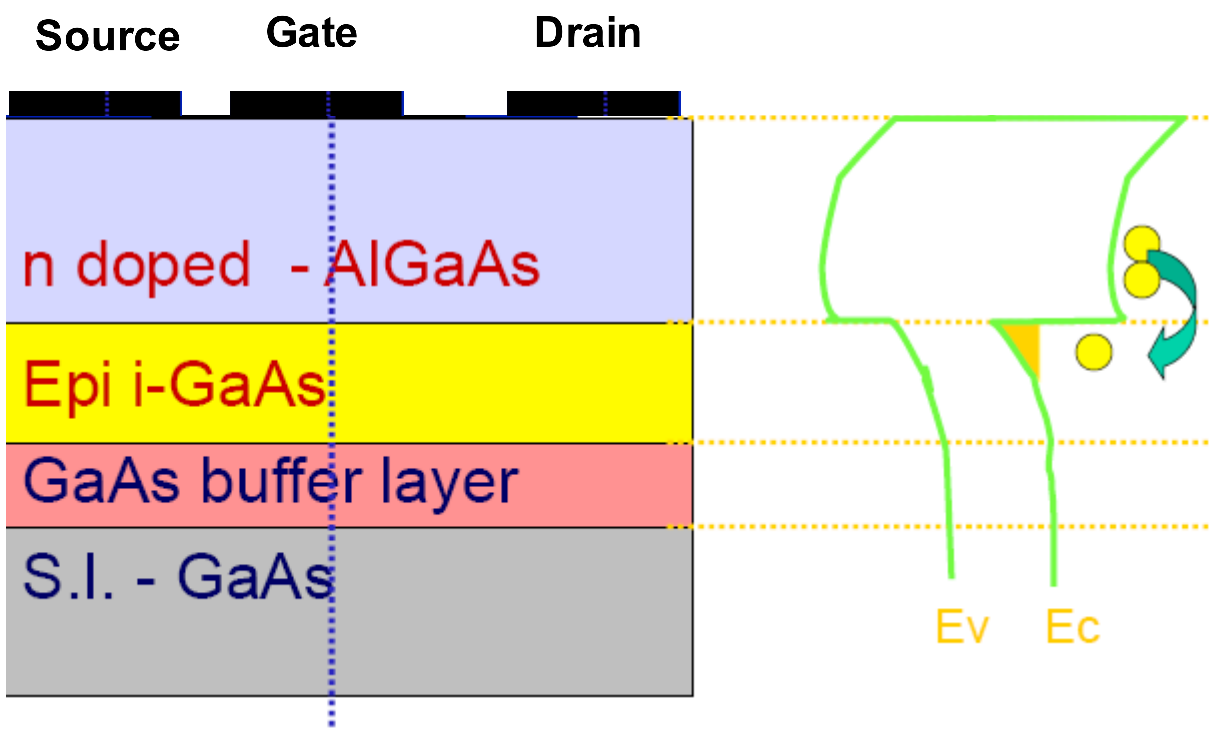
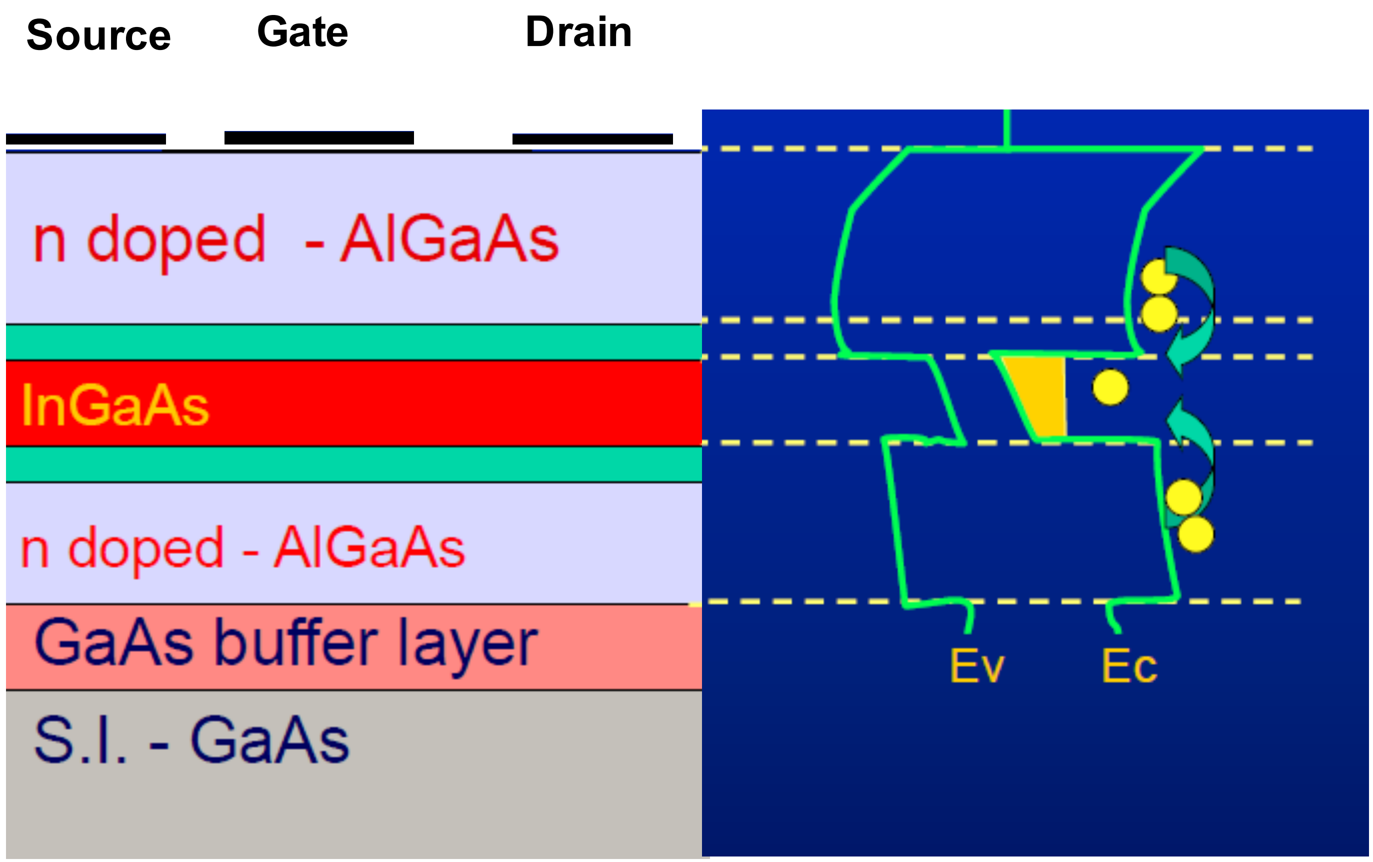

© Bart Van Zeghbroeck 2007
Mobility (cm^2/V-s)
1600
1400
1200
1000
800
600
400
200
0
Electrons
Holes
10^{14}
10^{16}
10^{18}
10^{20}
Doping density (cm^{-3})


Source
Gate
Drain
n doped - AlGaAs
Epi i-GaAs
GaAs buffer layer
S.I. - GaAs
Ev
Ec

PHEMTs



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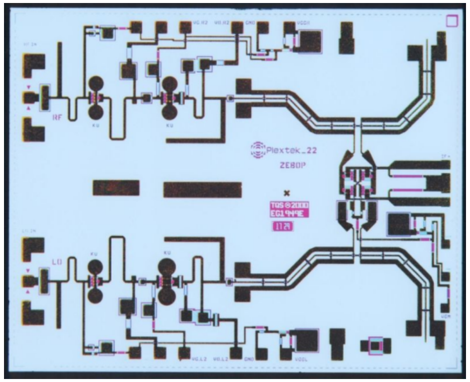
applications



MMIC

Space and satellite

LED

Radio astronomy

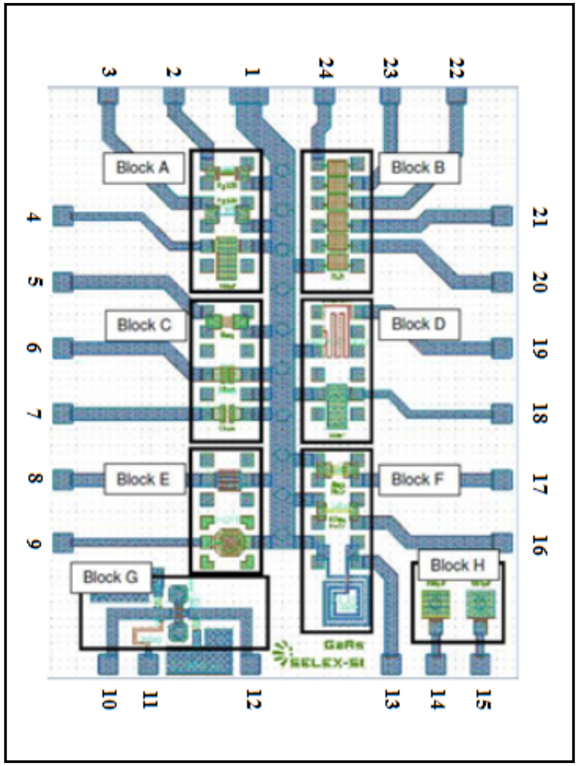
Aim and Summary of the Presentation

Aim of the presentation:

- To analyze the degradation induced by a pure thermal storage at ambient temperature T_{AMB} = 275°C.
- To define the main failure mechanisms.

Experimental Details:

- Tested devices (16 samples) are GaAs multifinger pHEMTs with a gate width of 0.2 mm.
- Test structures (MIM capacitors and diodes) are analyzed to confirm the hypotheses about the failure mechanisms
- A full characterization is performed at 24 h, 48 h, 144 h and 500 h of thermal stress.



Representative example of a test structure

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Survey on degradation mechanisms in GaAs pHEMTs

After del Alamo et al. * we can divide degradation mechanisms in GaAs pHEMTs into three main categories: (i) thermal, (ii) electrical, (iii) environmental.

Thermal Reliability

Reversible

Thermally activated electron detrapping (deep traps in the barrier):
- V_{TH} negative shift, R_D and R_S decrease, max g_m increase,

Irreversible

Barrier height variation
- V_{TH} shift

Surface state annealing (modification of surface oxides in the access regions):
- VTH no shift, sheet carrier density ns increase
- Frequency dispersion reduction, reduction of breakdown off state

Gate Sinking (formation of intermetallic compounds):
- V_{TH} positive shift, I_{DSS} and P_{OUT} drop
- Max g_m may slightly increase
- Ea = 1.4-1.6 eV
- Evolves at $\sqrt{t}$

Ohmic contact degradation (diffusion of Au in the barrier):
- Increase of (ohmic) contact resistance, max g_m decrease
- Ea = 1.6 eV
- Evolves at $\sqrt{t}$

*del Alamo, et "Thermal, electrical and environmental reliability of InP HEMTs and GaAs PHEMTs," in Electron Devices Meeting, 2004. IEDM Technical Digest. IEEE International , vol., no., pp.1019-1022, 13-15 Dec. 2004)

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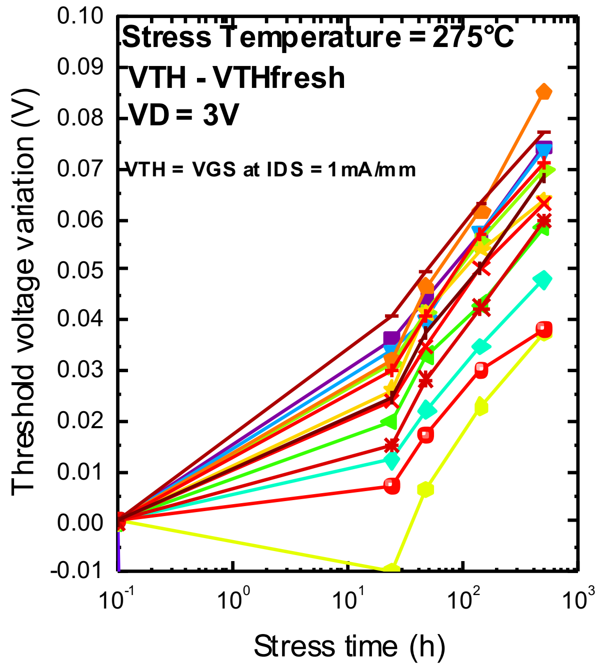
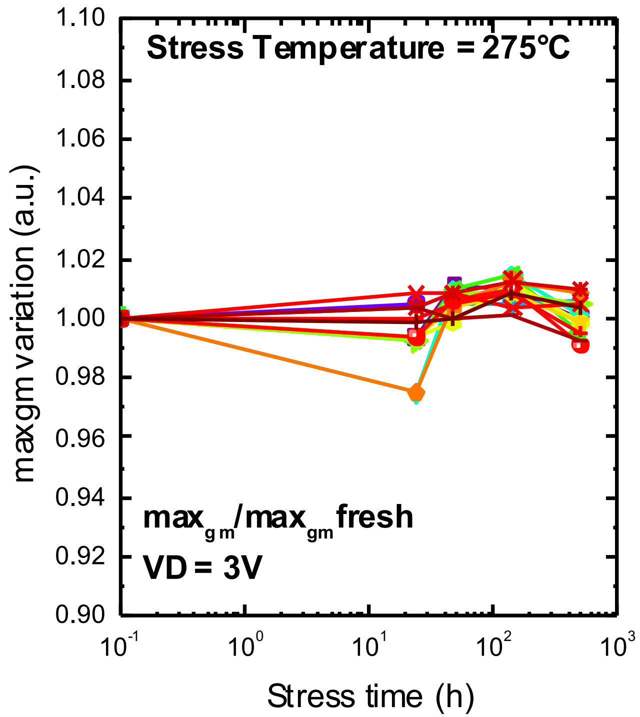
DC performance:

- Stability of the drain current (less than 5%) after 500 h of stress.
- Slight positive shift of the pinch-off voltage (less than 100 mV), probably ascribed to the gate sinking phenomenon and/or to the barrier height decrease..





DC performance:

- No degradation of the ohmic contacts (no variation in max g_m, on resistance and “end resistances”)

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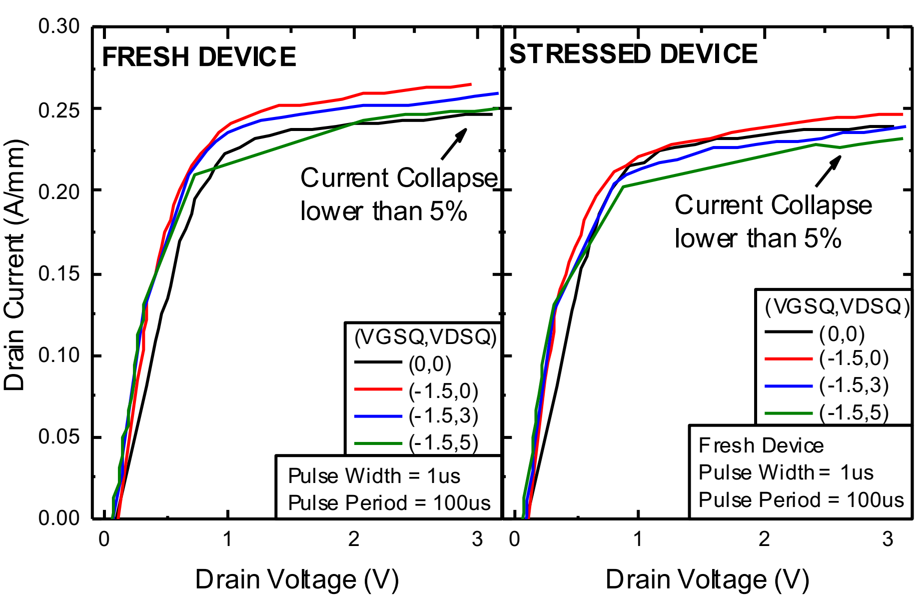
Trapping effects:

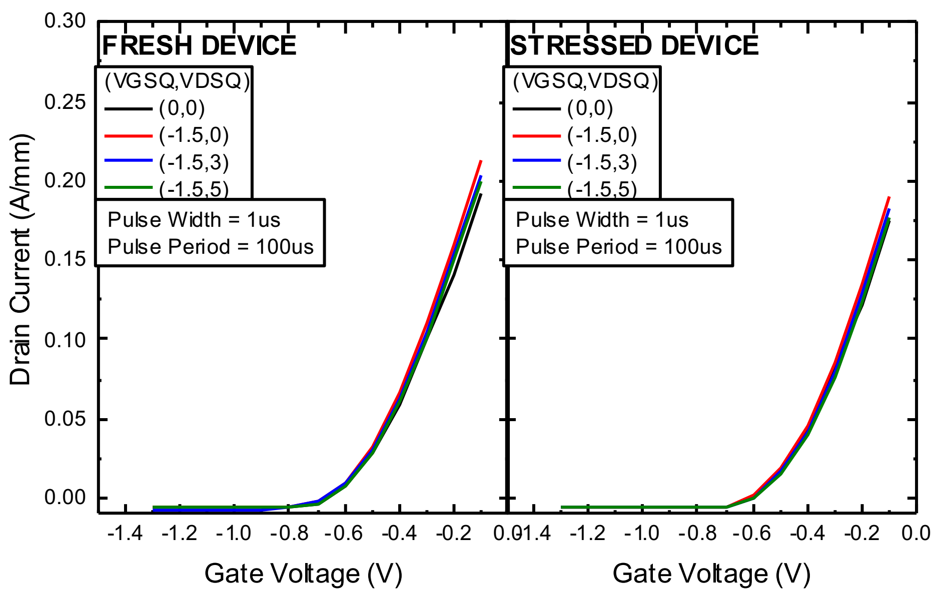
comparison of pulsed measurements: **fresh vs. stressed** devices

- the thermal storage (T_{amb} = 275°C in the case considered) induces **no variation** in the trapping effects.
- **no new defect** is created within the semiconductor material after stress

ID-VD



ID-VG

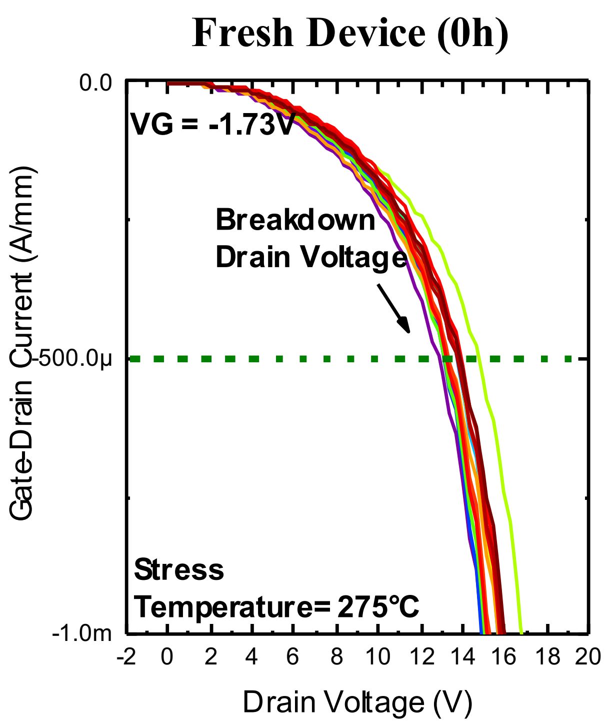


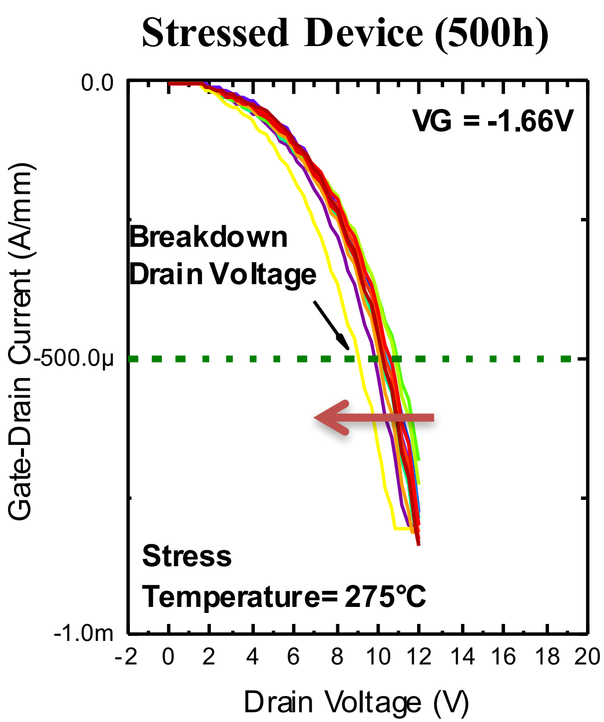
Breakdown voltage

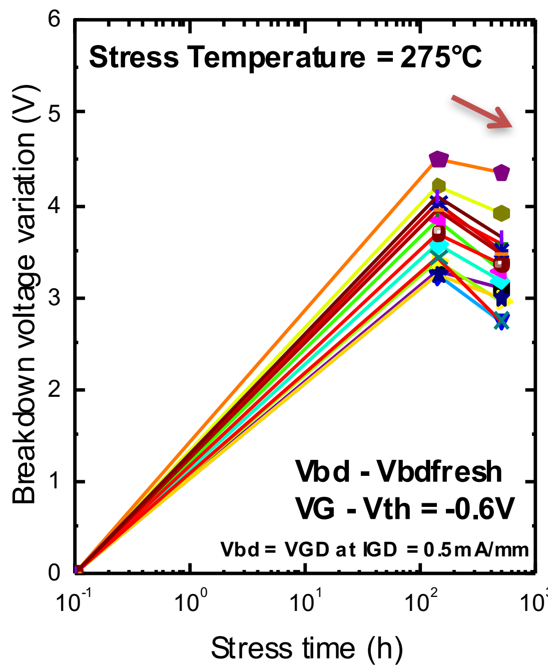
A significant decrease of the breakdown voltage is noticed (different colors correspond to the different devices tested).

breakdown voltage is defined as the gate-drain voltage corresponding to a gate-drain current value of 0.5 mA/mm

breakdown walk-in is induced by the thermal release of negative charge.







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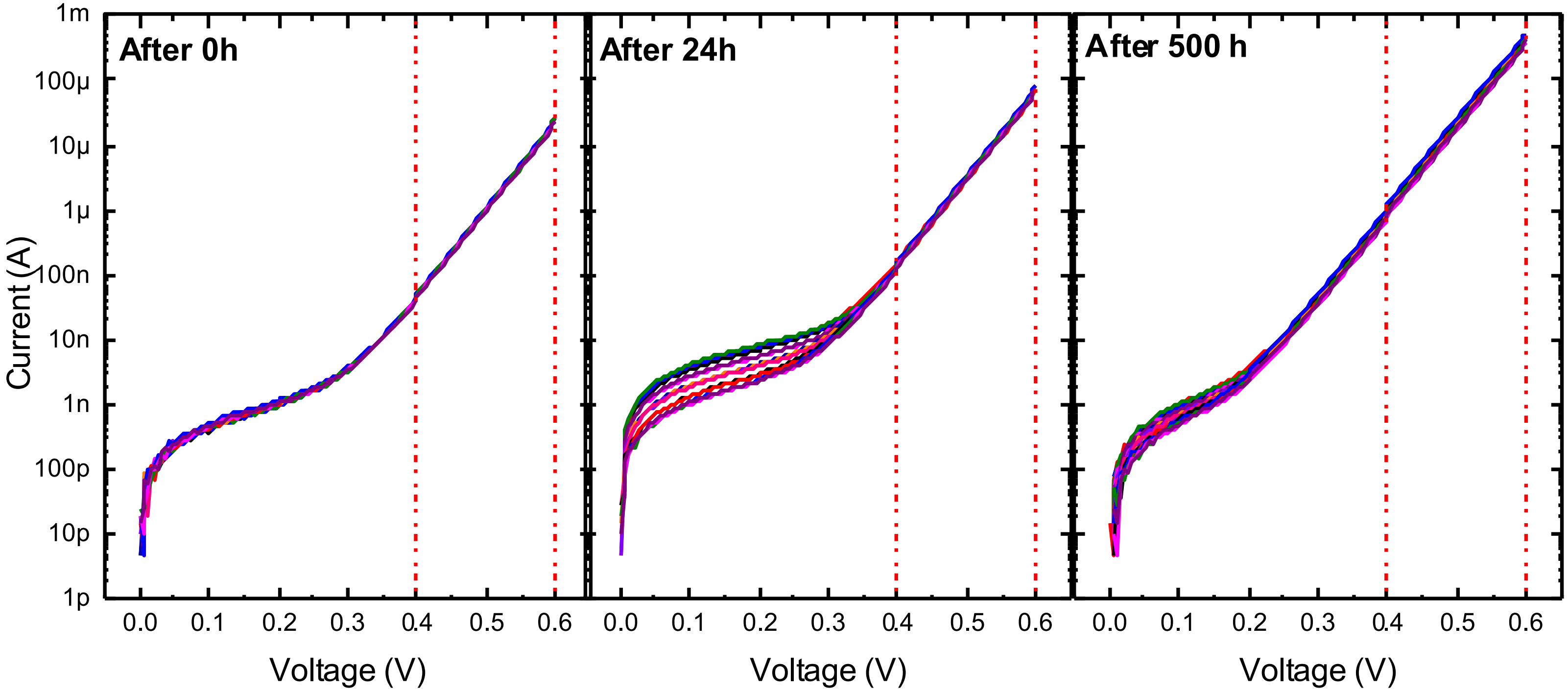
Diode: Degradation modes and mechanisms

Forward gate current – high gate bias levels

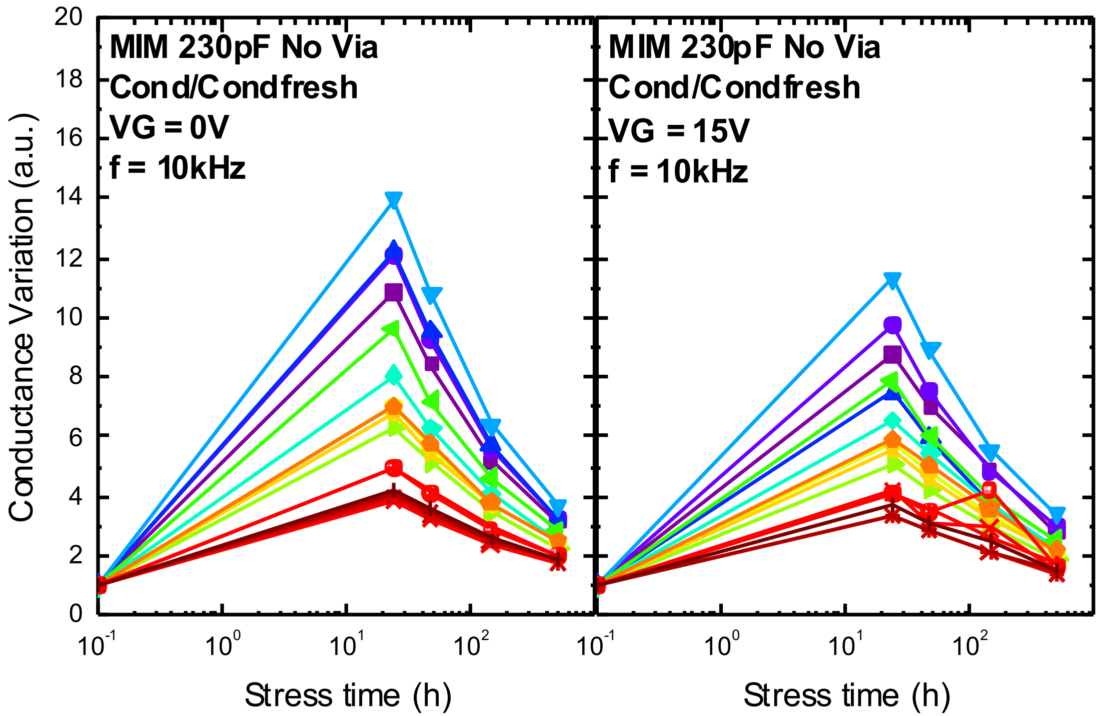
- Increase of the diode forward gate current (log trend).
- Behavior confirmed by the barrier height decrease and by the stability of the ideality factor



Forward gate current – low gate bias levels

- Non monotonic trend in both the reverse and forward current.
- Good correlation with the device position in the wafer.
- Degradation modes suggest the possible impact of the SiN passivation layer

Degradation Mechanisms in capacitors (MIM)



MIM capacitors

- No variation in the capacitance value
- Conductance value (ac, dc) reveals similar signature of the diode behavior at low voltage (non monotonic trend, correlation with the device position)
- The degradation of the dielectric of the MIM capacitors is suggested.

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Conclusions

- In the GaAs pHEMTs the pure thermal storage induces
  - negligible impact on the dc performance (I_{DSS}, V_{TH}, max g_m, on resistance and end resistances) ⟹ slight gate sinking and ohmic contact degradation
  - negligible impact on the pulsed performance ⟹ no degradation of the trapping effects and/or creation of new defects
  - Strong variation of the breakdown voltage ⟹ breakdown walk-in, thermal release of negative charges

- In the diodes the pure thermal storage influences:
  - the high bias forward current ⟹ variation of the barrier height decrease
  - the low bias behavior ⟹ Degradation of the SiN passivation layer

- The degradation of the SiN is confirmed by
  - The non monotonic variation of the diode (low bias) and its correlation with the device position
  - The analogous behavior of the degradation in the MIM capacitors

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Thank you!