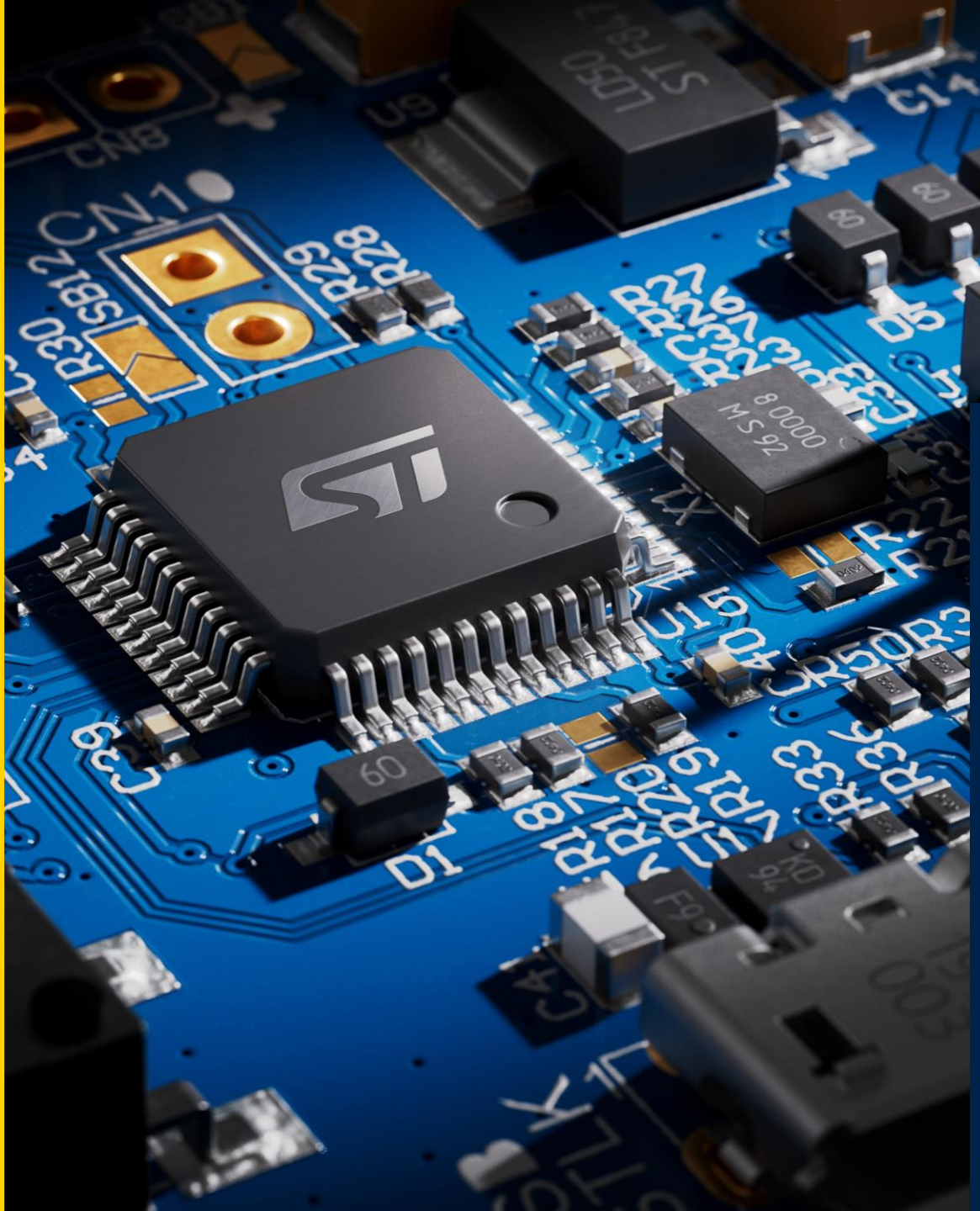

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MASTER THESIS PROPOSAL

MASTER THESIS OUTLINE

FIRST STEP

- State of the art research
- Theoretical background investigation

SECOND STEP

- Architecture proposal
- Circuit design

THIRD STEP

- Simulation and design verification
- Circuit performances evaluation

FIRST STEP

The state of the art is investigated to compare the latest solutions and make sure to design a competitive circuit. The candidate will get a deep understanding of the theoretical knowledge necessary for the development of the thesis.

SECOND STEP

Once the proposed architecture is approved, the design activity begins and throughout this phase the candidate will be supported to deepen his design skills, thus developing an optimal solution.

THIRD STEP

Simulations, performed in Cadence environment, will aim to assure the adherence of circuit performances to the expected behavior, while also verifying the robustness of the circuit over a wide temperature range.

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THESIS PROPOSALS

VOLTAGE REFERENCE DESIGN

- Car electrification demands high accuracy ADC to monitor cells in battery stack and guarantee proper State Of Charge (SOC) and State of Health (SOH) diagnostics.1-2mV variations on 5V full scale must be detected and such measurement must be stable over temperature and life-time, including prevention of piezo stress during soldering and assembly process. The candidate will explore the art of fully integrated references and design a very stable voltage reference circuit with respect to temperature and piezo effect.

LOW NOISE LDO DESIGN

- Low noise power supply are needed in the automotive field in a wide range of applications that can go from RF module to accurate sensors. In the meantime electric cars need very low power consumption IC. The candidate will explore state of the art low noise voltage regulators and will design an LDO trying to find out the best trade off between noise and power consumption.

VOLTAGE REFERENCE DESIGN

THESIS OBJECTIVES

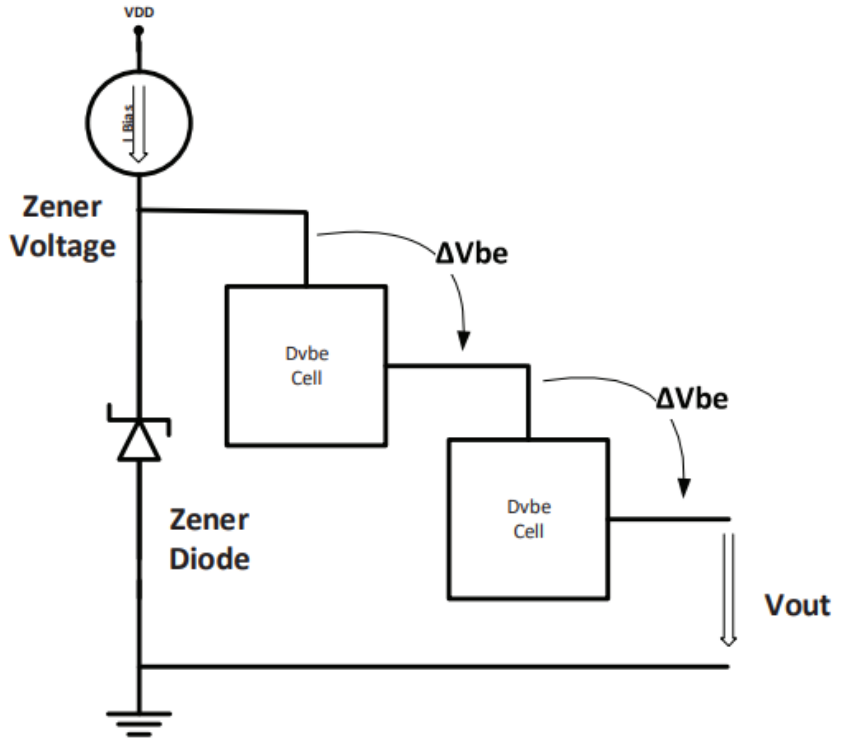
- Implementation of a robust **reference voltage** with respect to temperature variation and across all process corners

MAIN ACHIEVEMENT

- Design of an analog integrated circuit in **BCD technology**: prototype design, simulations in Cadence environment

SKILLS ACHIEVED

- Deepening of circuit analysis and design skills
- Problem solving and reasoning skills



1. V. Bucur, G. Banarie, S. Marinca and M. Bodea, **"A Zener-Based Voltage Reference Design Compensated Using a ΔVBE Stack,"** *2018 25th International Conference "Mixed Design of Integrated Circuits and System" (MIXDES)*, Gdynia, Poland, 2018, pp. 116-120, doi: 10.23919/MIXDES.2018.8436687

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VOLTAGE REFERENCE DESIGN

The most used and of simplest implementation digital calibration algorithms for the voltage characteristics of ADCs involve the use of a quadratic calibration curve. However, for the calibration process to be successful it is essential that the **reference voltage** of the ADCs also has a quadratic trend.

Some circuit non-idealities can induce a distortion of the well-known parabolic characteristic of the reference voltage with respect to the **temperature variation**. This usually causes the onset of a non-quadratic behavior, but of a higher order, and thus making the calibration incapable of correcting some terms and therefore ineffective.

The candidate will first have to analyze this phenomenon, delving into the reasons that lead to these dynamics.
Next, he/she will work on the design of a circuit prototype that is robust to the non-idealities that induce these deviations.

He/She will finally design a **reference voltage** based on a **buried zener diode**, expecting better performances with respect to a classical bandgap:

- **Lower stress dependence**
- **Reduced Long-Term Drift**
- **Good noise performance**
- **Lower Re-Flow Drift**
- **Almost linear characteristic**

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LOW NOISE LDO DESIGN

THESIS OBJECTIVES

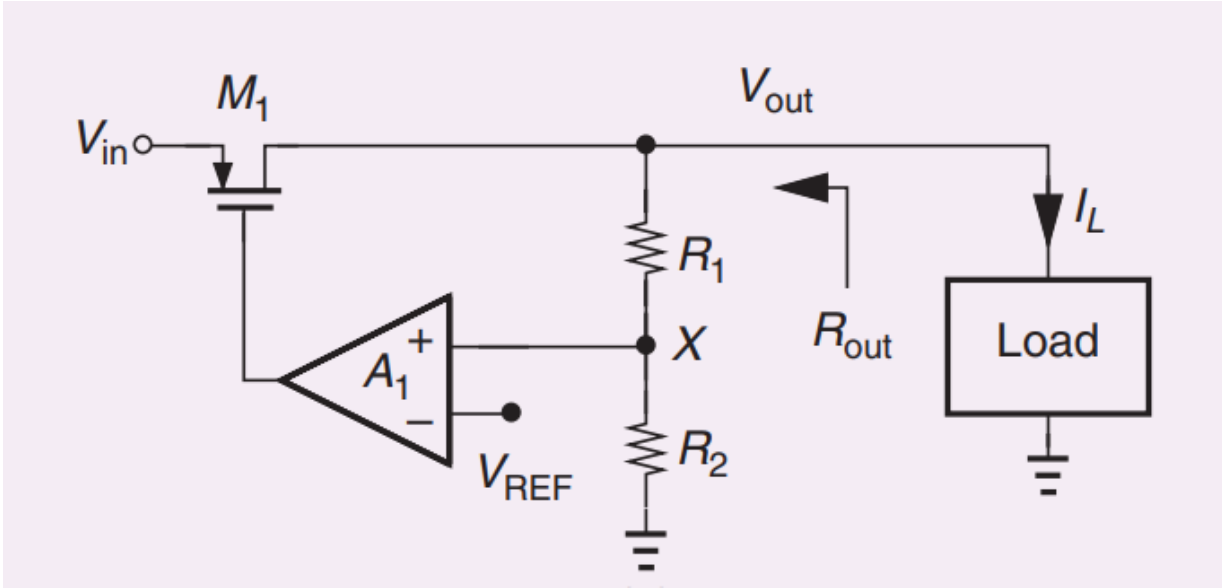
- Implementation of a **low noise LDO** with high PSRR and low current consumption

MAIN ACHIEVEMENT

- Design of an analog integrated circuit in **BCD technology**: prototype design, simulations in Cadence environment

SKILLS ACHIEVED

- Deepening of circuit analysis and design skills
- Problem solving and reasoning skills



4. B. Razavi, **"The Low Dropout Regulator [A Circuit for All Seasons],"** in *IEEE Solid-State Circuits Magazine*, vol. 11, no. 2, pp. 8-13, Spring 2019, doi: 10.1109/MSSC.2019.2910952.

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LOW NOISE LDO DESIGN

New applications of Advanced Driver Assistance Systems (ADAS) require low-noise power supplies for cameras, Lidar, and high-performance MCUs.

Thus, the growing need to decrease noise levels requires the deft ability to design an **LDO** that exhibits both **low noise** and **high PSRR** while still satisfying the requirement for **low current consumption**.

In a first step, the candidate should conduct a careful study of the state of the art and review of the literature.

Next, he/she will focus on the analysis of an existing LDO IP, designed with the purpose of meeting the requirements of output regulated voltage accuracy, which, however, has insufficiently lower noise levels.

Following a simulation and measurement phase of the key parameters of the considered LDO, he/she will have to analytically identify the shortcomings to be addressed.

Finally, he/she will define a new architecture of the reference and the LDO, and then move on to the design and verification phase of the identified solution to highlight consistency with the specification targets set earlier.

- **State of the art and literature review**
- **Analytic identification of LDO top detractors**
- **Definition of new reference and LDO architecture**
- **Design and verification of identified solution**

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For further investigation

1. V. Bucur, G. Banarie, S. Marinca and M. Bodea, **"A Zener-Based Voltage Reference Design Compensated Using a ΔVBE Stack,"** *2018 25th International Conference "Mixed Design of Integrated Circuits and System" (MIXDES)*, Gdynia, Poland, 2018, pp. 116-120, doi: 10.23919/MIXDES.2018.8436687

2. B. Razavi, **"The Bandgap Reference [A Circuit for All Seasons],"** in *IEEE Solid-State Circuits Magazine*, vol. 8, no. 3, pp. 9-12, Summer 2016, doi: 10.1109/MSSC.2016.2577978.

3. B. Razavi, **"The Design of a Low-Voltage Bandgap Reference [The Analog Mind],"** in *IEEE Solid-State Circuits Magazine*, vol. 13, no. 3, pp. 6-16, Summer 2021, doi: 10.1109/MSSC.2021.3088963.

4. B. Razavi, **"The Low Dropout Regulator [A Circuit for All Seasons],"** in *IEEE Solid-State Circuits Magazine*, vol. 11, no. 2, pp. 8-13, Spring 2019, doi: 10.1109/MSSC.2019.2910952.

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