

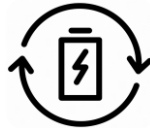


UNIVERSITÀ
DEGLI STUDI
DI PADOVA

Internship Positions for Master Thesis Students and Possible Ph.D. Positions



Fully Integrated Power Management

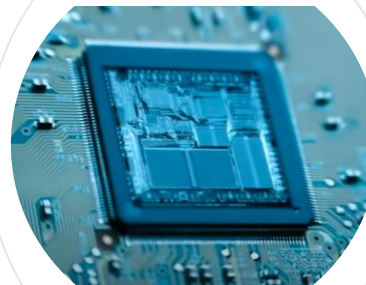


- Low power bandgap voltage reference in nm-scale CMOS
- Fully integrated capless LDO with fast load response for wireless transmitter application in nm-scale CMOS
- A fully integrated Switched Capacitor Converter (SCC) with low power consumption regulation loop for high efficiency in light load condition in nm-scale CMOS
- Low power control loop for Hybrid DC-DC converter in nm-scale CMOS
- And much more to come...



Digital Assisted RF and mmW

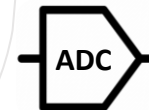
- High performance harmonic oscillators for car radar applications) in nm-scale CMOS
- Low power transceiver for Bluetooth Low Energy radios in nm-scale CMOS
- Digital power amplifiers for Ultra Wide Band ranging applications in nm-scale CMOS
- mmWave Front-ends for wireless communications systems and radar applications in CMOS/BiCMOS technology.
- And much more to come...



Clocking and Interfaces



- Design of low power digitally controlled ring oscillator in nm-scale CMOS
- Analysis and development of a compact delay lines for digital DLL in nm-scale CMOS
- Concept and design of self-calibrated reference frequency doubler in nm-scale CMOS
- Design of a digital PLL with a dedicated modelling and design tool CAD in nm-scale CMOS
- And much more to come...



Analog to Digital Converters

- Modelling and simulation of cascade oversampling ADC (e.g. SMASH Delta Sigma) in nm-scale CMOS
- Modelling and simulation of RFDAC for Bluetooth/Wifi radios in nm-scale CMOS
- Concept study on the Continuous Time Pipeline ADC architecture for high speed applications
- Coding scripts for Systematic Design of Multi-Stage Operational Amplifiers
- And much more to come...

Infineon Villach contact: **Gianluca Marin**
Gianluca.Marin@infineon.com
+39 3402581465

University contact: **Andrea Neviani**
Andrea.Neviani@unipd.it