# Harmonic Limiting Standards and Power Factor Correction Techniques

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## OUTLINE

- BASICS OF POWER FACTOR CORRECTION
- REVIEW OF HARMONIC STANDARDS
- BASICS OF SINGLE-PHASE PFC TOPOLOGIES AND CONTROL
- CONTROL TECHNIQUES FOR SINGLE-PHASE PFC'S AND COMMERCIAL CONTROL IC'S
- INSULATED TOPOLOGIES
- TECHNIQUES FOR IMPROVING OUTPUT VOLTAGE CONTROL SPEED
- BASICS OF SOFT-SWITCHING TECHNIQUES
- SMALL-SIGNAL MODELING
- SINGLE-PHASE APPLICATION EXAMPLES

### **POWER FACTOR DEFINITION**

Input voltage and current are periodic waveforms with period T<sub>i</sub>.

Power factor **PF**:

$$PF \equiv \frac{P}{V_{i,rms} \cdot I_{i,rms}}$$

where **P** is the average power:

$$P = \frac{1}{T_i} \cdot \int_{T_i} v_i i_i dt$$

and 
$$\mathbf{V}_{i,rms}$$
 and  $\mathbf{I}_{i,rms}$  are :  
 $V_{i,rms} \equiv \sqrt{\frac{1}{T_i} \int_{T_i}^{1} v_i^2 dt}$ 
 $I_{i,rms} \equiv \sqrt{\frac{1}{T_i} \int_{T_i}^{1} i_i^2 dt}$ 

## **POWER FACTOR DEFINITION**

Being voltage and current periodic waveforms we can write in Fourier series:

$$v_{i} = V_{0} + \sum_{k=1}^{\infty} \sqrt{2} V_{k} \sin(k\omega_{i} + \phi_{k})$$
$$i_{i} = I_{0} + \sum_{k=1}^{\infty} \sqrt{2} I_{k} \sin(k\omega_{i} + \gamma_{k})$$

 $V_0$ ,  $I_0$  = average values

 $V_k$  ,  $I_k$  = RMS values of harmonics

The average power is:

$$\mathbf{P} = \mathbf{V}_0 \mathbf{I}_0 + \sum \mathbf{V}_k \mathbf{I}_k \cos(\phi_k - \gamma_k)$$

#### CONSEQUENCE:

Current harmonic terms contributes to active power only in the presence of voltage harmonic terms of the same frequency.

### **POWER FACTOR DEFINITION**

$$0 \le PF \le 1$$

PF = 1 only if current and voltage are proportional

Power Factor Correction



An ideal Power Factor Corrector (PFC) takes from the supply a current which is proportional to the supply voltage

 $R_{em} = \frac{V_i}{i_i}$  emulated resistance

#### **POWER FACTOR DEFINITION**

#### PARTICULAR CASE: SINUSOIDAL INPUT VOLTAGE

$$PF = \frac{V_1 I_1 \cos(\phi_1)}{V_1 \cdot I_{i,rms}} = \frac{I_1}{I_{i,rms}} \cdot \cos(\phi_1)$$

D.F.= 
$$\frac{I_1}{I_{i,rms}}$$
 = DISTORTION FACTOR

$$cos(\phi_1) = DISPLACEMENT FACTOR$$

D.F. = 
$$\frac{1}{\sqrt{1 + (THD)^2}}$$
, THD =  $\frac{\sqrt{I_{i,rms}^2 - I_1^2}}{I_1}$ 

(THD = Total Harmonic Distortion)

# **POWER FACTOR REQUIREMENTS**

- PF = 1 implies:
- o zero displacement between voltage and current fundamental component ( $\phi_1 = 0$ )
- o zero current harmonic content



 $\cos(\phi_1) \neq 0$ , D.F. = 0

In both cases PF<1

### WHY POWER FACTOR CORRECTION

- o Increased source efficiency
  - lower losses on source impedance
  - lower voltage distortion (cross-coupling)
  - higher power available from a given source
- o Reduced low-frequency harmonic pollution
- o Compliance with limiting standards (IEC 555-2, IEEE 519 etc.)

# BASICS OF ACTIVE POWER FACTOR CORRECTION

### **POWER FACTOR CORRECTION TECHNIQUES**

#### **PASSIVE METHODS: LC filters**

- o power factor not very high
- o bulky components
- o high reliability
- o suitable for very small or high power levels

#### **ACTIVE METHODS: high-frequency converters**

- o high power factor (approaching unity)
- o possibility to introduce a high-frequency insulating transformer
- o layout dependent high-frequency harmonics generation (EMI problems)
- o suitable for small and medium power levels

# **ACTIVE POWER FACTOR CORRECTION**



**DEFINITION**:

#### **Power Factor Corrector (PFC)**:

AC/DC converter with sinusoidal current absorption

(Current Proportional To Supply Voltage)

$$v_i = V_i \operatorname{sen}(\vartheta)$$
  
 $i_i = I_i \operatorname{sen}(\vartheta), \vartheta = \omega_i t$ 

The converter behaves like an equivalent resistance Rem given by:

$$R_{em} = \frac{V_i}{I_i}$$

#### ACTIVE POWER FACTOR CORRECTION: BASIC CONSIDERATIONS

Input power:

$$p_{i}(\vartheta) = v_{i}(\vartheta) \cdot i_{i}(\vartheta) = 2 \cdot V_{i,rms} I_{i,rms} \sin^{2}(\vartheta) =$$
$$= V_{i,rms} I_{i,rms} (1 - \cos(2\vartheta))$$

Considering unity efficiency:

$$\mathbf{V}_{i,rms} \cdot \mathbf{I}_{i,rms} = \mathbf{P} = \mathbf{V} \cdot \mathbf{I}$$

P = output power





**ASSUMPTIONS:** 

- o constant output voltage
- o unity efficiency
- o no low-frequency pulsating energy stored in the dc/dc stage

$$\Rightarrow p_i(\vartheta) = V \cdot \overline{i}'(\vartheta)$$

$$\overline{i}'(\vartheta) = \frac{p_i(\vartheta)}{V} = 2Isin^2(\vartheta)$$

 $\overline{i}'(\vartheta)$  = average value of  $i'(\vartheta)$  in a switching period



Voltage conversion ratio M':

$$\mathbf{M}'(\vartheta) = \frac{\mathbf{V}}{\mathbf{v}_{g}(\vartheta)} = \frac{\overline{\mathbf{i}}_{g}(\vartheta)}{\overline{\mathbf{i}}'(\vartheta)}$$

Load seen by the dc/dc stage:

$$\mathbf{R}'(\vartheta) = \frac{\mathbf{V}}{\overline{\mathbf{i}}'(\vartheta)} = \mathbf{M}'(\vartheta)^2 \cdot \frac{\mathbf{v}_g(\vartheta)}{\overline{\mathbf{i}}_g(\vartheta)} = \mathbf{M}'(\vartheta)^2 \cdot \mathbf{R}_{em}$$

$$R'(\vartheta) = \frac{R}{2 \cdot \sin^2(\vartheta)}$$
$$M'(\vartheta) = \frac{M}{|\sin(\vartheta)|}, M = \frac{V}{V_g}$$

For a PFC we have:

$$\frac{\mathbf{R'}(\vartheta)}{\mathbf{M'}^2(\vartheta)} = \mathbf{R}_{em}$$

a dc/dc converter when used as rectifier operates as a PFC with constant control if :  $M'(\vartheta) \propto \sqrt{R'(\vartheta)}$ 

OUTPUT FILTER DESIGN

Output filter capacitor current:

$$i_{c}(\vartheta) = \overline{i}'(\vartheta) - I = -I \cdot \cos(2\vartheta)$$

If  $\Delta V$  is the desired peak-to-peak output voltage ripple, then:

$$C \ge \frac{I}{\omega_i \Delta V}$$

# **PFC WITH INDUCTIVE FILTER**



**ASSUMPTIONS:** 

- o constant output current
- o unity efficiency
- o no low-frequency pulsating energy stored in the dc/dc stage

$$\overline{v}'(\vartheta) = \frac{p_i(\vartheta)}{I} = 2V\sin^2(\vartheta)$$
$$\overline{v}'(\vartheta) = \text{average value of } v'(\vartheta) \text{ in a switching period}$$

# **PFC WITH INDUCTIVE FILTER**



Voltage conversion ratio M':

$$\mathbf{M}'(\vartheta) = \frac{\overline{\mathbf{v}}'(\vartheta)}{\mathbf{v}_{g}(\vartheta)} = \frac{\overline{\mathbf{i}}_{g}(\vartheta)}{\mathbf{I}} = 2\mathbf{M} |\sin(\vartheta)|$$

Load seen by the dc/dc stage:

$$R'(\vartheta) = \frac{\overline{v}'(\vartheta)}{I} = 2R\sin^2(\vartheta)$$

### POWER FACTOR CORRECTORS: STANDARD CONFIGURATION

TWO STAGE PFC: CASCADE CONNECTION



PREREGULATORS: AC/DC converters with high power factor and poor output voltage regulation

LOW EFFICIENCY: THE SAME POWER IS PROCESSED TWICE

# **BASIC PREREGULATORS: BOOST TOPOLOGY**



#### CHARACTERISTICS:

- o Inherent input filter (low input current harmonic content)
- o Simple topology
- o high power factor
- o Output voltage greater than peak input voltage
- o no start-up or short circuit protection
- o no high-frequency insulation

### **BASIC PREREGULATORS: BOOST TOPOLOGY**

#### CCM OPERATION

#### Assumption:

switching frequency much greater than line frequency (quasi-stationary approach).



### **BASIC PREREGULATORS: BOOST TOPOLOGY**

#### **OPERATION AS DC/DC CONVERTER**

Voltage conversion ratio :

$$M = \frac{1}{1 - d}$$

d = duty-cycle

OPERATION AS AC/DC CONVERTER

In order to draw a sinusoidal current the duty-cycle must be modulated during the line period:

$$d(\vartheta) = 1 - \frac{V_g |\sin(\vartheta)|}{V}$$

(This is an approximation because CCM operation cannot be maintained during the whole line period)

BASIC PREREGULATORS: BUCK + BOOST TOPOLOGY



CHARACTERISTICS:

- o S<sub>1</sub> and D<sub>1</sub> provide start-up and short circuit protection
- o buck-mode operation for  $v_g$  higher than output voltage and boost mode-operation for  $v_g$  lower than output voltage
- o high conduction losses (four semiconductors in series)

# **BASIC PREREGULATORS: FLYBACK TOPOLOGY**



#### CHARACTERISTICS:

- o Simple topology
- o high power factor with constant duty-cycle in Discontinuous Conduction Mode (DCM) operation
- o inherent start-up and short circuit protection
- o high-frequency insulation transformer
- o high input current harmonic content

### **BASIC PREREGULATORS: FLYBACK TOPOLOGY**

#### DCM OPERATION

Main waveforms in a switching period



### **BASIC PREREGULATORS: FLYBACK TOPOLOGY**

#### DCM OPERATION

d = duty-cycle

L = transformer magnetizing inductance (primary side)

R = load resistance

 $T_s$  = switching period

 $M \propto \sqrt{R} \Rightarrow$  automatic PFC when used as rectifier

#### OPERATION AS AC/DC CONVERTER

Average input current:

$$\overline{i}_{g}(\vartheta) = \frac{v_{g}(\vartheta)}{L} \cdot d^{2}T_{s}$$

At constant duty-cycle and switching frequency the input current is sinusoidal

# CONTROL TECHNIQUES FOR SINGLE-PHASE PFC'S AND COMMERCIAL CONTROL IC'S

### **BOOST PREREGULATOR**

PEAK CURRENT CONTROL



Input current waveform



# PEAK CURRENT CONTROL

CHARACTERISTICS:

- o CONSTANT SWITCHING FREQUENCY
- O CONTINUOUS CONDUCTION MODE (CCM) OPERATION
  - low device current stresses
  - low RMS current
  - small EMI filter
- o POSSIBILITY TO SENSE ONLY SWITCH CURRENT
  - efficiency improvement
  - possibility to implement a pulse-by-pulse current limit
- o SUBHARMONIC OSCILLATIONS (for duty-cycle > 50%)
- o LINE CURRENT DISTORTION (increases for high line voltages, light load and high amplitude of compensating ramp)
- o COMMUTATION NOISE SENSITIVITY
- HARD REVERSE RECOVERY OF FREEWHEELING DIODE (increased commutation losses and EMI)

# **PEAK CURRENT CONTROL**

IDEAL REFERENCE CURRENT WAVEFORMS



DISTORTION REDUCTION TECHNIQUES

- ADDING A DC OFFSET TO CURRENT REFERENCE
   (function of both line voltage and load current)
- o PROGRAMMED DISTORTION CURRENT REFERENCE
  - line dependent DC offset
  - constant offset plus soft clamp

# **CURRENT CLAMPING CONTROL**



CHARACTERISTICS:

- o VERY SIMPLE CONTROL STRUCTURE
- LINE CURRENT DISTORTION BELOW 10% FOR LIMITED LOAD AND LINE VARIATIONS
- UNIVERSAL INPUT VOLTAGE OPERATION CANNOT BE EASILY ACCOMPLISHED

### **BOOST PREREGULATOR**

AVERAGE CURRENT CONTROL



#### Input current waveform



## **AVERAGE CURRENT CONTROL**

CHARACTERISTICS:

- o CONSTANT SWITCHING FREQUENCY
- o CONTINUOUS CONDUCTION MODE (CCM) OPERATION
  - low device current stresses
  - low RMS current
  - small EMI filter
- o COMPLEX CONTROL SCHEME
  - need of inductor current sensing
  - need of a multiplier
- o COMMUTATION NOISE IMMUNITY
- HARD REVERSE RECOVERY OF FREEWHEELING DIODE (increased commutation losses and EMI)
- o SEVERAL CONTROL IC'S AVAILABLE

## **BOOST PREREGULATOR**

HYSTERETIC CURRENT CONTROL



# **HYSTERETIC CURRENT CONTROL**

CHARACTERISTICS:

- o WIDE SWITCHING FREQUENCY VARIATION
- o CONTINUOUS CONDUCTION MODE (CCM) OPERATION
  - low device current stresses
  - low RMS current
  - small EMI filter
- o COMPLEX CONTROL SCHEME
  - need of inductor current sensing
  - need of a multiplier
- o COMMUTATION NOISE SENSITIVITY
- HARD REVERSE RECOVERY OF FREEWHEELING DIODE (increased commutation losses and EMI)
- SMALL INPUT CURRENT DISTORTION NEAR ZERO CROSSING OF LINE VOLTAGE TO AVOID HIGH SWITCHING FREQUENCY

### **BOOST PREREGULATOR**

BORDERLINE CONTROL (Operation at the boundary between DCM and CCM)



Input current waveform


# **BORDERLINE CONTROL**

CHARACTERISTICS:

- o AUTOMATIC PFC (CONSTANT SWITCH ON TIME)
- o VARIABLE SWITCHING FREQUENCY (function of load current and instantaneous line voltage)
- DISCONTINUOUS CONDUCTION MODE (DCM)
   OPERATION
  - high device current stresses
  - high RMS current
  - large EMI filter
  - reduced switch turn on losses and increased turn off losses
- o SIMPLE CONTROL SCHEME
  - no need for a multiplier (however some IC's make use of it)
  - need for sensing the instant of inductor current zeroing
- o SOFT RECOVERY OF FREEWHEELING DIODE

## **BOOST PREREGULATOR**

DISCONTINUOUS CURRENT PWM CONTROL



Input current waveform



# **DISCONTINUOUS CURRENT PWM CONTROL**

#### CHARACTERISTICS:

- o CONSTANT SWITCHING FREQUENCY
- OPERATION CONDUCTION MODE (DCM)
  - high device current stresses
  - high RMS current
  - large EMI filter
  - reduced switch turn on losses and increased turn off losses
- o NO NEED OF CURRENT SENSING
- o SIMPLE PWM CONTROL
- INPUT CURRENT DISTORTION (WITH BOOST CONVERTER)
  - distortion can be reduced by subtracting a fraction of rectified line voltage from the error voltage or by modulating the clock frequency with rectified line voltage
- o SOFT RECOVERY OF FREEWHEELING DIODE

# FLYBACK PREREGULATOR

## DCM OPERATION



#### Input current waveform



## **DCM OPERATION**

CHARACTERISTICS:

- o AUTOMATIC PFC (CONSTANT SWITCH ON TIME)
- o CONSTANT SWITCHING FREQUENCY
- o DCM OPERATION
  - high device current stresses
  - high RMS current
  - large EMI filter
  - reduced switch turn on losses and increased turn off losses
- o NO NEED OF CURRENT SENSING
- o SIMPLE PWM CONTROL
- o SOFT OF RECOVERY OF FREEWHEELING DIODE

# FLYBACK PREREGULATOR



## **CCM OPERATION - CHARGE CONTROL**

CHARACTERISTICS:

- o CONSTANT SWITCHING FREQUENCY
- o CONTINUOUS CONDUCTION MODE (CCM) OPERATION
  - low device current stresses
  - low RMS current
  - relatively large EMI filter (current ripple is small, but input current is discontinuous)
- o SUBHARMONIC OSCILLATIONS (for duty-cycle > 50%)
- o COMPLEX CONTROL SCHEME
  - need of inductor current sensing
  - need of a multiplier
- o COMMUTATION NOISE IMMUNITY
- HARD REVERSE RECOVERY OF FREEWHEELING DIODE (increased commutation losses and EMI)

# **CONTROL IC'S**

Constant frequency peak	ML4812 (Micro Linear)
current control	TK84812 (Toko)
Constant frequency	UC1854/A/B family (Unitrode)
average current control	UC1855 (Unitrode)
	TK3854A (Toko)
	ML4821 (Micro Linear)
	TDA4815, TDA4819 (Siemens)
	TA8310 (Toshiba)
	L4981A/B (SGS-Thomson)
	LT1248, LT1249 (Linear Tech.)
Hysteretic control	CS3810 (Cherry Semic.)
Borderline control	TDA4814, TDA4816,
	TDA4817, TDA4818 (Siemens)
	SG3561 (Silicon General)
	UC1852 (Unitrode)
	MC33261,
	MC33262(Motorola)
	L6560 (SGS-Thomson)
Two stage PFC with	UC1891/2/3/4 family (Unitrode)
average-current control	ML4824, ML4826 (Micro Linear)
	TK65030 (Toko)
Two stage PFC with	ML4819 (Micro Linear)
peak-current control	TK84819 (Toko)
Buck-boost constant	ML4813 (Micro Linear)
frequency automatic	
control	

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# INSULATED POWER FACTOR CORRECTOR TOPOLOGIES

DCM OPERATION



Sepic converter

#### DCM OPERATION

Inductor and diode current waveforms during a switching period for a Sepic converter



DCM operation = diode current zeroes during switch turn off interval

#### DCM OPERATION

Diode current = sum of inductor currents

#### CONSEQUENCE:

By choosing suitable values for inductors  $L_1$  and  $L_2$  it is possible to obtain a low high-frequency input current ripple

Simulated waveforms of a Sepic preregulator



## **CUK PREREGULATORS**

#### CHARACTERISTICS:

- o CONSTANT SWITCHING FREQUENCY
- o GOOD TRANSFORMER EXPLOITATION
- o DCM OPERATION
  - high device current stresses
  - small EMI filter
  - reduced switch turn on losses and increased turn off losses
  - soft diode turn off
- o SIMPLE CONTROL SCHEME
  - no need of current sensing
  - no need of multiplier
- POSSIBILITY OF MAGNETIC COUPLING (REDUCTION OF MAGNETIC STRUCTURE SIZE AND INPUT CURRENT RIPPLE)

## SEPIC PREREGULATORS

#### CHARACTERISTICS:

- o CONSTANT SWITCHING FREQUENCY
- o POOR TRANSFORMER EXPLOITATION
- o DCM OPERATION
  - high device current stresses
  - small EMI filter
  - reduced switch turn on losses and increased turn off losses
  - soft diode turn off
- o SIMPLE CONTROL SCHEME
  - no need of current sensing
  - no need of multiplier
- POSSIBILITY OF MAGNETIC COUPLING (REDUCTION OF MAGNETIC STRUCTURE SIZE AND INPUT CURRENT RIPPLE)

#### CCM OPERATION

EXAMPLE: Sepic converter with average current mode control



#### **PROBLEM**: design of the inner current loop

CCM OPERATION

Transfer function between duty-cycle and input current:  $G_{id}(s) = \frac{DV_D}{D'^2L'_2 + D^2L_1} \cdot \frac{1 + \frac{I_c}{V_D}\frac{D'}{D}L'_2 \cdot s + \frac{L'_2C'_1}{D} \cdot s^2}{s \cdot \left(1 + \frac{L_1L'_2C'_1}{D'^2L'_2 + D^2L_1} \cdot s^2\right)}$ 

where D'=1-D.

APPROXIMATION:  $G_{id}(s) \approx \frac{V_D}{sL_1}$  V<sub>D</sub> depends on input voltage (for the boost preregulator is:  $G_{id}(s) \approx \frac{V}{sL}$ , i.e. constant gain)

	Sepic	Cuk
$V_{\rm D}$	$V_g + V/n$	$V_g + V/n$
I <sub>c</sub>	$I_1 + I_2$	$I_1 + n I_2$
$C'_1$	C <sub>1</sub>	$C_a \cdot n^2 C_b$
		$C_a + n^2 C_b$
$L'_2$	L <sub>2</sub>	$L_2/n^2$

CCM OPERATION



a)  $\pi = \pi/2$ , b)  $\pi = \pi/18$ 

CCM OPERATION

A damping  $R_d$ - $C_d$  network across energy transfer capacitor  $C_1$  is used to properly shape the transfer function



## **INSULATED BOOST PREREGULATORS**

FULL-BRIDGE BOOST CONVERTER



TWO-SWITCH BOOST CONVERTER



A coupling winding to the input inductor is added to implement start-up and overload protection: during these conditions the converter operates in **flyback mode** 

## **INSULATED BOOST PREREGULATORS**

CHARACTERISTICS:

- DIFFICULT TRANSFORMER IMPLEMENTATION
  - low leakage inductance is essential
- NEED OF A SUITABLE CLAMP CIRCUIT
- HIGH VOLTAGE STRESS IN THE TWO-SWITCH IMPLEMENTATION



**OPERATION AS DC/DC CONVERTER** 

Voltage conversion ratio:

$$M = \frac{v_p}{v_g} = \frac{1}{\frac{\pi^2}{8} \cdot \left[1 - f_n^2\right] + \frac{j}{Q} \cdot f_n}, \qquad f_n = \frac{f}{f_r}$$
$$f_r = \frac{1}{2\pi\sqrt{L_r C_p}}, \qquad Q = R\sqrt{\frac{C_p}{L_r}}$$



#### GAIN CHARACTERISTICS

OPERATION AS AC/DC CONVERTER  

$$Q(\theta) = \frac{R'(\theta)}{Z_{r}} = \frac{R}{2\sin^{2}(\theta)} \cdot \frac{1}{Z_{r}}$$



- Near the zero crossing the circuit is lightly damped
   HIGH GAIN
- Near the peak of ac line the circuit is heavily damped
   LOW GAIN

OPERATION AS AC/DC CONVERTER

## CONSEQUENCE:

Good power factor (>90%) is obtained without active control of the line current.

#### NOTE:

The same result holds also for the series/parallel (LCC) resonant converter. For this converter, an active control is necessary to maintain zero voltage switching condition (operation must remain on the right side of resonant peaks in all operating conditions)

## FAST RESPONDING POWER FACTOR CORRECTOR TOPOLOGIES

#### **OBJECTIVES**:

- COMPACTNESS
- □ HIGH POWER FACTOR
- Image: TIGHT AND FAST OUTPUT VOLTAGE REGULATION
- □ HIGH-FREQUENCY INSULATION

## **TWO STAGE PFC: PARALLEL CONNECTION**



About 68% of input power goes directly to the output through stage 1, while stage 2 processes only 32% of input power

## **TWO STAGE PFC: PARALLEL CONNECTION**



- Boost converter controls power factor
- Forward converter regulates output
- C<sub>B</sub> stores energy
- C<sub>L</sub> is small

## **TWO STAGE PFC: PARALLEL CONNECTION**



 $i_{D2}$  or  $i_{D3}$ 

 $t_3$ 

 $T_{S}$ 

 $t_4$ 

• t<sub>2</sub> controls power factor

 $t_{1}$ 

• t<sub>3</sub> regulates output

## SINGLE STAGE PFC: PARALLEL POWER PROCESSING



- o need for several switches
- o complex control
- o discontinuous input current at least for a part of the line cycle (large EMI filter)

## SINGLE STAGE PFC: PARALLEL POWER PROCESSING

EXAMPLE: FLYBACK CONVERTER



- t<sub>2</sub> controls power factor
- t1 regulates output
- C<sub>B</sub> stores energy
- C<sub>L</sub> is small

## SINGLE STAGE PFC: PARALLEL POWER PROCESSING

EXAMPLE: FLYBACK CONVERTER







- t1 controls power factor
- t2 regulates output

# SINGLE STAGE PFC: BIFRED

(Boost Integrated with Flyback Rectifier/Energy storage/DC-DC



- DCM input current ensures high power factor
- duty-cycle regulates output
- C<sub>B</sub> stores energy
- CL is small

# SINGLE STAGE PFC: BIBRED

# (Boost Integrated with Buck Rectifier/Energy storage/DC-DC converter)



- DCM input current ensures high power factor
- duty-cycle regulates output
- C<sub>B</sub> stores energy
- $C_L$  is small

## SINGLE STAGE PFC: BIFRED, BIBRED

CHARACTERISTICS:

- o DCM OPERATION
  - high device current stresses
  - big EMI filter
- $\ensuremath{\mathsf{o}}$  Tank capacitor voltage  $v_B$  is load and line dependent
  - high device voltage stresses
  - limited load range

SOLUTIONS:

- o VARIABLE FREQUENCY CONTROL
  - trade-off between voltage stress and frequency range of control
- O DISCONTINUOUS OUTPUT CURRENT OPERATION

# SINGLE STAGE PFC: S<sup>2</sup>IP<sup>2</sup> FAMILY

(Single-Stage Isolated Power-factor corrected Power supplies)



- a) when the off voltages are the same
- b) when the off voltage of the left switch is always higher than the off voltage of the right switch
- c) when the off voltage of a switch can be higher or lower than the off voltage of the other switch
# SINGLE STAGE PFC: S<sup>2</sup>IP<sup>2</sup> FAMILY

EXAMPLE: BOOST+FLYBACK



# SINGLE STAGE PFC: S<sup>2</sup>IP<sup>2</sup> FAMILY

CHARACTERISTICS:

- SINGLE POWER STAGE WITH SINGLE HIGH-SPEED CONTROL LOOP (PWM CONTROL)
- o TANK CAPACITOR VOLTAGE  $\mathrm{V}_{\mathrm{B}}$  INDEPENDENT OF LOAD CURRENT
- DCM OPERATION OF BOTH PFC AND CURRENT-FED DC/DC CONVERTER STAGES
  - high device current stresses
  - big EMI filter

# SINGLE STAGE PFC: DITHER RECTIFIERS

### CONCEPT



Adding to the low-frequency input signal a high-frequency signal with amplitude higher than  $V_B$  increases the conduction interval of the dead-zone element (diode-capacitor rectifier)

# SINGLE STAGE PFC: DITHER RECTIFIERS

EXAMPLE: VOLTAGE DOUBLER + HALF-BRIDGE CONVERTER



The connection is moved from point A to point B. In this way, the high-frequency signal present on the inverter leg is added to the input voltage. An inductor is needed to smooth the input current.

# SINGLE STAGE PFC: DITHER RECTIFIERS

### EXAMPLE: VOLTAGE DOUBLER + HALF-BRIDGE CONVERTER

CHARACTERISTICS:

- o DCM OPERATION
  - high device current stresses
  - big EMI filter
- 0 TANK CAPACITOR VOLTAGE  $\mathrm{V}_{\mathrm{B}}$  is load and line dependent
  - high device voltage stresses
  - limited load range
- o VARIABLE FREQUENCY CONTROL

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# TECHNIQUES FOR IMPROVING OUTPUT VOLTAGE CONTROL SPEED

## **NATURE OF THE PROBLEM - 1**



To improve the dynamic response of power factor preregulators by manipulation of the output voltage feedback signal without additional sensing and with limited increase of control complexity

## NATURE OF THE PROBLEM - 2

Output voltage behavior:

$$v(t) = V_{DC} + \Delta v(t) = V_{DC} - \frac{P}{2\omega_i CV} \cdot \sin(2\omega_i t)$$

The voltage error signal contains a low-frequency ripple at twice the

line frequency

#### CONSEQUENCE:

the bandwidth of the voltage loop must be kept below the

line frequency in order to avoid input current distortion



The low-pass filter provides a voltage proportional to the RMS input voltage which is squared and used in the multiplier to divide the current reference

this avoids heavy compensating actions by the voltage error amplifier during line transients

# **CONTROL SCHEME WITH NOTCH FILTER**



A notch filter tuned at twice the line frequency is inserted in the feedback path in order to remove the output voltage low-frequency ripple from the feedback signal

#### COMMENTS:

- □ the filter must be well tuned with high quality factor
- □ the bandwidth is limited below twice the line frequency

## **CONTROL SCHEME WITH SAMPLE & HOLD**



By sampling the output voltage error signal at a rate equal to the voltage ripple near zero crossing of the line voltage, the average output voltage is sensed.

#### COMMENTS:

- a high power factor is maintained in both transient and steady-state conditions
- □ the bandwidth is limited below twice the line frequency

# CONTROL SCHEME WITH RIPPLE COMPENSATION $\Delta v(t) = -\frac{P}{2\omega_i CV} \cdot \sin(2\omega_i t)$

The output voltage ripple is estimated and subtracted to the feedback signal so that the error amplifier processes a ripple-free signal

Under unity power factor condition, input power is given by:

$$p_i(t) = \eta P - \frac{\eta P}{2} \cdot \cos(2\omega_i t)$$

where h is converter efficiency.

Error signal  $\Delta v(t)$  can be estimated from input power signal through:

Elimination of DC component
Phase shifting of ninety degrees
Multiplication by a proper gain

## CONTROL SCHEME WITH RIPPLE COMPENSATION



$$G_{c}(s) = K_{c} \cdot s$$

COMMENTS:

- $\Box$  in the presence of distorted input voltage, network  $G_c(s)$  turns out to be complicated
- a second multiplier is needed
- □ the bandwidth can be increased above twice the line frequency

## **CONTROL SCHEME WITH "REGULATION BAND"**



The current reference amplitude is kept constant as long as the output voltage remains within a defined regulation band. When the output voltage goes outside of this band a high gain controller changes rapidly the current reference amplitude so as to bring the output voltage back into the regulation band

#### COMMENTS:

- correct average output voltage is obtained only at nominal condition in which the voltage ripple amplitude is equal to the dead zone amplitude
- □ slow input current dynamic response at load step changes

# **CONTROL SCHEME WITH "REGULATION BAND"**

## **REGULATION BAND APPROACH TYPE 2**



In order to overcome the problem represented by the steady-state error on the output voltage of the previous control technique, a low-bandwidth PI controller can be used which ensures stability and no DC errors. When the output voltage goes outside the band, the gain of the voltage error amplifier is increased in order to enhance the corrective action

## **COMPARISON OF CONTROL STRATEGIES**

#### **BOOST POWER FACTOR PREREGULATOR**

**TABLE 1** - Converter parameters

Vg=220VRMS	V=380V	f <sub>S</sub> =50kHz	
L=2mH	C=470μF	P=600W	

Error voltage amplifier transfer function

$$G_{v}(s) = \frac{K_{I}}{s} \left(1 + \frac{s}{\omega_{z}}\right)$$

**TABLE 2** - Error voltage amplifier parameter values

	S.C.	N.F.	S.H.	B.#1	B.#2	R.C.
KĮ	8.8	73.4	8.7	100∙K <sub>a</sub>	8.8∙Kd	223
ωΖ	69.2	188.5	62.8	166.7	69.2	354.4

 $(K_a=13.8, K_b=1, K_d=21.4)$ 

S.C. = Standard Control

S.H. = Sample & Hold

B.#2 = Regulation Band TYPE 2

N.F. = Notch Filter

B.#1 = Regulation Band TYPE 1

R.C. = Ripple Compensation

# STANDARD CONTROL





Rectified input current

## **SAMPLE & HOLD**



# **REGULATION BAND TYPE 1**



## **REGULATION BAND TYPE 2**



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## **RIPPLE COMPENSATION**



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# BASICS OF SOFT-SWITCHING TECHNIQUES

# WHY SOFT TRANSITIONS?

- o EMI (ELECTRO-MAGNETIC INTERFERENCE) REDUCTION
  - compliance with EMC (Elettro-Magnetic Compatibility) standards
  - input filter size reduction
- o INCREASE OF SWITCHING FREQUENCY
  - converter size reduction
  - fast dynamic (high loop bandwidth)
- o INCREASE OF EFFICIENCY

# SOFT SWITCHING SOLUTIONS

#### o QUASI-RESONANT OR RESONANT TOPOLOGIES

- increased current and/or voltage stresses
- increased conduction losses (resonant components in series with main power path)
- difficulties to maintain soft-switching condition for wide line and load ranges
- o AUXILIARY CIRCUIT
  - "PWM like" current and voltage waveforms
  - need of an auxiliary switch
  - little increase of control complexity
  - soft-switching condition easily maintained for wide line and load ranges

## REVERSE RECOVERY PROBLEM IN BOOST RECTIFIERS



- o INCREASED SWITCHING LOSSES
- o INCREASED EMI
- o INCREASED DEVICE CURRENT STRESSES



## ASSUMPTIONS:

- constant boost inductor current during commutation
- constant output voltage

Main waveforms in a switching period



PRINCIPLE OF OPERATION (T0-T1)





PRINCIPLE OF OPERATION (T1-T2)





PRINCIPLE OF OPERATION (T2-T3)





PRINCIPLE OF OPERATION (T<sub>3</sub>-T<sub>4</sub>)





PRINCIPLE OF OPERATION (T<sub>4</sub>-T<sub>5</sub>)





PRINCIPLE OF OPERATION (T5-T6)



PRINCIPLE OF OPERATION (T<sub>6</sub>-T<sub>0</sub>)



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CHARACTERISTICS:

- SOFT-SWITCHING FOR BOTH MAIN SWITCH AND RECTIFIER
- o CONSTANT FREQUENCY OPERATION
- o HIGH EFFICIENCY
- o ZERO-CURRENT TURN ON OF THE AUXILIARY SWITCH
- HARD TURN OFF OF THE AUXILIARY SWITCH

A "flying" capacitor  $C_1$  is added in order to achieve soft turn off of the auxiliary switch.






An autotransformer is added in series to the resonant inductor acting like a voltage source to bring the resonant current to zero after the commutation

 $\Rightarrow$  S<sub>r</sub> turns off at zero current

# SMALL-SIGNAL MODELING

### SMALL-SIGNAL MODEL OF A PFC OPERATING IN CCM



### SMALL-SIGNAL MODEL FOR A PFC OPERATING IN CCM

Under PFC conditions the input current is sinusoidal and its RMS value depends on control voltage  $V_c$ :

$$\mathbf{i}_{i} = \frac{\mathbf{v}_{i}}{k} \cdot \mathbf{v}_{c}$$

Substituting we obtain:

$$\frac{\mathbf{v}_{i}^{2}}{\mathbf{k}} \cdot \mathbf{v}_{c} = \mathbf{v}_{0} \cdot \mathbf{i}_{0}$$

After perturbation and linearization (small-signal approximation):

$$\hat{\mathbf{i}}_{0} = \frac{2\mathbf{V}_{i}\mathbf{V}_{c}}{\mathbf{k}\mathbf{V}_{0}} \cdot \hat{\mathbf{v}}_{i} + \frac{\mathbf{V}_{i}^{2}}{\mathbf{k}\mathbf{V}_{0}} \cdot \hat{\mathbf{v}}_{c} - \frac{\mathbf{I}_{0}}{\mathbf{V}_{0}} \cdot \hat{\mathbf{v}}_{0}$$
$$\hat{\mathbf{i}}_{0} = \frac{2\mathbf{M}}{\mathbf{r}_{0}} \cdot \hat{\mathbf{v}}_{i} + \frac{\mathbf{V}_{i}}{\mathbf{k}\mathbf{M}} \cdot \hat{\mathbf{v}}_{c} - \frac{1}{\mathbf{r}_{0}} \cdot \hat{\mathbf{v}}_{0}$$
$$\mathbf{M} = \frac{\mathbf{V}_{0}}{\mathbf{V}_{i}} \quad , \quad \mathbf{r}_{0} = \frac{\mathbf{V}_{0}}{\mathbf{I}_{0}}$$

where

### SMALL-SIGNAL MODEL FOR A PFC OPERATING IN CCM

In the same way, from the power balance, we obtain:

$$\hat{\mathbf{i}}_{i} = \frac{\mathbf{V}_{i}}{\mathbf{k}} \cdot \hat{\mathbf{v}}_{c} + \frac{\mathbf{M}^{2}}{\mathbf{r}_{0}} \cdot \hat{\mathbf{v}}_{i}$$



М	r <sub>i</sub>	g <sub>i</sub>	r <sub>0</sub>	9f	g <sub>c</sub>
$\frac{V_0}{V_i}$	$\frac{r_o}{M^2}$	$\frac{V_i}{k}$	$\frac{V_0}{I_0}$	$\frac{2M}{r_o}$	$\frac{V_i}{kM}$

### SMALL-SIGNAL MODEL FOR A PFC OPERATING IN CCM

TRANSFER FUNCTION BETWEEN CONTROL VOLTAGE AND OUTPUT VOLTAGE

$$G_{vc}(s) = \frac{\hat{v}_0}{\hat{v}_c} = g_c \cdot \frac{r_p}{1 + sCr_p}$$
$$r_p = \frac{r_0 \cdot R_L}{r_0 + R_L}$$

 $r_p=R_L/2$  resistive load

r<sub>p</sub>=R<sub>L</sub> constant current load

 $r_p = \infty$  constant power load

### SMALL-SIGNAL MODEL FOR A PFC OPERATING IN DCM (FLYBACK, CUK, SEPIC)



### SMALL-SIGNAL MODEL FOR A PFC OPERATING IN DCM

Under PFC conditions the input current is sinusoidal and its RMS value depends on duty-cycle  $\delta$ :

$$i_i = \frac{T_s v_i}{2L_{eq}} \cdot \delta^2$$

where  $L_{eq}$  depends on converter topology. Substituting we obtain:

$$\frac{\mathbf{v}_{i}^{2}\mathbf{T}_{s}}{2\mathbf{L}_{eq}}\cdot\boldsymbol{\delta}^{2}=\mathbf{v}_{0}\cdot\mathbf{i}_{0}$$

After perturbation and linearization (small-signal approximation):

$$\hat{\mathbf{i}}_{0} = \frac{2\mathbf{V}_{i}\mathbf{Y}_{i}\mathbf{D}^{2}}{\mathbf{V}_{0}} \cdot \hat{\mathbf{v}}_{i} + \frac{2\mathbf{V}_{i}^{2}\mathbf{Y}_{i}\mathbf{D}}{\mathbf{V}_{0}} \cdot \hat{\boldsymbol{\delta}} - \frac{\mathbf{I}_{0}}{\mathbf{V}_{0}} \cdot \hat{\mathbf{v}}_{0}$$
$$\mathbf{Y}_{i} = \frac{\mathbf{T}_{s}}{2\mathbf{L}_{eq}}$$

where

### SMALL-SIGNAL MODEL FOR A PFC OPERATING IN DCM

$$\hat{i}_0 = \frac{2Y_i D^2}{M} \cdot \hat{v}_i + \frac{2V_i Y_i D}{M} \cdot \hat{\delta} - \frac{1}{r_0} \cdot \hat{v}_0$$
  
e  $M = \frac{V_0}{V_i}$ ,  $r_0 = \frac{V_0}{I_0}$ 

where

In the same way, from the power balance, we obtain:

 $\hat{i}_i = 2V_iY_iD\cdot\hat{\delta} + D^2Y_i\cdot\hat{v}_i$ 



### SMALL-SIGNAL MODEL FOR A PFC OPERATING IN DCM

#### MODEL PARAMETERS

М	r <sub>i</sub>	9 <sub>i</sub>	r <sub>0</sub>	9 <sub>f</sub>	9 <sub>c</sub>
$\frac{V_0}{V_i}$	$\frac{1}{D^2 Y_i}$	2DV <sub>i</sub> Y <sub>i</sub>	$\frac{V_0}{I_0}$	$\frac{2Y_iD^2}{M}$	$\frac{2V_iY_iD}{M}$

	FLYBACK	CUK	SEPIC
L <sub>eq</sub>	L	$\frac{L_1 \cdot L_2}{n^2 L_1 + L_2}$	$\frac{L_1 \cdot L_2}{L_1 + L_2}$

n=transformer turns ratio (N<sub>2</sub>/N<sub>1</sub>)

TRANSFER FUNCTION BETWEEN DUTY-CYCLE AND OUTPUT VOLTAGE

$$G_{v}(s) = \frac{\hat{v}_{0}}{\hat{\delta}} = g_{c} \cdot \frac{r_{p}}{1 + sCr_{p}}$$
$$r_{p} = \frac{r_{0} \cdot R_{L}}{r_{0} + R_{L}}$$

# DESIGN OF BOOST PFC OPERATING IN CCM WITH AVERAGE CURRENT MODE CONTROL

# **POWER STAGE SCHEME**



CHARACTERISTICS:

Input voltage: $V_{in} = 90-260V_{RMS}$ Output voltage: $V_0 = 380V$ Output power: $P_0 = 600W$ Switching frequency: $f_S = 70kHz$ 

1) Inductor peak current (average value in a switching period)  $P_{_{O}}=\eta\cdot P_{_{g}}$ 

where  $\eta$  is converter efficiency

$$\eta \cdot \frac{I_{L} \cdot V_{g}}{2} = P_{o} \implies \hat{I}_{L} = \frac{2P_{o}}{\eta \hat{V}_{g}}$$
 (1)

Worst case: minimum input voltage

$$\hat{I}_{L} = \frac{2 \cdot 600}{0.95 \cdot \sqrt{2} \cdot 90} = 9.92 \text{A}$$

#### 2) Input inductor value

Duty-cycle in CCM:  

$$\delta(\vartheta) = 1 - \frac{V_{g}(\vartheta)}{V_{o}}, \delta = \frac{t_{on}}{T_{s}}; \vartheta = \omega_{i}t$$
(2)
Peak-to-peak input current ripple:

$$\Delta i_{L}(\vartheta) = \frac{V_{g}(\vartheta)}{L} \cdot t_{on} = \frac{V_{g}(\vartheta)}{f_{s} \cdot L} \cdot \delta(\vartheta)$$
(3)

The maximum ripple occurs at half the input voltage peak. From the allowed ripple the input inductor value is found.

(example: relative ripple =  $30\% \implies L = 0.46$  mH.

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# **POWER STAGE DESIGN**

3) Output capacitor value

$$C = \frac{I_o}{\omega_i \Delta V_o}$$
(4)

where  $\Delta V_0$  is the desired peak-to-peak voltage ripple and  $I_0$  is the output current.

(Example:

relative ripple  $<5\% \implies C > 260 \ \mu\text{F}$ , we use C=470 $\mu\text{F}$ )

4) Switch peak current  

$$\hat{i}_{s} = \hat{I}_{L} + \frac{\Delta i_{L} (\pi/2)}{2} = 10.9A$$
(5)

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# **POWER STAGE DESIGN**

5) Switch RMS current



RMS current is determined by first averaging the switch current over a switching period and second averaging over the line period. Neglecting the inductor current ripple we obtain:

$$\begin{split} \frac{I_{s,rms}}{I_o} &\cong 2M \sqrt{\frac{1}{2} - \frac{1}{M} \cdot \frac{4}{3\pi}} \end{split} \tag{6}$$
 where  $M = \frac{V_o}{V_g}$  is voltage conversion ratio  
Considering the minimum input voltage we obtain:  $I_{s,rms} = 5.63A$ .

6) Freewheeling diode peak current (average value)  

$$\hat{I}_{D,avg} = 2 \cdot I_o = 3.16A$$
(7)



#### IC: SGS-THOMSON L4981A

#### COMPONENT VALUES

$V_{CC} = 18V$	$R_7 = 3.3 \text{ k}\Omega$	$R_{13} = 18 \text{ k}\Omega$	C4 = 100 nF
R2 = 150 kΩ	$R_8 = 3.3 \text{ k}\Omega$	$R_{14} = 5.6 k\Omega$	C5 = 1 nF
R3 = 1 MΩ	$Rg = 47 \ k\Omega$		C <sub>6</sub> = 68 pF
R4 = 560 kΩ	$R_{10} = 33 \Omega$	C <sub>1</sub> = 15 nF	C7 = 10 μF
$R_5 = 33 \text{ k}\Omega$	$R_{11} = 33 \ k\Omega$	C <sub>2</sub> = 220 nF	C8 = 1 nF
$R_6 = 1.2 M\Omega$	$R_{12} = 1.5 M\Omega$	C3 = 220 nF	C9 = 10 μF

IC: SGS-THOMSON L4981A



1) Shunt resistance RS:

Choosing  $R_s = 0.054\Omega$  the power loss is:

$$P_{R_s} = R_s \cdot \frac{\hat{I}_L^2}{2} = 2.65W$$
 (8)

2) Switching frequency:

C<sub>8</sub> and R<sub>11</sub> determine the switching frequency:  $f_s = \frac{2.4}{C_8 \cdot R_{11}}, \quad hertz$ 

Choosing C<sub>8</sub>=1nF gives R<sub>11</sub>=33k $\Omega$ 

3 Reference current IAC:

$$I_{AC} = \frac{\hat{V}_g}{R_6}$$
(10)

The suggested value for R<sub>6</sub> is 1.2M $\Omega$ . Correspondingly, I<sub>AC</sub> is between 106 $\mu$ A at minimum line voltage and 306 $\mu$ A at maximum line voltage.

(9)

4) Feedforward voltage V<sub>RMS</sub>:

R<sub>3</sub>, C<sub>3</sub>, R<sub>4</sub>, R<sub>5</sub>, C<sub>4</sub> form a low pass filter which must give at pin 7 a DC voltage between 1.5V and 6.5V. Suggested values are: R<sub>3</sub>=1M $\Omega$ , R<sub>4</sub>=560k $\Omega$ , R<sub>5</sub>=33k $\Omega$ , C<sub>3</sub>=220nF, C<sub>4</sub>=100nF:

$$V_{RMS} = \frac{R_5}{R_3 + R_4 + R_5} \cdot \frac{2}{\pi} \cdot \hat{V}_g = \alpha \cdot \hat{V}_g = 1.68 \div 4.85V \quad (11)$$

This low-pass filter must give a good attenuation at twice the line frequency.

5) Peak current limiter:

We choose I<sub>pk,lim</sub>=11A:  

$$I_{pk,lim} = 100 \mu A \cdot \frac{R_{14}}{R_S}$$
(12)

from which  $R_{14}=5.6k\Omega$ .

6) R7 and R8 values:

If the current error amplifier has enough gain at line frequency we have:

$$\mathbf{R}_{S} \cdot \mathbf{I}_{L} = \mathbf{R}_{7} \cdot \mathbf{I}_{\text{MULT-OUT}}$$
(13)

where IMULT-OUT is the multiplier output current, which is related to the output voltage of the voltage error amplifier VA-OUT by:

$$I_{MULT-OUT} = I_{AC} \cdot \frac{V_{A-OUT} - 1.28}{V_{RMS}^2}$$
(14)

which is valid if pin 6 ( $V_{LFF}$ ) is connected to pin 11 ( $V_{REF}$ ).

Imposing that the maximum input current occurs with a voltage VA-OUT=5V, we obtain  $R_7=R_8=3.3k\Omega$ .

7) Over voltage protection:  

$$V_{o,max} = V_{REF} \cdot \left(1 + \frac{R_{12}}{R_{13}}\right)$$
(15)

Choosing R<sub>12</sub>=1.5M $\Omega$  and R<sub>13</sub>=18k $\Omega$  gives V<sub>0,max</sub>=425V.

#### 8) Soft-start:

Connecting a capacitor between pin 12 and ground a ramp voltage is generated which causes the duty-cycle to vary from minimum to nominal value.

Suggested value:  $C_9 = 10\mu F$ .

9) Feedback signal divider:  

$$V_{REF} = V_{o} \cdot \frac{R_{p2}}{R_{p1} + R_{p2}}$$
(16)

 $R_{p1}=1M\Omega e R_{p2}=12k\Omega + 4.7k\Omega$  trimmer.

As suggested a filter capacitor  $C_7 = 10\mu F$  is connected between pin 11 (VREF) and ground.

# **CURRENT REGULATOR DESIGN**



Approximated power stage transfer function (between duty-cycle and input current) for frequency above the output filter corner frequency:

$$G_{i}(s) = \frac{i_{g}(s)}{d(s)} = \frac{V_{o}}{sL}$$
(17)

# **CURRENT REGULATOR DESIGN**

The current loop transfer function is:

$$T_{i}(s) = \frac{V_{o}}{sL} \cdot \frac{1}{V_{osc}} \cdot R_{s} \cdot G_{ri}(s)$$
(18)

where,  $V_{OSC} = 5V$  is the amplitude of the internal ramp of the PWM generator.

Current error amplifier: 
$$G_{ri}(s) = \frac{m(s)}{\epsilon_i(s)} = \frac{\omega_{ri}}{s} \cdot \frac{(1 + s\tau_{zi})}{(1 + s\tau_{pi})}$$
 (19)

where

$$\omega_{\rm ri} = \frac{1}{R_8 (C_5 + C_6)} \approx \frac{1}{R_8 C_5} \text{if } C_5 >> C_6 \tag{20}$$

$$\tau_{zi} = R_9 \cdot C_5 \tag{21}$$

$$\tau_{\rm pi} = R_9 \cdot \frac{C_5 \cdot C_6}{C_5 + C_6} \approx R_9 \cdot C_6 \quad \text{if } C_5 >> C_6 \tag{22}$$

# **CURRENT REGULATOR DESIGN**

If  $f_{zi} < f_c < f_{pi}$  where  $f_c$  is the crossover frequency, then:

$$\left|G_{ri}(j\omega_{c})\right| \approx \frac{\kappa_{9}}{R_{8}}$$
(23)

$$T_{i}(j\omega_{c}) = 1 \Longrightarrow \frac{R_{9}}{R_{8}} = \frac{2\pi f_{c} \cdot L \cdot V_{osc}}{R_{s} \cdot V_{o}}$$
(24)

As far as the phase is concerned:

$$\angle T_{i}(j\omega_{c}) = -90^{\circ} - 90^{\circ} + \operatorname{arctg}\left(\frac{f_{c}}{f_{zi}}\right) - \operatorname{arctg}\left(\frac{f_{c}}{f_{pi}}\right) = m_{\phi} - 180^{\circ} (25)$$

where  $m_{\Phi}$  is the desired phase margin.

Given  $f_C$  , the phase margin and choosing  $f_S/2{<}f_{pi}{<}f_S$  so as to attenuate the high-frequency ripple Rg, C5 and C6 values are obtained.

Example:  $f_C$  = 15 kHz,  $f_{pi}$  = 50 kHz and  $~m_{\phi}$  = 60°  $\Rightarrow$   $f_{Zi}$  = 3.5kHz, R9=47k\Omega, C5=1nF, C6=68pF.

# **VOLTAGE REGULATOR DESIGN**

Transfer function between control voltage and output voltage:

$$G_{v}(s) = \frac{V_{0}(s)}{V_{c}(s)} = g_{c} \cdot \frac{r_{p}}{1 + sCr_{p}}$$
(26)

where,

$$r_{p} = \frac{r_{o} \cdot Z_{L}}{r_{o} + Z_{L}}, \quad g_{c} = \frac{V_{g,rms}}{k \cdot M}, \quad r_{o} = \frac{V_{o}}{I_{o}}, \quad M = \frac{V_{o}}{V_{g,rms}}$$
(27)

$Z_L = R_L = r_O$	resistive load
$Z_L = Y$	constant current load
ZL = - RL	constant power load

and k is defined by the relation:

$$I_{g,rms} = \frac{V_{g,rms}}{k} \cdot v_c$$
(28)

In the L4981A controller, feedforward term VRMS eliminates the dependence of gain  $g_c$  from input voltage.

### **VOLTAGE REGULATOR DESIGN**

From eqs. (13-14) we can write  $(R_M=R_7)$ :

$$I_{g,RMS} = \frac{R_7}{R_S} \cdot I_{MULT-OUT} = \frac{R_7}{R_S} \cdot \frac{V_{g,RMS}}{R_6} \cdot \frac{V_{A-OUT} - 1.28}{V_{RMS}^2}$$

$$= \frac{R_7}{R_S} \cdot \frac{V_{g,RMS}}{R_6} \cdot \frac{V_{A-OUT} - 1.28}{2\alpha^2 V_{g,RMS}^2}$$
(29)

which corresponds to (28) if:

$$k = 2R_{6} \cdot \frac{R_{S}}{R_{7}} \cdot \left(\frac{2}{\pi} \cdot \frac{R_{5}}{R_{3} + R_{4} + R_{5}}\right)^{2} \cdot V_{g,RMS}^{2}$$
(30)

### **VOLTAGE REGULATOR DESIGN**

The voltage regulator transfer function is:  $G_{rv} = \frac{V_{C}(s)}{V_{C}(s)} = \frac{\omega_{rv}}{(1 + \tau_{zv})}$ 

$$G_{rv}(s) = \frac{c(r)}{\varepsilon_v(s)} = \frac{1}{s} \cdot \frac{c(r)}{(1 + s\tau_{pv})}$$
(31)

where

$$\omega_{\rm rv} = \frac{R_{\rm p2}}{R_{\rm p1} + R_{\rm p2}} \cdot \frac{1}{C_1 + C_2} \cdot \frac{1}{R_1} \approx \frac{V_{\rm REF}}{V_{\rm o}} \cdot \frac{1}{C_2} \cdot \frac{1}{R_1} \quad (C_2 >> C_1)$$
(32)

with 
$$R_1 = R_{p1} || R_{p2}$$
  
 $\tau = R_{p1} C$ 
(33)

$$\tau_{\rm zv} = R_2 \cdot C_2$$
(33)  
$$\tau_{\rm pv} = R_2 \cdot (C_1 //C_2) \approx R_2 \cdot C_1 \sec C_2 >> C_1$$
(34)

Considering a crossover frequency higher than the power stage pole we have:

$$\left|\frac{g_{c}}{j\omega_{c}C}\cdot\omega_{rv}\tau_{zv}\right| = 1$$
(35)

Choosing  $f_c = 10 \div 20$  Hz,  $f_i < f_{pv} < 2f_i$  and a suitable phase margin, the regulator parameters can be calculated.

Example:  $f_C$  = 20Hz,  $f_{PV}$  = 70Hz and  $~m_{\phi}$  = 60°  $\Rightarrow$   $f_{ZV}$  = 5Hz, R2=150k\Omega,C1=15nF, C2=220nF.

# DESIGN OF A SEPIC PFC OPERATING IN DCM

### POWER STAGE SCHEME



#### PROTOTYPE PARAMETERS

V <sub>g</sub> = 220 V <sub>rms</sub> ± 20%	V = 36 V	P = 100W	f <sub>S</sub> = 100 kHz
L <sub>2</sub> = 74 μH	C <sub>1</sub> = 0.68 μF	C <sub>2</sub> = 10 μF	n = 0.5

1) Operation as dc/dc converter.

The voltage conversion ratio is:

$$\begin{split} M &= \frac{V}{V_g} = \frac{I_g}{I} = n \cdot \frac{D}{1-D} \end{split} \tag{CCM} \\ M &= \frac{V}{V_g} = \frac{I_g}{I} = \frac{D}{\sqrt{K}} \pmod{DCM} \end{split}$$

where  $n=N_2/N_1$  is transformer turns ratio, D is duty-cycle and parameter K is given by:

$$K = \frac{2L_e}{RT_s}$$
, with  $L_e = \frac{L_1L_2}{L_1 + L_2}$ 

In the above equations  $T_{\rm s}$  is the switching period and  $L_{\rm 2}$  is the transformer magnetizing inductance.

Critical parameter:

$$K_{crit} = \frac{(1-D)^2}{n^2} = \frac{1}{(n+M)^2} \begin{cases} K > K_{crit} \Longrightarrow CCM \\ K < K_{crit} \Longrightarrow DCM \end{cases}$$

Average inductor current I\_2 :  $I_2 = n \cdot i_D = n \cdot I$ 



Inductor current waveforms in DICM

2) Operation as a rectifier.

When operating as a rectifier, the dc input voltage  $\mathbf{V}_{\rm g}$  is substituted by the rectified line voltage:

$$v_{g}(\theta) = V_{g} \cdot |\sin(\theta)|$$
  
where  $\theta = \omega_{i}t$ . Consequently, the voltage conversion ratio becomes:

$$m(\theta) = \frac{V}{v_{g}(\theta)} = \frac{M}{|\sin(\theta)|}$$

where M=V/V<sub>g</sub>.

Under power factor correction conditions:  $i_2(\theta) = n \cdot i_D(\theta) = n \cdot 2Isin^2(\theta)$ 

The apparent load  $r(\boldsymbol{q})$  seen at the secondary side of the transformer is given by:

$$r(\theta) = \frac{V}{i_{D}(\theta)} = \frac{R}{2\sin^{2}(\theta)}$$
  
Thus the parameter k becomes function of angle q  
$$k(\theta) = \frac{2L_{e}}{r(\theta)T_{s}} = 2K_{a}\sin^{2}(\theta), K_{a} = \frac{2L_{e}}{RT_{s}}$$
$$k_{crit}(\theta) = \frac{\sin^{2}(\theta)}{(M + n \cdot |\sin(\theta)|)^{2}}$$

For the converter to operate in DCM the following condition must be satisfied:

$$\mathbf{K}_{\mathrm{a}} < \frac{1}{2(\mathbf{M} + \mathbf{n} \cdot |\sin(\theta)|)^2}$$

The average current drawn by the converter, at constant duty-cycle and switching frequency, is sinusoidal and in phase with the line voltage and is given by

$$i_{g}(\theta) = \frac{D^{2}T_{s}}{2L_{e}} \cdot v_{g}(\theta) = \frac{v_{g}(\theta)}{R_{em}}$$

where,

 $R_{em} = \frac{2\,L_e}{D^2 T_s}\,$  is the emulated resistance.

The converter duty-cycle results:  $D=M\cdot \sqrt{2K_a}$ 

#### INPUT DATA:

- $\hfill\square$  minimum and maximum input voltage peak value  $V_{gmin},$   $V_{gmax};$
- output voltage V;
- output power P;
- $\Box$  switching frequency  $f_s$ ;
- initial value for transformer turns ratio n.

#### DESIGN PROCEDURE:

- calculate minimum and maximum voltage conversion ratio
   M<sub>min</sub>, M<sub>max</sub>
- evaluate K<sub>a</sub> for  $\pi = \pi / 2$  and M<sub>max</sub> (minimum line voltage)

$$K_a = \alpha \cdot \frac{1}{2(M_{max} + n)^2}, \alpha = 0.9 \div 0.95$$

- □ find the value of inductance L<sub>e</sub> from K<sub>a</sub> definition
- □ find the value of duty-cycle D;
- calculate the value of inductances L<sub>1</sub> and L<sub>2</sub> from L<sub>e</sub> and the desired input current ripple
- calculate device current and voltage stresses as well as peak inductor currents;
- repeat the procedure for different values of transformer turns ratio;
- choose the solution which best meets device ratings.

#### NOTE:

particular attention must be given to the selection of capacitor  $C_1$ . Three constrains must be taken into account:

- $\Box$  voltage  $u_1$  must follow the input voltage shape without distorsion
- its voltage ripple must be as low as possible