A Double-Line-Frequency Commutated Rectifier Complying with IEC 1000-3-2 Standards

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Abstract- This paper presents a high power factor rectifier, based on a modified conventional rectifier with passive L-C filter, which utilizes a line-frequency-commutated switch and a small auxiliary circuit in order to improve both harmonic content of the input current and power factor, thus allowing compliance with IEC 1000-3-2 standards. Being the switch turned on and off only twice per line period, the associated losses are very small. Moreover the limited di/dt and dv/dt considerably reduce the high-frequency noise emission, thus avoiding heavy EMI filters. The switch operation results in a boost action, which compensates for the filter inductor voltage drop, thus providing output voltage stabilization against load variations. Compared with other similar approaches, the presented topology can achieve higher power levels with a reasonable overall magnetic component size.

I. INTRODUCTION

High quality rectifiers (also called power factor correctors - PFCs) are rapidly substituting conventional frontend rectifiers due to harmonic limits imposed by international standards like IEC-1000-3-2 [1]. Such high-frequency PFCs provides very high power factors, many times much more then required by the standards and a good output voltage regulation, at the expense of an increase of the overall ac-to-dc converter size and cost. For these reasons, some large volume applications still use standard low cost - high reliable rectifiers with passive filters in order to improve the quality of the current drawn from the line, even if the volume of the reactive components needed becomes rapidly prohibitive as the power increases [2].

Performance improvements of rectifiers with passive filters were achieved in [3] and [4] by adding another capacitor inside the rectifier or even another diode. However, such solutions are useful for an input power up to 300W, and, being completely passive, they do not provide output voltage stabilization against load variations.

The active solution presented in [5-6] is, actually, a boost converter operated at line frequency which provides compliance with the standard as well as some degree of output voltage stabilization. However, as the power increases, the inductor value needed makes the solution progressively less interesting.

This paper presents another double-line-frequency commutated high-power factor rectifier capable of maintaining IEC 1000-3-2 compliance even at high power levels with smaller overall magnetic components as compared to previous solutions. Similarly to the low-frequency boost, it provides output voltage stabilization against load variations. Moreover, the low switching frequency allows reduction of switching losses and EMI filter requirements.

The proposed solution is described in detail in the paper and suitable design criteria are given. Comparison with existing line-frequency commutated rectifiers as well as with standard rectifiers with a passive L-C filter is given, in order to fully highlight advantages and limitation of the proposed solution.



Fig. 1 - Scheme of the line frequency commutated rectifier

II. CONVERTER DESCRIPTION AND OPERATION

Fig. 1 shows the scheme of the proposed high quality rectifier. Basically, it consists of a standard rectifier with an L-C filter, plus an additional switching unit consisting of two diodes, one switch, one capacitor and one inductor which are all rated at a fraction of the total power delivered to the load. The converter behavior can be better understood with the help of Fig. 2 which reports the simulated circuit main waveforms: auxiliary capacitor voltage u_{Ca} , output voltage

 $U_{\text{o}},$ rectified input current $i_{g},$ and auxiliary inductor current $i_{\text{La}}.$

The analysis can be broken into two parts: the discharging interval Ton+Toff, at the end of which the auxiliary capacitor C_a is charged at the voltage U_1 , and the resonance interval T_1+T_2 , in which we have the input current evolution. The switch gate signal can be applied at any instant around the line voltage zero crossing, and it is maintained for an interval Ton commanded by the output voltage regulator. During the on interval, which is relatively short compared to the line half-period, capacitor Ca, initially charged at the output voltage U_o, is partially discharged through L_a. Being the voltage across C_a still higher than the input voltage, during this interval, and the subsequent one (T_{off}), the input current remains zero. When the switch is turned-off, the current i_{La} flows to the output through diode D_a, continuing to discharge the auxiliary capacitor, until it becomes zero (interval Toff). The input current will start to flow at instant T_d when the input voltage becomes equal to the voltage U1. This occurs earlier respect to the bridge diodes turn-on natural instant due to the lower voltage U₁ as compared to U₀. During this phase, the input inductor resonates with the auxiliary capacitor, giving rise to the smoothed current waveform shown in Fig. 2. When, after interval T_1 , voltage u_{Ca} reaches the output voltage value, diode D starts to conduct and now the input inductor resonates with $C+C_a$. In this sense, the auxiliary capacitor can be considered part of the output voltage filter. This phase (interval T₂) lasts until the input current zeroes.



Fig. 2 - Rectifier main waveforms: auxiliary capacitor voltage u_{Ca} , output voltage U_o , rectified input current i_g and auxiliary inductor current i_{La}

A detailed description of the converter waveforms are reported in the appendix. Here we want just summarize some results:

 the voltage U₁ across capacitor C_a at the end of the discharge interval as well as the auxiliary switch and diode current stress depend only on the auxiliary inductor and capacitor values and on the switch on-time T_{on}, i.e.:

$$U_{I} = U_{o} \left(l - \sqrt{2 \left(l - \cos(\omega_{a} T_{on}) \right)} \right)$$
(1)

$$\hat{i}_{La} = \hat{i}_{Sa} = \hat{i}_{Da} = \frac{U_o}{Z_a} sin(\omega_a T_{on})$$

$$= \frac{1}{\sqrt{L_a C_a}} \text{ and } Z_a = \sqrt{\frac{L_a}{C_a}};$$
(2)

 similarly to the line frequency boost rectifier presented in [5-6], the switch voltage stress is simply given by the output voltage U_o.

where ω_{a}

• the input current waveform depends, besides on the input inductor value, on the resonant frequency $\omega_r = 1/\sqrt{LC_a}$ and on the voltage U₁ across capacitor C_a at the end of the discharge interval. The effects of the different parameters on the input current waveform are analyzed in successive sections.

III. COMPARISON WITH PREVIOUS SOLUTIONS

Many different solutions, based on modified L-C diode rectifier, have already been presented in the literature [3-6] aimed to achieve compliance with the IEC 1000-3-2 standard. For applications below 600W, these solutions exploit the difference between the absolute harmonic limits applied to class A loads and the relative limits applied to class D loads [1]. As known, the difference can be remarkable especially for low power applications. Thus, the goal of these modified rectifiers is to change the shape of the input current so as to stay outside the Class D template [1] for at least 5% of the line half period. For the low-power range of applications these solutions are surely cost-effective. However, for power levels higher then 600W, no more differences exist between Class A and D limits, thus the goal becomes simply to improve the input current harmonic content. In particular, since for the standard passive L-C filter the third harmonic is responsible for the loss of compliance [2,6], reduction of this harmonic is achieved at the expense of an increase of the high order harmonics. Thus, the latters now set the power limit for such solutions: as an example, Fig. 3 reports the comparison between the passive L-C rectifier and the line frequency commutated boost rectifier of [5,6] in terms of input current waveform and its spectrum ($U_i = 230 V_{rms}$, $P_o = 900 W$, L = 10mH). As we can see, the active solution reduces the third harmonic at the expense of an increase of the high order harmonics.

The proposed solution overcome this limitation since the input current waveform, shown in Fig. 2, is now smoother as compared to that of Fig. 3, making this rectifier well suited for high power levels. However, a meaningful comparison must be done taking into account all the aspects and in particular the higher circuit complexity and the need for a second inductor. To this purpose, the data collected in table I should help the reader in making this comparison and in selecting the power range in which this rectifier achieves the maximum advantage as compared with the other solutions.

The table reports the simulation results of the passive L-C rectifier (P), the proposed active rectifier (A_1) and the boost





rectifier (A_2) for three different power levels ranging from 600 up to 1200 W ($U_i = 230 V_{rms}$). For each power value the following data were collected: average output voltage U_o, inductor current values ensuring compliance with the standard, peak and rms inductor currents, coefficient distortion $K_L = L \cdot I_{rms} \cdot I_{pk}$ factor $DF = I_{g1rms}/I_{grms}$, displacement factor $\cos(\phi_1)$ power factor and $PF = DF \cdot cos(\phi_1)$. Coefficient K_L is related to the core size and is proportional to the product between the iron cross section A_e and the core window area A_w as it will be shown later. It is also related to the inductor peak energy, i.e. $K_L = \frac{2 E_L}{CF}$ where $CF = \frac{I_{pk}}{I_{rms}}$ is the crest factor. These data

show that, in this power range, the proposed solution allows a considerable reduction of the total magnetic component size as compared with both the passive filter and the line-frequency-commutated boost. Note, also, the higher output voltage achievable as a consequence of a lower input inductor value and of the switch boost action.

IV. DESIGN CONSIDERATIONS

The choice of the converter parameters depends on the designer objective. In fact, if the goal is just to comply with the standard without looking for a deep output voltage regulation, then the minimum switch on-time should be used, since it strongly affects the auxiliary inductor size and auxiliary switch and diode current stress, as can be seen by (2). On the other hand, allowing higher T_{on} values, an increase in the converter boost action is achieved, thus increasing the output voltage regulation against both line and load variations. In the following the analysis will be limited to the objective of achieving compliance with the standard at the minimum cost, i.e minimum size and device stresses.

A. Analysis of the Input Current Waveform

The input inductor waveform is influenced by three main factors: input inductor value, auxiliary capacitor value, which sets the resonant frequency during the secondary resonance interval T_1 and residual voltage U_1 on capacitor C_a at the end of the discharging process. Since the effects of these different factors combines together in a way which is very hard to put in correlation with the input current spectrum, simulation must be used in order to verify the design choices. Here, some simulations are reported which help to make a reasonable parameter value first estimation.

The effect of capacitor C_a can be analyzed by looking at Fig. 4: it shows the input current waveform and its spectrum at different values of parameter $\alpha = \omega_r / \omega_i$ at constant output power and normalized voltage $U_{1N} = U_1 / U_0$ $(\omega_r = 1/\sqrt{LC_a} \text{ and } \omega_i$: line voltage angular frequency). As we can see, higher C_a values (lower α) cause lower harmonic amplitudes, except for the third and nineth ones, together with lower peak current values. However, of the three waveforms it is the only which does not comply with the standard. Moreover, high C_a values cause high switch current stress since, at constant U_{1N} values, the current stress is proportional to the square root of C_a (from (1) and (2)).

As far as the effect of voltage U_1 is concerned, Fig. 5 shows the simulation results at different U_{1N} values at constant output power and converter parameters values. Actually, changing of voltage U_1 is achieved modifying the switch on-time. Decreasing U_1 causes a reduction of dead time T_d as well as reduction of third, nineth and thirteenth harmonics, while other harmonics increase. The peak input current is also decreased. However, only the waveform corresponding to $U_{1N} = 0.7$ complies with the standard. Moreover, lower U_1 values mean higher T_{on} value and consequently increase of the switch current stress.

From both Figs. 4 and 5, we can see that the purpose of the switching unit should be to modify as little as possible the

Tuble I. Comparison between passive and active recentlets at unrefert power levels													
		L	L _a	I _{gpeak}		I _{Lapeak}	I _{Larms}	E _L	K _L	K _{La}	DF	cos(\$)	PF
	[V]	լաոյ	լաոյ		[A]	[A]	[A]	լայլ	լայլ	լայլ			
600 - P	294	7		8.5	3.66			253	218		0.762	0.936	0.713
600 - A ₁	318	4	1	7.84	3.42	14.1	2.01	123	107	28.3	0.761	0.994	0.756
600 - A ₂	298	6		8.6	3.64			222	188		0.756	0.948	0.717
900 - P	258	19		9.77	5.13			908	953		0.888	0.859	0.763
900 - A ₁	310	6	1	9.64	4.62	19.5	2.61	279	267	51	0.849	0.992	0.842
900 - A ₂	287.4	10		9.88	4.82			488	476		0.93	0.859	0.799
1200 - A ₁	300	8	2	10.9	5.76	20.9	3.3	475	502	138	0.908	0.989	0.898
1200 - A ₂	268	18		11.19	6.22			1128	1254		0.924	0.907	0.838

Table I. Comparison between passive and active rectifiers at different power levels

 $P = passive; A_1 = active proposed solution; A_2 = active boost rectifier; DF = Distortion Factor; cos(\phi_1) = displacement factor; PF = Power Factor$

input current waveform as compared to that of the standard L-C rectifier, thus causing a decrease of the third harmonic amplitude below the limit without excessive increase of the high order harmonic amplitudes and with the minimum switching unit size.



Fig. 4 - Effect of variation of capacitor $C_a (\alpha = \omega_t/\omega_t)$. a) Input current waveform; b) input current spectrum ($U_i = 230 V_{rms}$, $P_o = 900W$, L = 6mH, $L_i = 1mH$, $U_{1N} = 0.72$).

B. Selection of L_a

The objective of this work is to provide compliance with the standards with a reduced overall magnetic component size as compared to previous solutions. To this purpose, the switch on-time should be kept as small as possible since it strongly affect the auxiliary inductor size and auxiliary switch and diode current stress, as can be seen by (2). Minimization of the auxiliary inductor size is accomplished by choosing the minimum value for inductor L_a taking into account the allowed switch current stress. In fact, the inductor core volume is related to the product between the iron cross section A_e and the core window area A_w , i.e.:

$$A_{w}A_{e} = \left(\frac{N}{k_{R}}\frac{I_{Larms}}{J}\right)\left(\frac{L_{a}I_{Lapk}}{NB_{max}}\right) = \frac{K_{La}}{k_{R}JB_{max}}$$
(3)

where B_{max} is the maximum flux density, J is the desired current density and k_R the window filling coefficient.

A plot of coefficient K_{La} as a function of inductor value L_a is reported in Fig. 6 for three different value of voltage U_1

showing a monotonic increase with the inductor value and a strong dependence on voltage U_1 , as already stated above.



Fig. 5 - Effect of variation of voltage U_1 ($U_{1N} = U_1/U_o$). a) Input current waveform; b) input current spectrum ($U_i = 230 V_{rms}$, $P_o = 900W$, L = 6mH, $L_1 = 1mH$, $\alpha = 6$)



Fig. 6 - Coefficient K_{La} as a function of the auxiliary inductor value. a) $U_{1N} = 0.4$; b) $U_{1N} = 0.5$; c) $U_{1N} = 0.6$. ($U_i = 230 V_{rms}$, $P_o = 900W$).

C. Selection of Output Capacitor C

For the selection of the output capacitor value, a good guess is the value obtained by the approximate analysis of the classical diode-bridge+capacitive filter rectifier, i.e.:

$$C = \frac{\pi P_o}{\omega_i U_o \Delta U_o} \tag{4}$$

where ΔU_o is the maximum allowed output voltage ripple (peak-to-peak). Note that, due to the extended diode conduction angle, caused by the filter inductor, and the switching unit operation, the effective output voltage ripple will be lower than the theoretical one.

D. Design Example

In order to give an idea of the magnetic component size, let us consider a practical example:

Converter specifications:

$$\begin{split} U_i &= 220 V_{rms} \pm 20\%, \quad P_o = 900 W, \quad L = 6 \text{ mH}, \quad L_a = 1 \text{ mH}, \\ C_a &= 44 \ \mu\text{F}, \ T_{on} = 60 \mu\text{s}. \end{split}$$

The material used for both the main and auxiliary inductors has the following parameter values:

relative permeability:...... $\mu_r = 11674$ flux density:.....B = 1.35 T

The utilized window filling coefficient k_R is 0.4, and the current density J is 3 A/mm². The auxiliar inductor parameters are:

iron cross section:	$\dots A_e = 1.6 \cdot 10^{-4} m^2$
window area:	$A_w = 1.92 \cdot 10^{-4} m^2$
mean magnetic path:	$\ell_{avg} = 0.089 \ m$
number of turns:	$N_a = 85$
wire diameter:	$\dots \Phi_a = 1 mm$
total winding area:	$A_{cu} = 1.67 \cdot 10^{-4} m^2$.
external core volume:	$Vol = 1.96 \cdot 10^{-5} m^3$

The main inductor parameter, calculated for the maximum input current (i.e. minimum input voltage), are:

	U
iron cross section:	 $A_e = 7.7 \cdot 10^{-4} m^2$
window area:	 $A_w = 3.63 \cdot 10^{-4} m^2$
mean magnetic path:	 $\ell_{avg} = 0.143 m$
number of turns:	 N = 69
air gap:	 $t_{gap} = 0.38 \ mm$
wire diameter:	 $\Phi = 1.6 mm$
total winding area:	 $A_{cu} = 3.37 \cdot 10^{-4} m^2$.
external core volume:	 $Vol = 1.27 \cdot 10^{-4} m^3$.

The rectifier output voltage at the minimum input voltage and nominal power is 227 V.

For the sake of comparison a similar design was carried out for the passive solution. The inductor value needed to comply with the standard for the same converter specification is 19 mH. The resulting inductor parameter are:

iron cross section:	$\dots A_e = 1.28 \cdot 10^{-3} m^2$
window area:	$\dots A_w = 7.84 \cdot 10^{-4} m^2$
mean magnetic path:	$\ell_{avg} = 0.22 \ m$
number of turns:	$\dots N = 131$
air gap:	$t_{gap} = 0.73 \ mm$
wire diameter:	$\Phi = 1.7 \ mm$
total winding area:	$A_{cu} = 7.43 \cdot 10^{-4} m^2$.
external core volume:	$Vol = 3.24 \cdot 10^{-4} m^3$.

The rectifier output voltage at the minimum input voltage and nominal power is 179V.

E. Output voltage regulation

As far as the output voltage regulation is concerned, we must consider separately the effects of load and input voltage variations, having in mind the constraint imposed by the maximum switch on-time which strongly affect the switching unit size. Thus, once we have selected the maximum Ton in order to accomplish compliance with the standards at nominal load and prescribed input voltage, the control can only reduce the switch on-time at load current decreasing. A standard PI regulator having a bandwidth well below the line frequency, like any other PFC regulator, is sufficient to accomplish this. Clearly, a minimum power level exists below which the output voltage regulation cannot be maintained, and it corresponds to the value for which the passive L-C rectifier (without the switching unit) achieves the same output voltage. At lower power levels, the output voltage increases toward the input voltage peak, like any standard rectifier. For this reason, a high output voltage reference is preferable, since it can be maintained for a broader load variation. To give an idea, the converter described in the experimental result section can maintain the output voltage regulation approximately down to 50% of the nominal power, even using a narrow pulse (70 μ s).

As far as the line voltage variation is concerned, having imposed a maximum switch on-time, the regulation of the output voltage can be maintained only for a small input voltage increase (which requires reduction of the switch on-time), while, at low input voltage, T_{on} is kept constant and equal to the maximum value allowed by the switching unit design, causing the decrease of the output voltage too.

V. EXPERIMENTAL MEASUREMENTS

In order to verify the results obtained by simulation a prototype was built having the following specifications:

$U_i = 230 V_{rms}$	$U_o = 292V$	$P_o = 900W$	$f_i=60Hz$
L = 6 mH	$L_a = 1 \text{ mH}$	$C_a = 44 \mu F$	$C = 470 \mu F$

The rectifier input current and voltage waveforms at nominal conditions are shown in Fig. 7 and the corresponding current harmonics amplitudes are reported in table II, together with Class A limits. As can be seen, the input current waveform well agrees with the simulation results and all the harmonics are well below their limits. The employed switch on-time is 70 μ s, as we can see from Fig. 8 which reports the auxiliary capacitor voltage u_{Ca} , the auxiliary inductor current i_{La} and the switch gate drive signal at the beginning of the line half period.

Comparing such waveforms with the idealized ones of Fig. 2 allows to easily recognize subintervals T_{on} , T_{off} , T_d and T_1 . The switch current stress is about 20A, while its voltage stress is limited by the output voltage. The measured efficiency is 96%, while the power factor is 0.85, and it is almost totally dominated by the distortion factor DF which results 0.86 (THD = 59%).



 Table II - MEASURED INPUT CURRENT HARMONICS

In	Harm.	Class A limits
	[A _{rms}]	[A _{rms}]
I ₃	2.18	2.30
I ₅	0.73	1.14
I ₇	0.46	0.77
I ₉	0.028	0.40
I ₁₁	0.14	0.33
I ₁₃	0.05	0.21
I ₁₅	0.058	0.15
I ₁₇	0.048	0.132
I ₁₉	0.022	0.118
I ₂₁	0.026	0.107



VI. CONCLUSIONS

The paper presented a modification of conventional rectifiers with a passive L-C filter which helps to make compliance with harmonic standard with a reduced overall magnetic component size as compared to previous solutions. The added switching unit employs a line frequency commutated switch rated at a fraction of the total power delivered to the load. Its inherent boost action allows regulation of the output voltage against load variations, without affecting the converter efficiency.

Measurements on a 900W prototype have shown a good agreement with theoretical expectations.

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APPENDIX

In order to derive the input current equations during the different time intervals in the line half period let us refers to Fig. 2 and to Fig. A1 which reports the corresponding converter subtopologies. The following equations hold on the assumption that during the total discharge interval of capacitor C_a ($T_{on}+T_{off}$) the input current stays at zero since the rectified input voltage is lower than u_{Ca} . Moreover the output capacitor is considered big enought to maintain constant the output voltage. The input voltage is given by:

$$u_g(t) = \hat{U}_g |sin(\omega_i t)$$

1) Discharge interval

a) $0 \le t \le T_{on}$

A resonance between C_a and L_a occurs:

$$i_{La}(t) = \frac{U_o}{Z_a} \sin(\omega_a t)$$
(A.1)

$$\begin{split} u_{Ca}(t) &= U_{o} \cos(\omega_{a} t) \\ \text{where } \omega_{a} &= \frac{1}{\sqrt{L_{a}C_{a}}} Z_{a} = \sqrt{\frac{L_{a}}{C_{a}}} . \\ \text{b) } T_{on} &\leq t \leq T_{on} + T_{off} \\ C_{a} \text{ continue to discharge until current } i_{La} \text{ zeroes.} \\ i_{La}(t) &= I_{a0} \cos(\omega_{a}(t - T_{on})) - \frac{U_{o} - U_{a0}}{Z_{a}} \sin(\omega_{a}(t - T_{on})) \\ u_{Ca}(t) &= U_{o} - Z_{a}I_{a0} \sin(\omega_{a}(t - T_{on})) - (U_{o} - U_{a0}) \cos(\omega_{a}(t - T_{on})) \end{split}$$
 $\begin{aligned} \text{(A.2)} \end{split}$

where the initial conditions I_{a0} and U_{a0} are given by:

$$I_{a0} = \frac{U_o}{Z_a} \sin(\omega_a T_{on})$$

$$U_{a0} = U_o \cos(\omega_a T_{on})$$
(A.3)

Interval T_{off} can be calculated setting current i_{La} to zero, i.e.:

$$T_{\rm off} = \frac{1}{\omega_{\rm a}} \operatorname{atan} \left(\frac{\sin(\omega_{\rm a} T_{\rm on})}{1 - \cos(\omega_{\rm a} T_{\rm on})} \right)$$
(A.4)

The voltage across C_a at the end of the discharge interval $T_{\text{on}}\text{+}T_{\text{off}}$ is given by:

$$U_{1} = U_{o} \left(1 - \sqrt{2 \left(1 - \cos \left(\omega_{a} T_{on} \right) \right)} \right)$$
(A.5)

2) Secondary resonance interval $T_d \le t \le T_d + T_1$

This interval starts at $t = T_d$ when the rectified input voltage becomes equal to voltage U_1 across C_a , i.e.

$$T_{d} = \frac{1}{\omega_{i}} \operatorname{asin}\left(\frac{U_{1}}{\hat{U}_{g}}\right)$$
(A.6)

$$a_{i} = -b_{i} \sqrt{\left(\frac{\hat{U}_{g}}{U_{1}}\right)^{2} - 1} \qquad a_{u} = -b_{u} \sqrt{\left(\frac{\hat{U}_{g}}{U_{1}}\right)^{2} - 1}$$

$$b_{i} = -\frac{U_{1}}{\omega_{i}L} \left(\frac{1}{\alpha^{2} - 1}\right) \qquad b_{u} = -U_{1} \left(\frac{\alpha^{2}}{\alpha^{2} - 1}\right)$$
(A.7a)

$$i_{g}(t) = a_{i} \left[\cos(\omega_{i}(t - T_{d})) - \cos(\omega_{r}(t - T_{d})) \right] +$$

$$+ b_{i} \left[\sin(\omega_{i}(t - T_{d})) - \frac{1}{\alpha} \sin(\omega_{r}(t - T_{d})) \right]$$

$$u_{Ca}(t) = U_{1} + a_{u} \left[\sin(\omega_{i}(t - T_{d})) - \frac{1}{\alpha} \sin(\omega_{r}(t - T_{d})) \right] +$$

$$+ b_{u} \left[\left(1 - \cos(\omega_{i}(t - T_{d})) \right) - \frac{1}{\alpha^{2}} \cos(\omega_{r}(t - T_{d})) \right]$$
(A.7c)

where $\omega_r = \frac{1}{\sqrt{L C_a}}$ and $\alpha = \frac{\omega_r}{\omega_i}$. This interval ends when

the voltage across the auxiliary capacitor C_a reaches the output voltage value, i.e. $u_{\,Ca}\big(T_d+T_l\,\big)\!=\!U_{\,o}\,.$

Let us indicate the input current value at this istant as I_{g0} .

3) Main resonance interval
$$T_d+T_1 \le t \le T_d+T_1+T_2$$

 $i_g(t) = I_{g0} +$
 $+\frac{\hat{U}_g}{\omega_i L} \left[\cos(\omega_i(T_d + T_1)) - \cos(\omega_i t) - \frac{U_o}{\hat{U}_g} \omega_i(t - T_d - T_1) \right]$
(A.8)

After interval T_2 , the input current zeroes and remains zero until the next line half period.



Fig. A1 - Converter subtopologies in a line half period. a) discharge interval $T_{on}+T_{off}$, b) resonance interval T_1+T_2